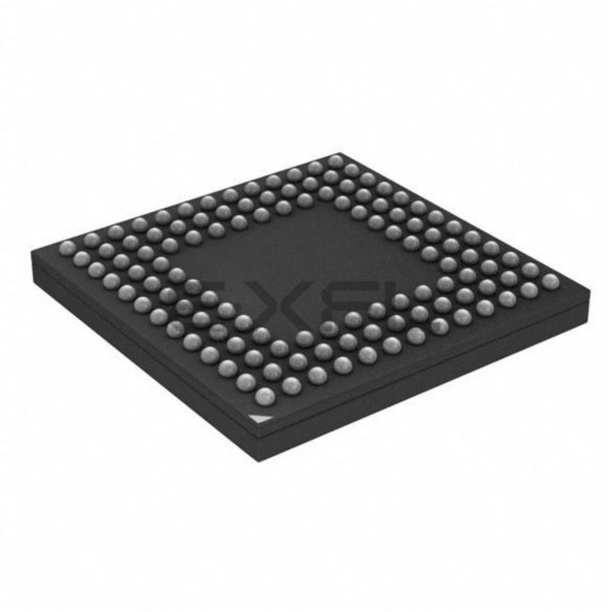

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b420f2048gl120-ar

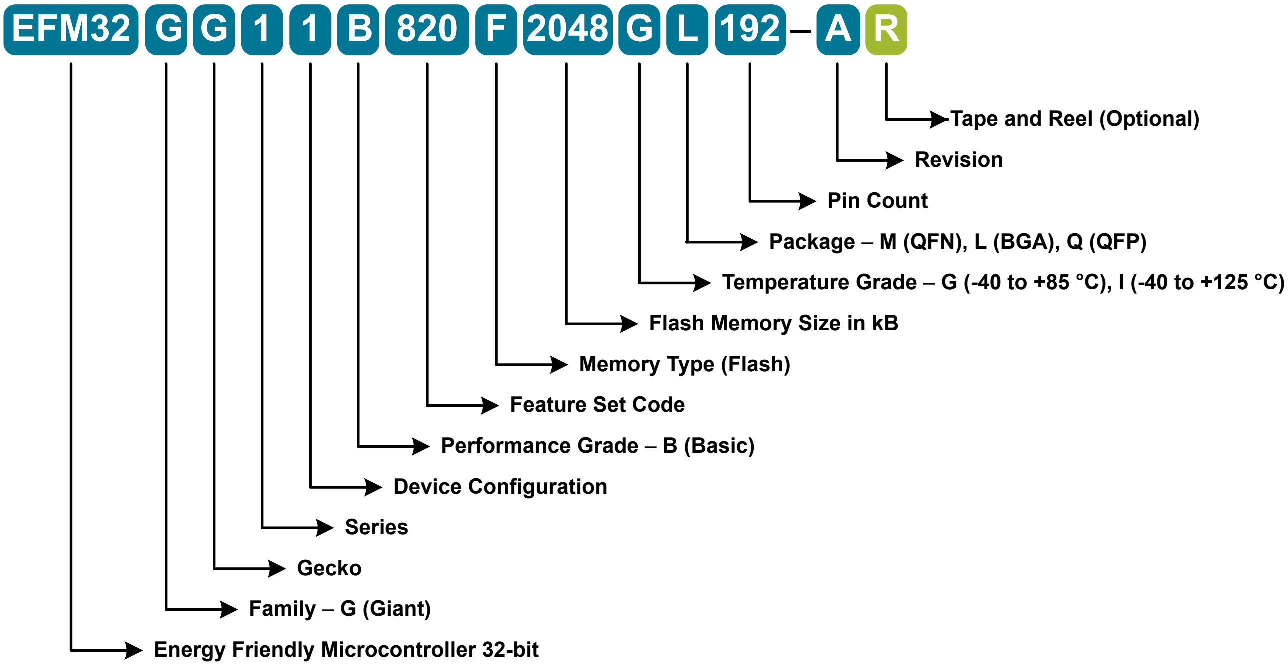

Figure 2.1. Ordering Code Key

4.1.7 Current Consumption

4.1.7.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.7. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	72 MHz HFRCO, CPU running Prime from flash	—	120	—	μA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	120	TBD	μA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	140	—	μA/MHz
		50 MHz crystal, CPU running while loop from flash	—	123	—	μA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	122	TBD	μA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	124	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	126	TBD	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	131	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	319	TBD	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	107	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	262	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	72 MHz HFRCO	—	57	TBD	μA/MHz
		50 MHz crystal	—	60	—	μA/MHz
		48 MHz HFRCO	—	59	TBD	μA/MHz
		32 MHz HFRCO	—	61	—	μA/MHz
		26 MHz HFRCO	—	63	TBD	μA/MHz
		16 MHz HFRCO	—	68	—	μA/MHz
		1 MHz HFRCO	—	255	TBD	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	55	—	μA/MHz
		1 MHz HFRCO	—	210	—	μA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.9	—	μA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	4.3	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.8	TBD	μA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFRCO	—	3.6	TBD	μA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.08	—	μA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.69	—	μA
		128 byte RAM retention, no RTCC	—	0.69	TBD	μA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.16	TBD	μA
Current consumption of peripheral power domain 1, with voltage scaling enabled	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[1]	—	0.68	—	μA
Current consumption of peripheral power domain 2, with voltage scaling enabled	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[1]	—	0.28	—	μA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.94	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.62	—	µA
		128 byte RAM retention, no RTCC	—	0.62	—	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.13	—	µA
Current consumption of peripheral power domain 1, with voltage scaling enabled, DCDC in LP mode[3]	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[4]	—	0.68	—	µA
Current consumption of peripheral power domain 2, with voltage scaling enabled, DCDC in LP mode[3]	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[4]	—	0.28	—	µA

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.10.6 USB High-Frequency RC Oscillator (USHFRCO)

Table 4.17. USB High-Frequency RC Oscillator (USHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{USHFRCO\_ACC}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
		USB clock recovery enabled, Active connection as device, FINETUNINGEN[1] = 1	-0.25	—	0.25	%
Start-up time	$t_{USHFRCO}$		—	300	—	ns
Current consumption on all supplies	$I_{USHFRCO}$	$f_{USHFRCO}$ = 48 MHz, FINETUNINGEN[1] = 1	—	340	TBD	µA
		$f_{USHFRCO}$ = 50 MHz, FINETUNINGEN[1] = 0	—	342	TBD	µA
		$f_{USHFRCO}$ = 48 MHz, FINETUNINGEN[1] = 0	—	292	TBD	µA
		$f_{USHFRCO}$ = 32 MHz, FINETUNINGEN[1] = 0	—	223	TBD	µA
		$f_{USHFRCO}$ = 16 MHz, FINETUNINGEN[1] = 0	—	132	TBD	µA
Period jitter	$PJ_{USHFRCO}$		—	0.2	—	% RMS

Note:

1. In the CMU_USHFRCOCTRL register.

4.1.10.7 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.18. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		TBD	1	TBD	kHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	µs
Settling time, (output settled within 1% of steady state value),	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption[2]	I_{IDAC}	EM0 or EM1 Source mode, excluding output current, Across operating temperature range	—	11	TBD	µA
		EM0 or EM1 Sink mode, excluding output current, Across operating temperature range	—	13	TBD	µA
		EM2 or EM3 Source mode, excluding output current, T = 25 °C	—	0.05	—	µA
		EM2 or EM3 Sink mode, excluding output current, T = 25 °C	—	0.07	—	µA
		EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C	—	11	—	µA
		EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C	—	13	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.11	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.06	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.04	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.03	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.29	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.27	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.12	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.03	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

SPI Slave Timing

Table 4.35. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1, 3, 2]	t_{SCLK}		6 * $t_{HFPERCLK}$	—	—	ns
SCLK high time[1, 3, 2]	t_{SCLK_HI}		2.5 * $t_{HFPERCLK}$	—	—	ns
SCLK low time[1, 3, 2]	t_{SCLK_LO}		2.5 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1, 3]	$t_{CS\_ACT\_MI}$		24	—	69	ns
CS disable to MISO [1, 3]	$t_{CS\_DIS\_MI}$		19	—	175	ns
MOSI setup time [1, 3]	t_{SU_MO}		7	—	—	ns
MOSI hold time [1, 3, 2]	t_{H_MO}		6	—	—	ns
SCLK to MISO [1, 3, 2]	t_{SCLK_MI}		16 + 1.5 * $t_{HFPERCLK}$	—	43 + 2.5 * $t_{HFPERCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

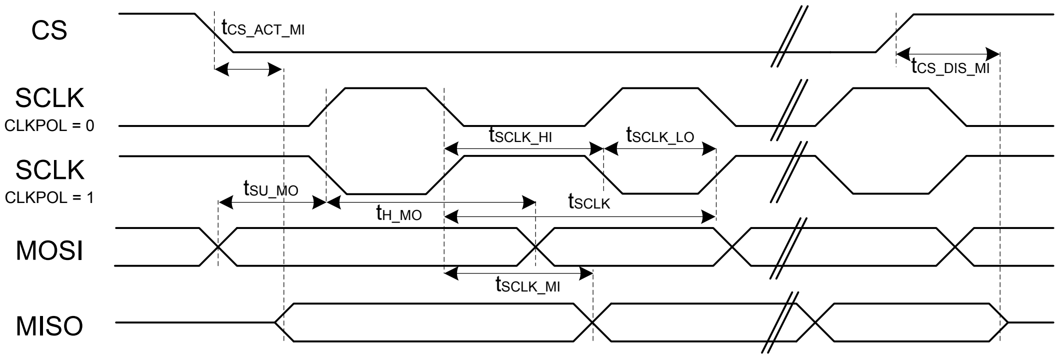

Figure 4.2. SPI Slave Timing Diagram

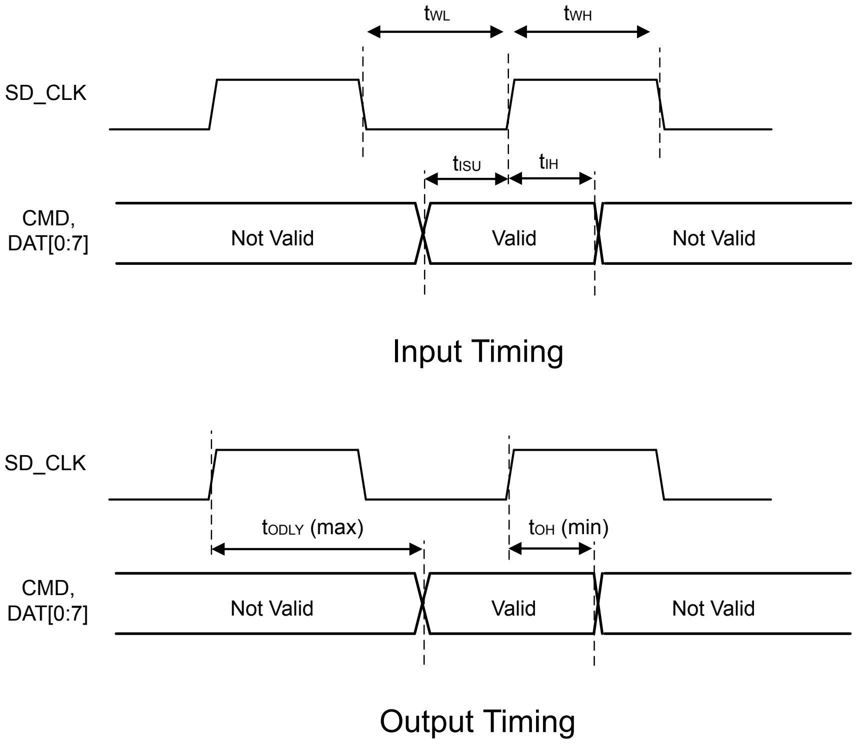

Figure 4.17. SDIO MMC SDR Mode Timing

QSPI DDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 53, RX DLL = 88, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.57. QSPI DDR Mode Timing (Locations 1, 2)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Half SCLK period	T/2	HFXO	$(1/F_{SCLK}) * 0.4 - 0.4$	—	—	ns
		HFRCO, AUXHFRCO, USHFRCO	$(1/F_{SCLK}) * 0.44$	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 6.6	ns
Output hold	t_{OH}		T/2 - 52.2	—	—	ns
Input setup	t_{SU}		44.8	—	—	ns
Input hold	t_H		-2.4	—	—	ns

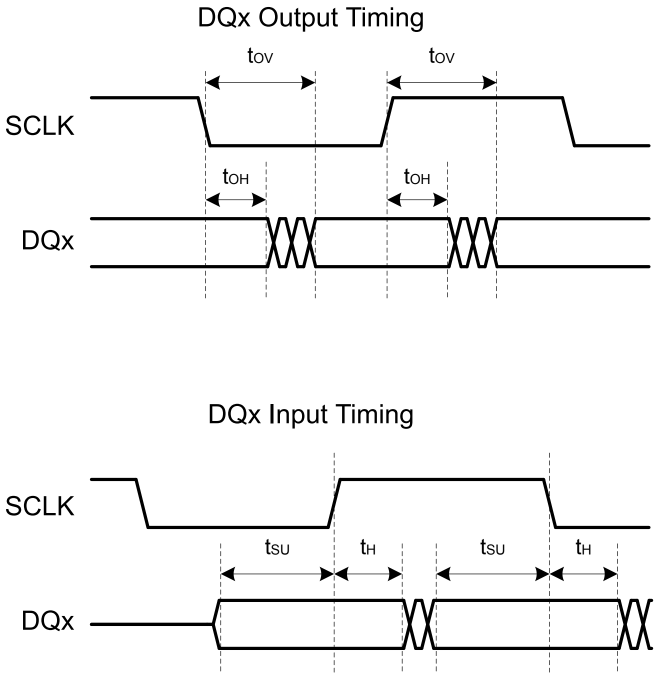

Figure 4.22. QSPI DDR Timing Diagrams

QSPI DDR Flash Timing Example

This example uses timing values for location 0 (DDR mode) to demonstrate the calculation of allowable flash timing using the QSPI in DDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 8 MHz from the HFXO clock source:
- The resulting minimum half-period, T/2(min) = $(1/F_{SCLK}) * 0.4 - 0.4 = 49.6$ ns.
- Flash will see a minimum setup time of $T/2 – t_{OV} = T/2 – (T/2 – 5.0) = 5.0$ ns.
- Flash will see a minimum hold time of $t_{OH} = T/2 – 39.4 = 49.6 – 39.4 = 10.2$ ns.
- Flash can have a maximum output valid time of $T/2 – t_{SU} = T/2 – 33.1 = 49.6 – 33.1 = 16.5$ ns.
- Flash can have a minimum output hold time of $t_H = - 0.9$ ns.

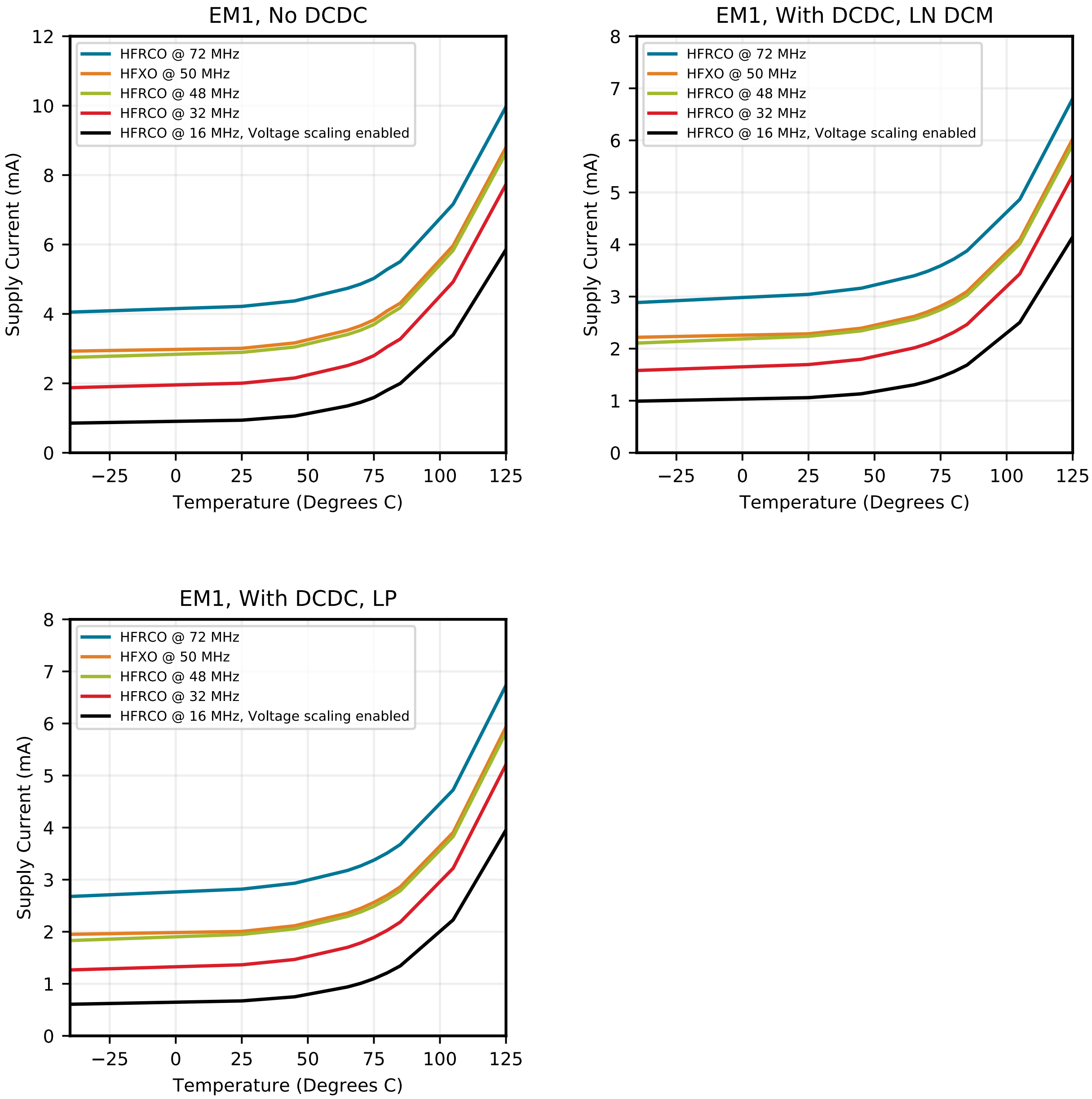

Figure 4.25. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF3	B9	GPIO
PF1	B10	GPIO (5V)	PF12	B11	GPIO
VBUS	B12	USB VBUS signal and auxiliary input to 5 V regulator.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 K12 L12 L13 M8 M11 N8	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L14	Digital IO power supply 0.
PF0	C10	GPIO (5V)	PE4	C11	GPIO
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PE5	D11	GPIO
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PE6	E11	GPIO
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE7	F11	GPIO
PC8	F12	GPIO (5V)	PC9	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE0	G11	GPIO (5V)
PE1	G12	GPIO (5V)	PE3	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
PC7	H13	GPIO	PD14	J1	GPIO (5V)

5.13 EFM32GG11B5xx in QFP64 Device Pinout

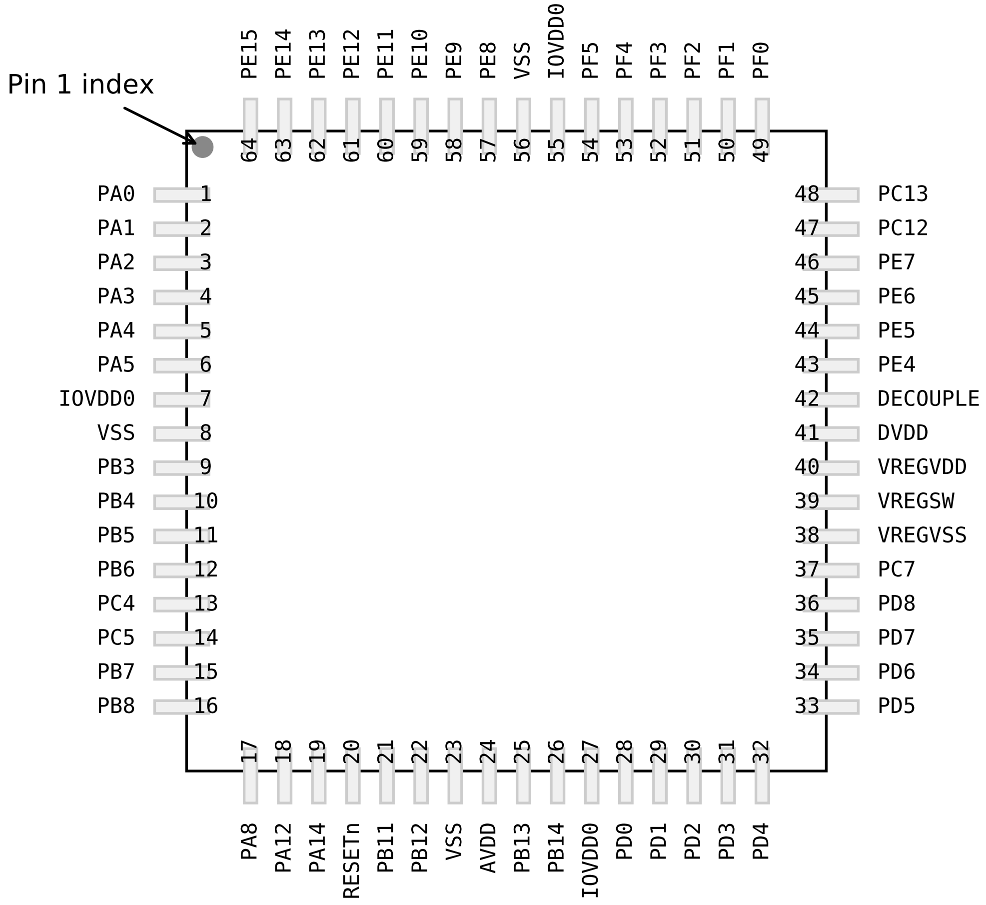

Figure 5.13. EFM32GG11B5xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.13. EFM32GG11B5xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

5.17 EFM32GG11B5xx in QFN64 Device Pinout

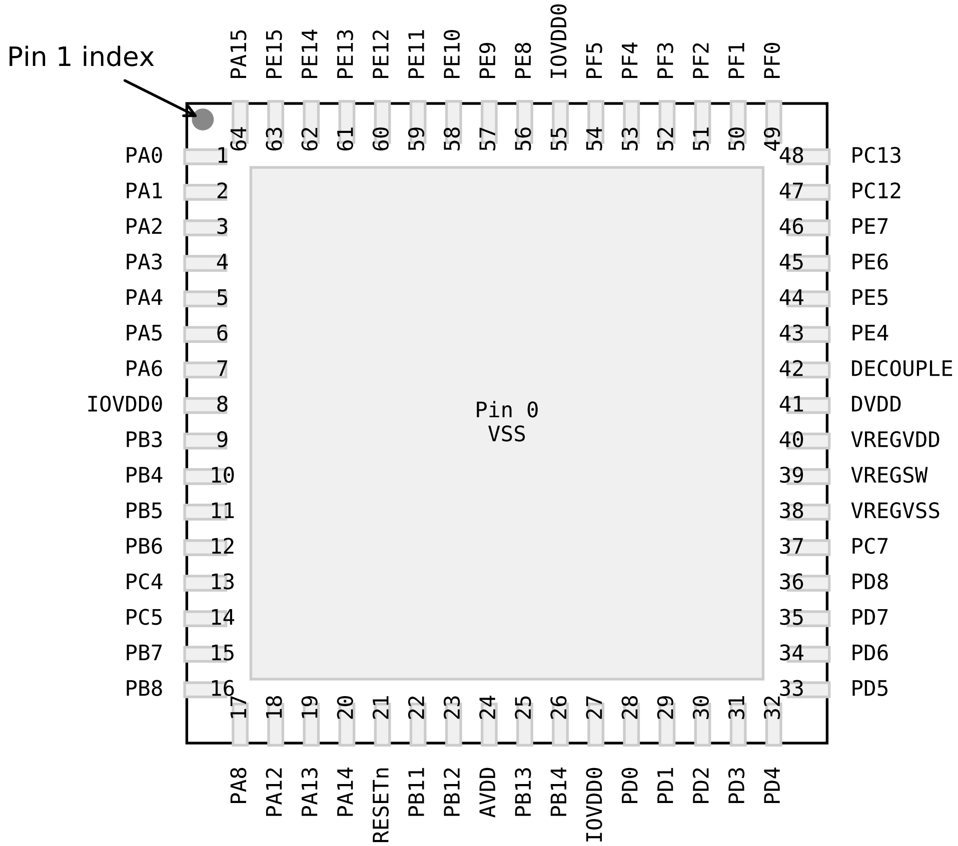

Figure 5.17. EFM32GG11B5xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.17. EFM32GG11B5xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
QSPI0_DQ7	0: PE11 1: PB6 2: PG8		Quad SPI 0 Data 7.
QSPI0_DQS	0: PF9 1: PE15 2: PG11		Quad SPI 0 Data S.
QSPI0_SCLK	0: PF6 1: PE14 2: PG0		Quad SPI 0 Serial Clock.
SDIO_CD	0: PF8 1: PC4 2: PA6 3: PB10		SDIO Card Detect.
SDIO_CLK	0: PE13 1: PE14		SDIO Serial Clock.
SDIO_CMD	0: PE12 1: PE15		SDIO Command.
SDIO_DAT0	0: PE11 1: PA0		SDIO Data 0.
SDIO_DAT1	0: PE10 1: PA1		SDIO Data 1.
SDIO_DAT2	0: PE9 1: PA2		SDIO Data 2.
SDIO_DAT3	0: PE8 1: PA3		SDIO Data 3.
SDIO_DAT4	0: PD12 1: PA4		SDIO Data 4.
SDIO_DAT5	0: PD11 1: PA5		SDIO Data 5.
SDIO_DAT6	0: PD10 1: PB3		SDIO Data 6.

Alternate	LOCATION		
Functionality	**0 - 3**	**4 - 7**	**Description**
SDIO_DAT7	0: PD9 1: PB4		SDIO Data 7.
SDIO_WP	0: PF9 1: PC5 2: PB15 3: PB9		SDIO Write Protect.
TIM0_CC0	0: PA0 1: PF6 2: PD1 3: PB6	4: PF0 5: PC4 6: PA8 7: PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PF7 2: PD2 3: PC0	4: PF1 5: PC5 6: PA9 7: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PF8 2: PD3 3: PC1	4: PF2 5: PA7 6: PA10 7: PA13	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PC13 2: PF3 3: PC2	4: PB7	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PC14 2: PF4 3: PC3	4: PB8	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PC15 2: PF5 3: PC4	4: PB11	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PC13 1: PE10 2: PB0 3: PB7	4: PD6 5: PF2 6: PF13 7: PI6	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PC14 1: PE11 2: PB1 3: PB8	4: PD7 5: PF3 6: PF14 7: PI7	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PC15 1: PE12 2: PB2 3: PB11	4: PC13 5: PF4 6: PF15 7: PI8	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PC12 1: PE13 2: PB3 3: PB12	4: PC14 5: PF12 6: PF5 7: PI9	Timer 1 Capture Compare input / output channel 3.
TIM2_CC0	0: PA8 1: PA12 2: PC8 3: PF2	4: PB6 5: PC2 6: PG8 7: PG5	Timer 2 Capture Compare input / output channel 0.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
U0_TX	0: PF6 1: PE0 2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.
U1_CTS	0: PC14 1: PF9 2: PB11 3: PE4	4: PC4 5: PH13	UART1 Clear To Send hardware flow control input.
U1_RTS	0: PC15 1: PF8 2: PB12 3: PE5	4: PC5 5: PH14	UART1 Request To Send hardware flow control output.
U1_RX	0: PC13 1: PF11 2: PB10 3: PE3	4: PE13 5: PH12	UART1 Receive input.
U1_TX	0: PC12 1: PF10 2: PB9 3: PE2	4: PE12 5: PH11	UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12 6: PG14	USART0 clock input / output.
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13 6: PG15	USART0 chip select input / output.
US0_CTS	0: PE14 1: PE3 2: PC7 3: PC13	4: PB6 5: PB11 6: PH0	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PE15 1: PE2 2: PC6 3: PC12	4: PB5 5: PD6 6: PH1	USART0 Request To Send hardware flow control output.
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1 6: PG13	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0 6: PG12	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4 6: PB2	USART1 chip select input / output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM0_CC2	0: PE6 1: PD14 2: PG4 3: PG10	4: PF1 5: PB2 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0	0: PE10 1: PD15 2: PA12 3: PG11	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1	0: PE11 1: PG0 2: PA13 3: PG12	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	0: PE12 1: PG1 2: PA14 3: PG13	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	4: PE3 5: PE7 6: PH8 7: PH12	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14 1: PD3 2: PD7 3: PE0	4: PE4 5: PI0 6: PH9 7: PH13	Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	0: PD0 1: PD4 2: PD8 3: PE1	4: PE5 5: PI1 6: PH10 7: PH14	Wide timer 1 Capture Compare input / output channel 2.
WTIM1_CC3	0: PD1 1: PD5 2: PC6 3: PE2	4: PE6 5: PI2 6: PH11 7: PH15	Wide timer 1 Capture Compare input / output channel 3.
WTIM2_CC0	0: PA9 1: PA12 2: PB9 3: PB12	4: PG14 5: PD3 6: PH4 7: PH7	Wide timer 2 Capture Compare input / output channel 0.
WTIM2_CC1	0: PA10 1: PA13 2: PB10 3: PG12	4: PG15 5: PD4 6: PH5 7: PH8	Wide timer 2 Capture Compare input / output channel 1.
WTIM2_CC2	0: PA11 1: PA14 2: PB11 3: PG13	4: PH0 5: PD5 6: PH6 7: PH9	Wide timer 2 Capture Compare input / output channel 2.
WTIM3_CC0	0: PD9 1: PC8 2: PC11 3: PC14	4: PI3 5: PI6 6: PB6 7: PF13	Wide timer 3 Capture Compare input / output channel 0.
WTIM3_CC1	0: PD10 1: PC9 2: PC12 3: PF10	4: PI4 5: PI7 6: PF4 7: PF14	Wide timer 3 Capture Compare input / output channel 1.

Table 5.29. CSEN Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
CEXT																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
CEXT_SENSE																																	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.30. IDAC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT1Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	

6. BGA192 Package Specifications

6.1 BGA192 Package Dimensions

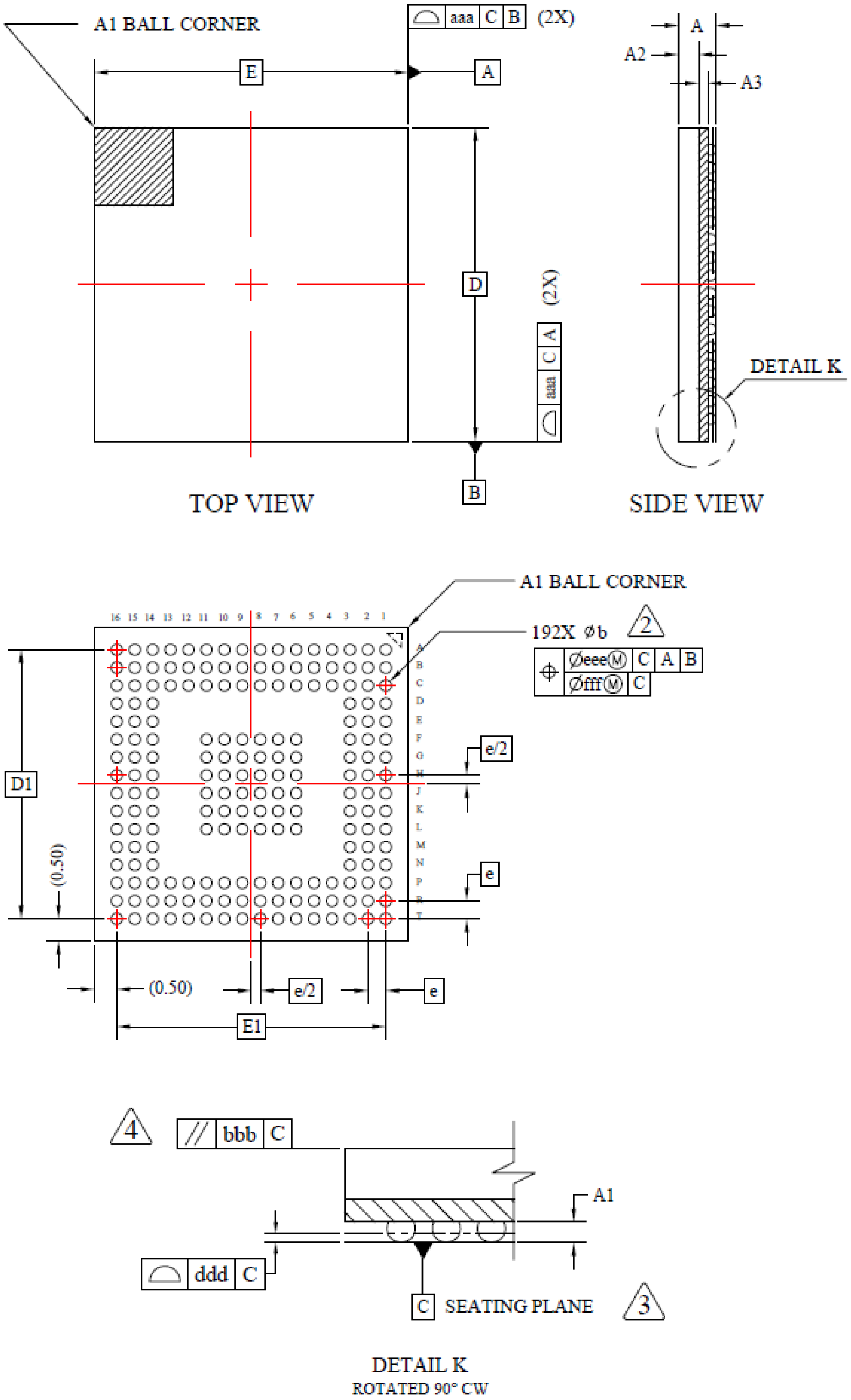

Figure 6.1. BGA192 Package Drawing

10.2 TQFP100 PCB Land Pattern

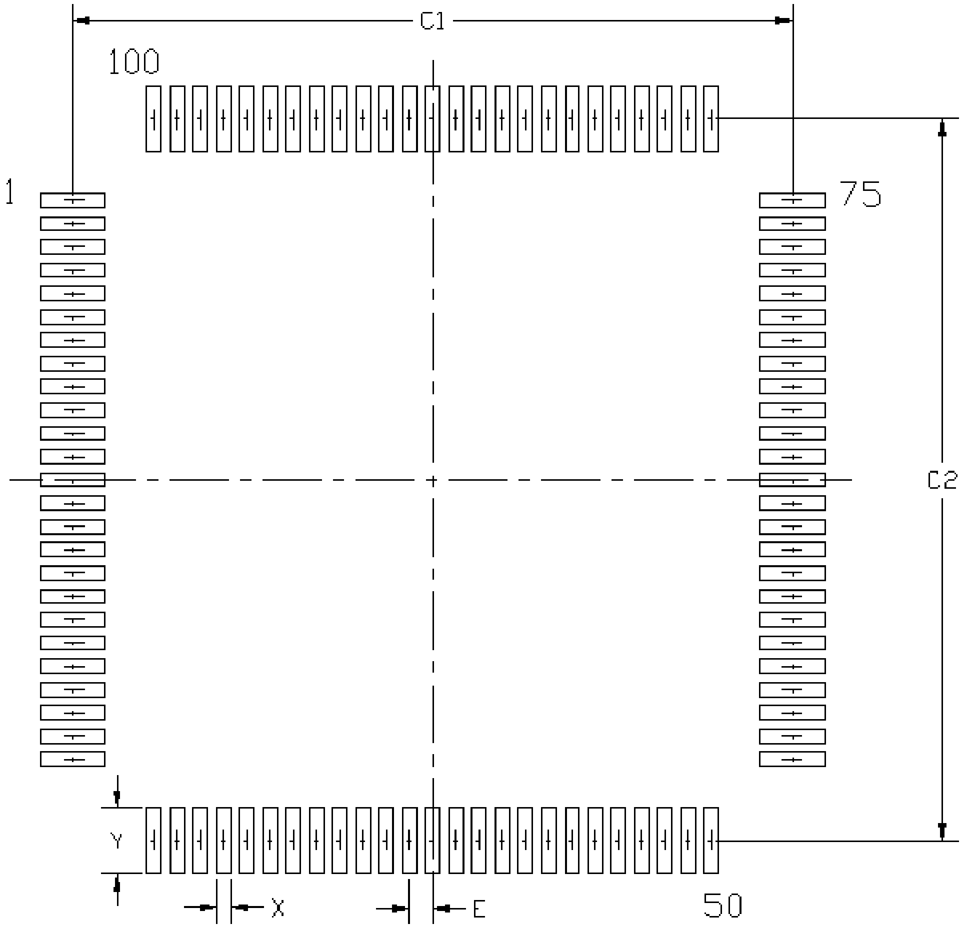

Figure 10.2. TQFP100 PCB Land Pattern Drawing