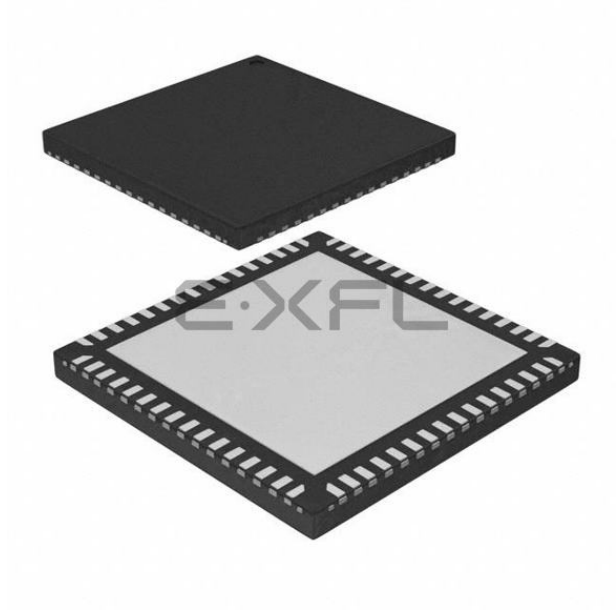
Silicon Labs - EFM32GG11B420F2048GM64-AR Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b420f2048gm64-ar

1. Feature List

The EFM32GG11 highlighted features are listed below.

- **ARM Cortex-M4 CPU platform**
  - High performance 32-bit processor @ up to 72 MHz
  - DSP instruction support and Floating Point Unit
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 80 µA/MHz in Active Mode (EM0)
  - 2.1 µA EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Up to 2048 kB flash program memory**
  - Dual-bank with read-while-write support
- **Up to 512 kB RAM data memory**
  - 256 kB with ECC (SEC-DED)
- **Octal/Quad-SPI Flash Memory Interface**
  - Supports 3 V and 1.8 V memories
  - 1/2/4/8-bit data bus
  - Quad-SPI Execute In Place (XIP)
- **Communication Interfaces**
  - Low-energy Universal Serial Bus (USB) with Device and Host support
    - Fully USB 2.0 compliant
    - On-chip PHY and embedded 5V to 3.3V regulator
    - Crystal-free Device mode operation
    - Patent-pending Low-Energy Mode (LEM)
  - SD/MMC/SDIO Host Controller
    - SD v3.01, SDIO v3.0 and MMC v4.51
    - 1/4/8-bit bus width
  - 10/100 Ethernet MAC with MII/RMII interface
    - IEEE1588-2008 precision time stamping
    - Energy Efficient Ethernet (802.3az)
  - Up to 2× CAN Bus Controller
    - Version 2.0A and 2.0B up to 1 Mbps
  - 6× Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
    - Triple buffered full/half-duplex operation with flow control
    - Ultra high speed (36 MHz) operation on one instance
  - 2× Universal Asynchronous Receiver/ Transmitter
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 3× I^2C Interface with SMBus support
    - Address recognition in EM3 Stop Mode
- **Up to 144 General Purpose I/O Pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 5 V tolerance on select pins
  - Asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **Up to 24 Channel DMA Controller**
- **Up to 24 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **External Bus Interface for up to 4x256 MB of external memory mapped space**
  - TFT Controller with Direct Drive
  - Per-pixel alpha-blending engine
- **Hardware Cryptography**
  - AES 128/256-bit keys
  - ECC B/K163, B/K233, P192, P224, P256
  - SHA-1 and SHA-2 (SHA-224 and SHA-256)
  - True Random Number Generator (TRNG)
- **Hardware CRC engine**
  - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
  - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8×36 segments**
  - Voltage boost, contrast and autonomous animation
  - Patented low-energy LCD driver
- **Backup Power Domain**
  - RTCC and retention registers in a separate power domain, available down to energy mode EM4H
  - Operation from backup battery when main power absent/ insufficient
- **Ultra Low-Power Precision Analog Peripherals**
  - 2× 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
    - On-chip temperature sensor
  - 2× 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
  - Digital to Analog Current Converter (IDAC)
  - Up to 4× Analog Comparator (ACMP)
  - Up to 4× Operational Amplifier (OPAMP)
  - Robust current-based capacitive sensing with up to 64 inputs and wake-on-touch (CSEN)
  - Up to 108 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
  - Supply Voltage Monitor

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	USB	Ethernet	QSPI	SDIO	LCD	GPIO	Package	Temp Range
EFM32GG11B820F2048GL192-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85°C
EFM32GG11B840F1024GL192-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85°C
EFM32GG11B820F2048GL152-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +85°C
EFM32GG11B820F2048IL152-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +125°C
EFM32GG11B840F1024GL152-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +85°C
EFM32GG11B840F1024IL152-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +125°C
EFM32GG11B820F2048GL120-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +85°C
EFM32GG11B820F2048IL120-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +125°C
EFM32GG11B840F1024GL120-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +85°C
EFM32GG11B840F1024IL120-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +125°C
EFM32GG11B820F2048GQ100-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85°C
EFM32GG11B820F2048IQ100-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +125°C
EFM32GG11B840F1024GQ100-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85°C
EFM32GG11B840F1024IQ100-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +125°C
EFM32GG11B820F2048GQ64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +85°C
EFM32GG11B820F2048GM64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +85°C
EFM32GG11B820F2048IQ64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +125°C
EFM32GG11B820F2048IM64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +125°C
EFM32GG11B840F1024GQ64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +85°C
EFM32GG11B840F1024GM64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +85°C
EFM32GG11B840F1024IQ64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +125°C
EFM32GG11B840F1024IM64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +125°C
EFM32GG11B520F2048GL120-A	2048	512	Yes	No	No	No	No	Yes	95	BGA120	-40 to +85°C
EFM32GG11B510F2048GL120-A	2048	384	Yes	No	No	No	No	Yes	95	BGA120	-40 to +85°C
EFM32GG11B520F2048IL120-A	2048	512	Yes	No	No	No	No	Yes	95	BGA120	-40 to +125°C
EFM32GG11B510F2048IL120-A	2048	384	Yes	No	No	No	No	Yes	95	BGA120	-40 to +125°C
EFM32GG11B520F2048GQ100-A	2048	512	Yes	No	No	No	No	Yes	83	QFP100	-40 to +85°C
EFM32GG11B510F2048GQ100-A	2048	384	Yes	No	No	No	No	Yes	83	QFP100	-40 to +85°C
EFM32GG11B520F2048IQ100-A	2048	512	Yes	No	No	No	No	Yes	83	QFP100	-40 to +125°C
EFM32GG11B510F2048IQ100-A	2048	384	Yes	No	No	No	No	Yes	83	QFP100	-40 to +125°C

4.1.5 5V Regulator

V_{VREGI} = 5 V, V_{VREGO} = 3.3 V, C_{VREGI} = 10 µF, C_{VREGO} = 4.7 µF, unless otherwise specified.

Table 4.5. 5V Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VREGI or VBUS input voltage range	V_{VREGI}	Regulating output	2.7	—	5.5	V
		Bypass mode enabled	2.7	—	3.8	V
VREGO output voltage	V_{VREGO}	Regulating output, 3.3 V setting	3.1	3.3	3.5	V
		EM4S open-loop output, I_{OUT} < 100 µA	1.8	—	3.8	V
Voltage output step size	V_{VREGO_SS}		—	0.1	—	V
Resistance in Bypass Mode	R_{BYP}	Bypass mode enabled	—	1.2	TBD	Ω
Output current	I_{OUT}	EM0 or EM1, V_{VREGI} > V_{VREGO} + 0.6 V	—	—	200	mA
		EM0 or EM1, V_{VREGI} > V_{VREGO} + 0.3 V	—	—	100	mA
		EM2, EM3, or EM4H, V_{VREGI} > V_{VREGO} + 0.6 V	—	—	2	mA
		EM2, EM3, or EM4H, V_{VREGI} > V_{VREGO} + 0.3 V	—	—	0.5	mA
		EM4S	—	—	20	µA
Load regulation	LR_{VREGO}	EM0 or EM1	—	0.10	—	mV/mA
		EM2, EM3, or EM4H	—	2.5	—	mV/mA
DC power supply rejection	PSR_{DC}		—	40	—	dB
VREGI or VBUS bypass capacitance	C_{VREGI}		—	10	—	µF
VREGO bypass capacitance	C_{VREGO}		1	4.7	10	µF
Supply current consumption	I_{VREGI}	EM0 or EM1, No load	—	29	—	µA
		EM2, EM3, or EM4H, No load	—	270	—	nA
		EM4S, No load	—	70	—	nA
VREGI and VBUS detection high threshold	V_{DET_H}		TBD	1.18	—	V
VREGI and VBUS detection low threshold	V_{DET_L}		—	1.12	TBD	V
Current monitor transfer ratio	$IMON_{XF}$	Translation of current through VREGO path to voltage at ADC input	—	0.35	—	mA/mV

4.1.6 Backup Supply Domain

Table 4.6. Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Backup supply voltage range	V_{BU_VIN}		1.8	—	3.8	V
PWRRES resistor	R_{PWRRES}	EMU_BUCTRL_PWRRES = RES0	3400	3900	4400	Ω
		EMU_BUCTRL_PWRRES = RES1	1450	1800	2150	Ω
		EMU_BUCTRL_PWRRES = RES2	1000	1350	1700	Ω
		EMU_BUCTRL_PWRRES = RES3	525	815	1100	Ω
Output impedance between BU_VIN and BU_VOUT [2]	R_{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	35	110	185	Ω
		EMU_BUCTRL_VOUTRES = MED	475	775	1075	Ω
		EMU_BUCTRL_VOUTRES = WEAK	5600	6500	7400	Ω
Supply current	I_{BU_VIN}	BU_VIN not powering backup domain	—	11	TBD	nA
		BU_VIN powering backup domain[1]	—	550	TBD	nA

Note:

1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.
2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

4.1.7.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.8. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{ACTIVE_DCM}	72 MHz HFRCO, CPU running Prime from flash	—	80	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	80	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	92	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	84	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	84	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	90	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	94	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	109	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	698	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode[1]	I_{ACTIVE_CCM}	72 MHz HFRCO, CPU running Prime from flash	—	84	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	84	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	95	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	91	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	92	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	104	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	113	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	142	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1264	—	µA/MHz

4.1.9 Brown Out Detector (BOD)

Table 4.11. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	1.62	V
		DVDD falling (EM0/EM1)	1.35	—	—	V
		DVDD falling (EM2/EM3)	TBD	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	18	—	mV
DVDD BOD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.8	V
		AVDD falling (EM0/EM1)	1.62	—	—	V
		AVDD falling (EM2/EM3)	TBD	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	20	—	mV
AVDD BOD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	—	300	—	µs

4.1.26 Ethernet (ETH)

MII Transmit Timing

Timing is specified with 3.0 V ≤ IOVDD ≤ 3.8 V, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.42. Ethernet MII Transmit Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX_CLK frequency	F_{TX_CLK}	Output slew rate set to 7	—	25	—	MHz
TX_CLK duty cycle	DC_{TX_CLK}		35	—	65	%
Output delay, TX_CLK to TXD[3:0], TX_EN, TX_ER	t_{OUT}		0	—	25	ns

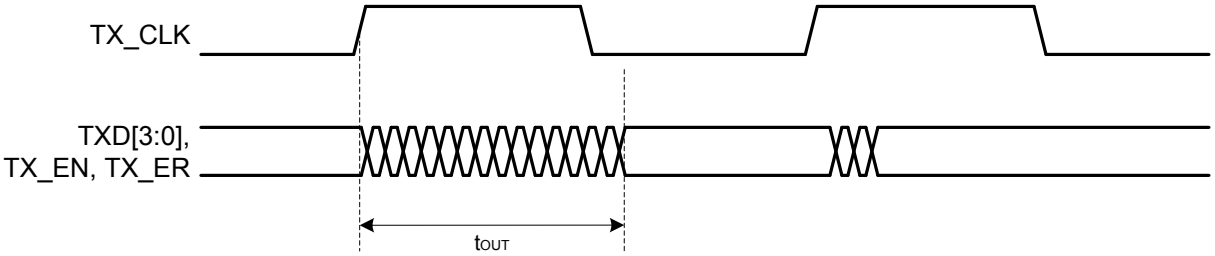

Figure 4.9. Ethernet MII Transmit Timing

SDIO SDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.48. SDIO SDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		0.99	4.68	—	ns
Clock fall time	t_F		0.90	3.64	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}		8	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}		1.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}		0	—	35	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}		0.8	—	—	ns

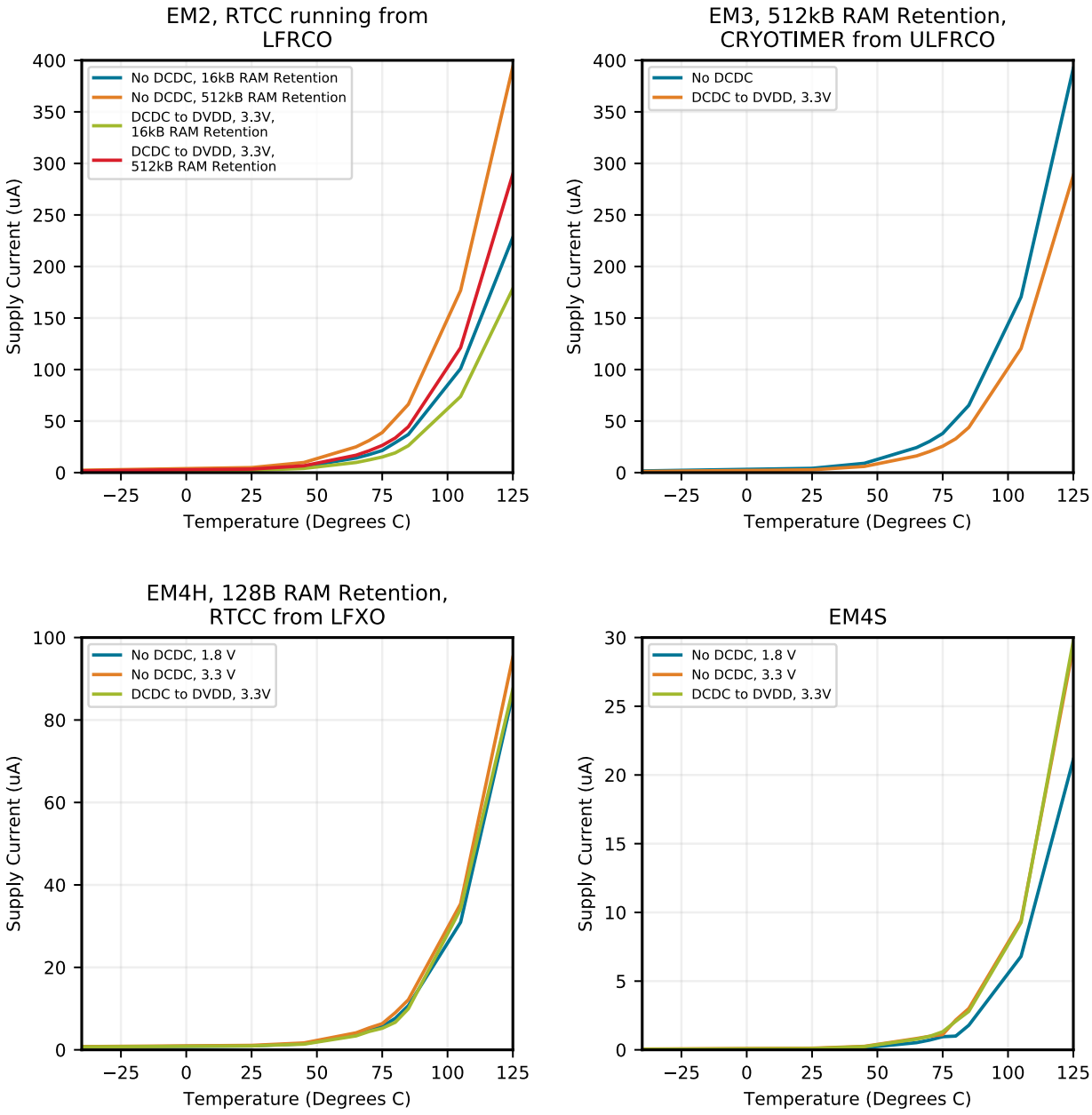

Figure 4.26. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
IOVDD1	F7 G7	Digital IO power supply 1.	VSS	F8 G8 G9 H6 H7 H8 H9 H10 H11 J6 J7 J8 J9 J10 J11 K8 K9 L8 L9	Ground
NC	F9	No Connect.	IOVDD0	F10 F11 G10 G11 K6 K7 K10 K11 L6 L7 L10 L11	Digital IO power supply 0.
PI5	F14	GPIO (5V)	PI4	F15	GPIO (5V)
PI3	F16	GPIO (5V)	PA5	G1	GPIO
PG6	G2	GPIO (5V)	PG5	G3	GPIO (5V)
PI2	G14	GPIO (5V)	PI1	G15	GPIO (5V)
PI0	G16	GPIO (5V)	PA6	H1	GPIO
PG8	H2	GPIO (5V)	PG7	H3	GPIO (5V)
PE5	H14	GPIO	PE6	H15	GPIO
PE7	H16	GPIO	PG11	J1	GPIO (5V)
PG10	J2	GPIO (5V)	PG9	J3	GPIO (5V)
PE3	J14	GPIO	PE4	J15	GPIO
DECOUPLE	J16	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PG14	K1	GPIO
PG13	K2	GPIO	PG12	K3	GPIO
PE1	K14	GPIO (5V)	PE2	K15	GPIO
DVDD	K16	Digital power supply.	PG15	L1	GPIO (5V)
PB15	L2	GPIO (5V)	PB0	L3	GPIO
PE0	L14	GPIO (5V)	PC7	L15	GPIO
VREGVDD	L16	Voltage regulator VDD input	PB1	M1	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD8	H8	GPIO	PD5	H9	GPIO
PD6	H10	GPIO	PD7	H11	GPIO
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF2	78	GPIO	VBUS	79	USB VBUS signal and auxiliary input to 5 V regulator.
PF12	80	GPIO	PF5	81	GPIO
PF6	84	GPIO	PF7	85	GPIO
PF8	86	GPIO	PF9	87	GPIO
PD9	88	GPIO	PD10	89	GPIO
PD11	90	GPIO	PD12	91	GPIO
PE8	92	GPIO	PE9	93	GPIO
PE10	94	GPIO	PE11	95	GPIO
PE12	96	GPIO	PE13	97	GPIO
PE14	98	GPIO	PE15	99	GPIO
PA15	100	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF3	79	GPIO	PF4	80	GPIO
PF5	81	GPIO	PF6	84	GPIO
PF7	85	GPIO	PF8	86	GPIO
PF9	87	GPIO	PD9	88	GPIO
PD10	89	GPIO	PD11	90	GPIO
PD12	91	GPIO	PE8	92	GPIO
PE9	93	GPIO	PE10	94	GPIO
PE11	95	GPIO	PE12	96	GPIO
PE13	97	GPIO	PE14	98	GPIO
PE15	99	GPIO	PA15	100	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA12	18	GPIO (5V)	PA13	19	GPIO (5V)
PA14	20	GPIO	RESETn	21	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	22	GPIO	PB12	23	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD8	35	GPIO	VREGVSS	36	Voltage regulator VSS
VREGSW	37	DCDC regulator switching node	VREGVDD	38	Voltage regulator VDD input
DVDD	39	Digital power supply.	DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	41	GPIO	PE5	42	GPIO
PE6	43	GPIO	PE7	44	GPIO
VREGI	45	Input to 5 V regulator.	VREGO	46	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PF10	47	GPIO (5V)	PF11	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.
PF12	53	GPIO	PF5	54	GPIO
PE8	56	GPIO	PE9	57	GPIO
PE10	58	GPIO	PE11	59	GPIO
PE12	60	GPIO	PE13	61	GPIO
PE14	62	GPIO	PE15	63	GPIO
PA15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO (5V)
PC9	42	GPIO (5V)	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD13		EBI_ARDY #1	TIM2_CDTI0 #1 TIM3_CC1 #6 WTIM0_CC1 #1	ETH_MDIO #1 US4_CTS #1 US5_CLK #1	ETM_TD1 #1
PI15				CAN1_TX #7 US3_CS #5	
PI14				CAN1_RX #7 US3_CLK #5	
PI13				CAN0_TX #7 US3_RX #5	
PI12				CAN0_RX #7 US3_TX #5	
PI10		EBI_A15 #2	TIM4_CC2 #3	US4_CTS #3	
PI7		EBI_A12 #2	TIM1_CC1 #7 TIM4_CC2 #2 WTIM3_CC1 #5	US4_RX #3	
PF15	BUSCY BUSDX		TIM1_CC2 #6 TIM4_CC2 #1 WTIM3_CC2 #7	US5_TX #2 I2C2_SDA #5	
PF12	BUSDY BUSCX	EBI_NANDREn #5	TIM4_CC2 #0 TIM1_CC3 #5 TIM5_CC0 #7 WTIM3_CC2 #6	US5_CS #2 I2C2_SCL #3 USB_ID	
PF4	BUSDY BUSCX LCD_SEG2	EBI_WEn #0 EBI_WEn #5	TIM4_CC1 #0 TIM0_CDTI1 #2 TIM1_CC2 #5 WTIM3_CC1 #6	US1_RTS #2 I2C2_SDA #3	PRS_CH1 #1
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BUSACMP1Y BUSACMP1X	EBI_NANDREn #4	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LETIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 U1_RTS #0 LEU0_RX #5 I2C2_SCL #1	LES_CH15 PRS_CH1 #2 ACMP3_O #1 DBG_SWO #1
PC14	VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSACMP1Y BUSACMP1X	EBI_NANDWEn #4	TIM0_CDTI1 #1 TIM1_CC1 #0 TIM1_CC3 #4 TIM5_CC0 #6 WTIM3_CC0 #3 LETIM0_OUT0 #5 PCNT0_S1IN #0	US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 U1_CTS #0 LEU0_TX #5 I2C2_SDA #1	LES_CH14 PRS_CH0 #2 ACMP3_O #2
PA2	BUSBY BUSAX LCD_SEG15	EBI_AD11 #0 EBI_DTEN #3	TIM0_CC2 #0 TIM3_CC2 #4	ETH_RMIIRXD0 #0 ETH_MIITXD2 #0 SDIO_DAT2 #1 US1_RX #6 US3_CLK #0 QSPI0_DQ0 #1	CMU_CLK0 #0 PRS_CH8 #1 ETM_TD0 #3
PG0	BUSACMP2Y BUSACMP2X	EBI_AD00 #2	TIM6_CC0 #0 TIM2_CDTI0 #3 WTIM0_CDTI1 #1 LETIM1_OUT0 #6	ETH_MIITXCLK #1 US3_TX #4 QSPI0_SCLK #2	CMU_CLK2 #3

Table 5.24. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP1X																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT0Y	BUSACMP1Y																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 10.1. TQFP100 Package Dimensions

Dimension	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.09	-	0.16
D	16.0 BSC		
E	16.0 BSC		
D1	14.0 BSC		
E1	14.0 BSC		
e	0.50 BSC		
L1	1 REF		
L	0.45	0.60	0.75
Θ	0	3.5	7
Θ1	0	-	-
Θ2	11	12	13
Θ3	11	12	13
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
aaa	0.2		
bbb	0.2		
ccc	0.08		
ddd	0.08		
eee	0.05		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 10.2. TQFP100 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
C1		15.4	
C2		15.4	
E		0.50 BSC	
X		0.30	
Y		1.50	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10.3 TQFP100 Package Marking

Figure 10.3. TQFP100 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

11. TQFP64 Package Specifications

11.1 TQFP64 Package Dimensions

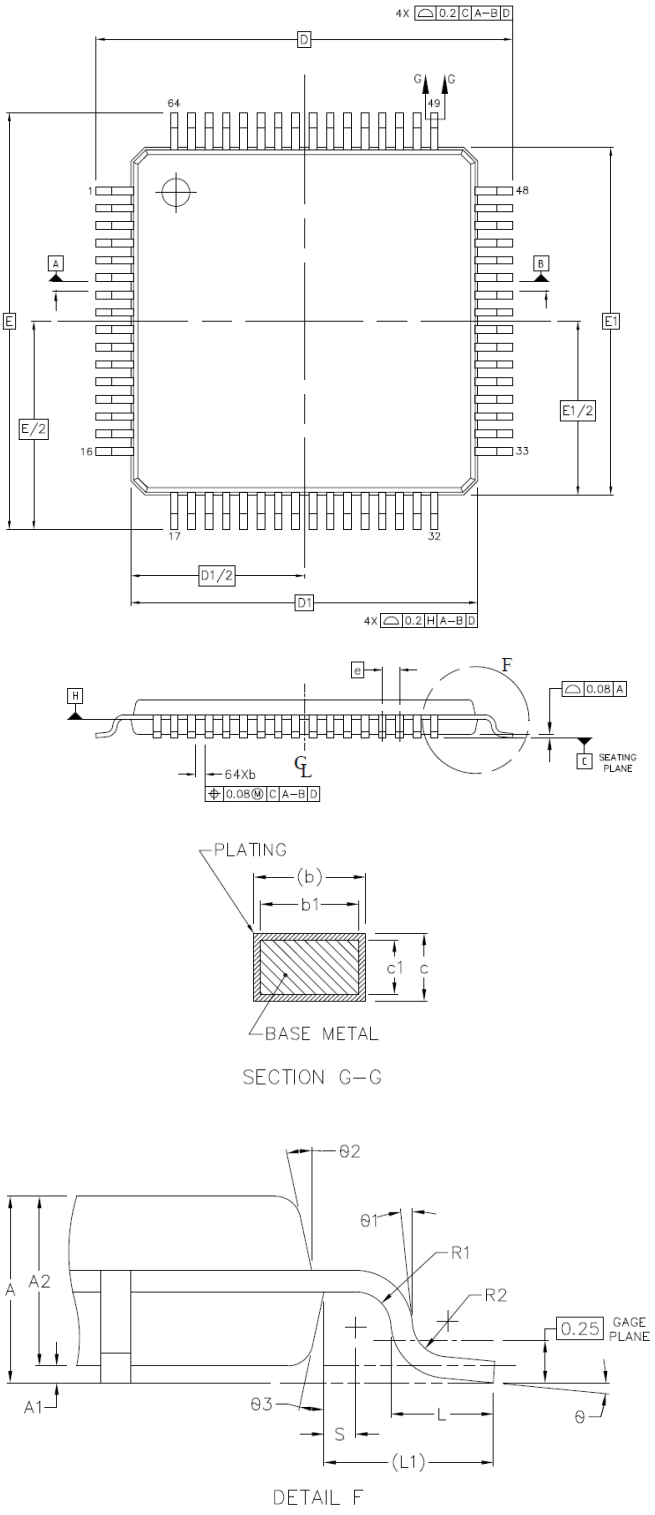

Figure 11.1. TQFP64 Package Drawing