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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b420f2048gm64-b

3.11 Memory Map

The EFM32GG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.
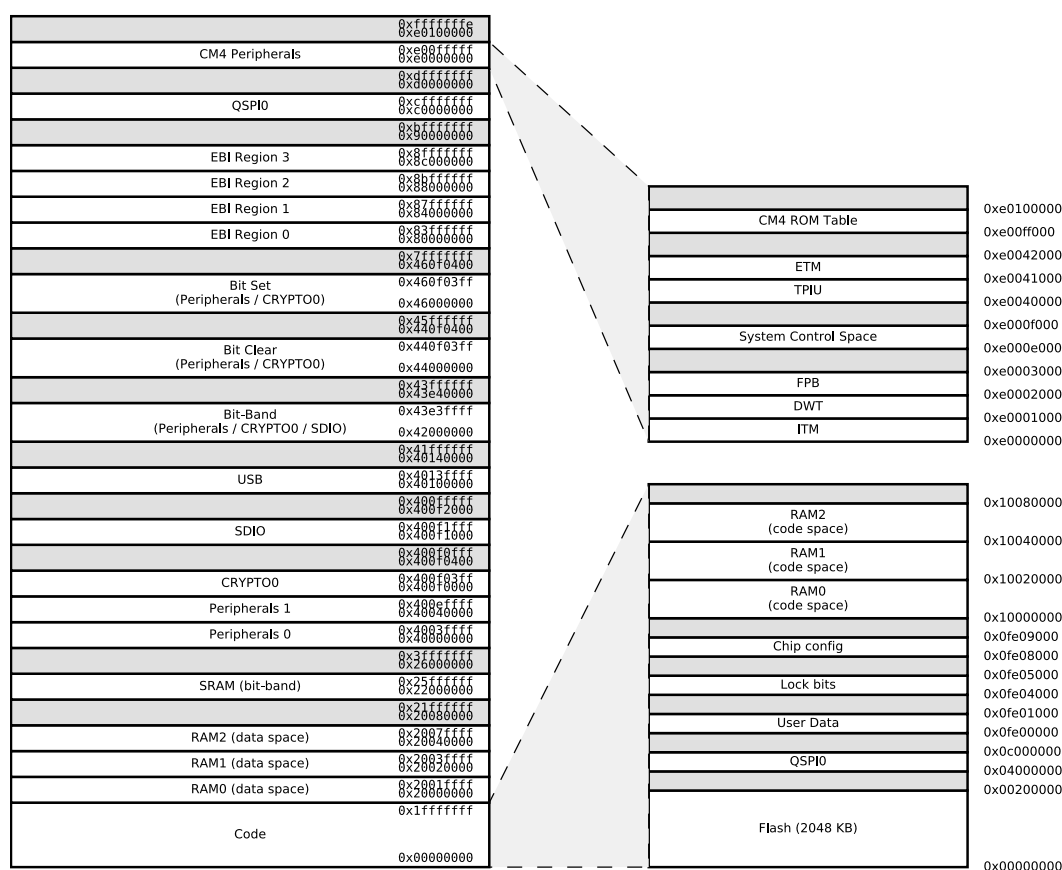

Figure 3.2. EFM32GG11 Memory Map — Core Peripherals and Code Space

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min} + I_{LOAD} * R_{BYP\_max}$.

2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.

3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.

4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).

5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.

6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - (THETA$_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and THETA$_{JA}$.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN64 Package	THETA$_{JA\_QFN64}$	4-Layer PCB, Air velocity = 0 m/s	—	17.8	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	15.4	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	13.8	—	°C/W
Thermal resistance, TQFP64 Package	THETA$_{JA\_TQFP64}$	4-Layer PCB, Air velocity = 0 m/s	—	33.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	32.1	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	30.1	—	°C/W
Thermal resistance, TQFP100 Package	THETA$_{JA\_TQFP100}$	4-Layer PCB, Air velocity = 0 m/s	—	44.1	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	37.7	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	35.5	—	°C/W
Thermal resistance, BGA112 Package	THETA$_{JA\_BGA112}$	4-Layer PCB, Air velocity = 0 m/s	—	42.0	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	37.0	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	35.3	—	°C/W
Thermal resistance, BGA120 Package	THETA$_{JA\_BGA120}$	4-Layer PCB, Air velocity = 0 m/s	—	47.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	41.8	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	39.6	—	°C/W
Thermal resistance, BGA152 Package	THETA$_{JA\_BGA152}$	4-Layer PCB, Air velocity = 0 m/s	—	35.7	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	31.0	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	29.5	—	°C/W
Thermal resistance, BGA192 Package	THETA$_{JA\_BGA192}$	4-Layer PCB, Air velocity = 0 m/s	—	47.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	41.8	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	39.6	—	°C/W

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 µF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.8	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC accuracy	ACC_{DC}	Low Noise (LN) mode, 1.8 V target output	TBD	—	TBD	V
Regulation window[4]	WIN_{REG}	Low Power (LP) mode, LPCMPBIASEMxx[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 µA	TBD	—	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	TBD	—	TBD	V
Steady-state output ripple	V_R		—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	25	TBD	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

4.1.10.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.13. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}	No clock doubling	4	—	50	MHz
		Clock doubler enabled	TBD	—	TBD	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	50 MHz crystal	—	—	50	Ω
		24 MHz crystal	—	—	150	Ω
		4 MHz crystal	—	—	180	Ω
Nominal on-chip tuning cap range[1]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	8.7	—	51.7	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.084	—	pF
Startup time	t_{HFXO}	50 MHz crystal, ESR = 50 Ohm, C_L = 8 pF	—	350	—	µs
		24 MHz crystal, ESR = 150 Ohm, C_L = 6 pF	—	700	—	µs
		4 MHz crystal, ESR = 180 Ohm, C_L = 18 pF	—	3	—	ms
Current consumption after startup	I_{HFXO}	50 MHz crystal	—	880	—	µA
		24 MHz crystal	—	420	—	µA
		4 MHz crystal	—	80	—	µA

Note:

1. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

SPI Slave Timing

Table 4.35. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		$6 * t_{HFPERCLK}$	—	—	ns
SCLK high time[1] [3] [2]	t_{SCLK_HI}		$2.5 * t_{HFPERCLK}$	—	—	ns
SCLK low time[1] [3] [2]	t_{SCLK_LO}		$2.5 * t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [3]	$t_{CS\_ACT\_MI}$		24	—	69	ns
CS disable to MISO [1] [3]	$t_{CS\_DIS\_MI}$		19	—	175	ns
MOSI setup time [1] [3]	t_{SU_MO}		7	—	—	ns
MOSI hold time [1] [3] [2]	t_{H_MO}		6	—	—	ns
SCLK to MISO [1] [3] [2]	t_{SCLK_MI}		$16 + 1.5 * t_{HFPERCLK}$	—	$43 + 2.5 * t_{HFPERCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).
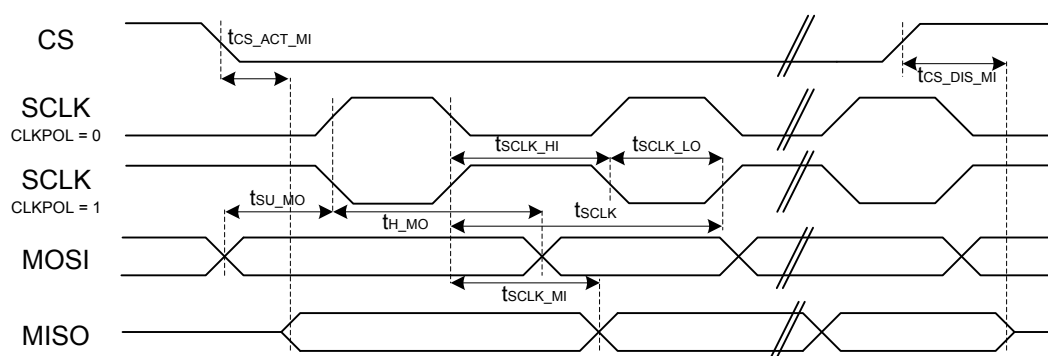
Figure 4.2. SPI Slave Timing Diagram

EBI Address Latch Enable Output Timing

Timing applies to multiplexed addressing modes D8A24ALE and D16A16ALE for both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.37. EBI Address Latch Enable Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_ALE edge to EBI_AD invalid[1][2]	t_{OH_ALEn}	IOVDD ≥ 1.62 V	$-22 + (ADDRHOLD * t_{HFCORECLK})$	—	—	ns
		IOVDD ≥ 3.0 V	$-11 + (ADDRHOLD * t_{HFCORECLK})$	—	—	ns
Output setup time, from EBI_AD valid to leading EBI_ALE edge	t_{OSU_ALEn}	IOVDD ≥ 1.62 V	-12	—	—	ns
		IOVDD ≥ 3.0 V	-9	—	—	ns
EBI_ALEn pulse width[1]	t_{WIDTH_ALEn}	IOVDD ≥ 1.62 V	$-4 + ((ADDRSETUP + 1) * t_{HFCORECLK})$	—	—	ns
		IOVDD ≥ 3.0 V	$-3 + ((ADDRSETUP + 1) * t_{HFCORECLK})$	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALEn can be moved to the left by setting HALFALE=1. This decreases the length of t_{WIDTH_ALEn} and increases the length of t_{OSU_ALEn} by $t_{HFCORECLK} - 1/2 * t_{HFCLKNODIV}$.
2. The figure shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

SDIO DDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 30 pF on all pins.

Table 4.49. SDIO DS Mode Timing (Location 0)

| Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.69	6.52	—	ns
Clock fall time	t_F		1.42	4.96	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		1.8	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		0.8	—	—	ns
Input setup time, DAT[0:3] valid to SD_CLK	t_{ISU2X}		6	—	—	ns
Input hold time, SD_CLK to DAT[0:3] change	t_{IH2X}		1.5	—	—	ns
Output delay time, SD_CLK to DAT[0:3] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:3] change	t_{OH2X}		0.8	—	—	ns
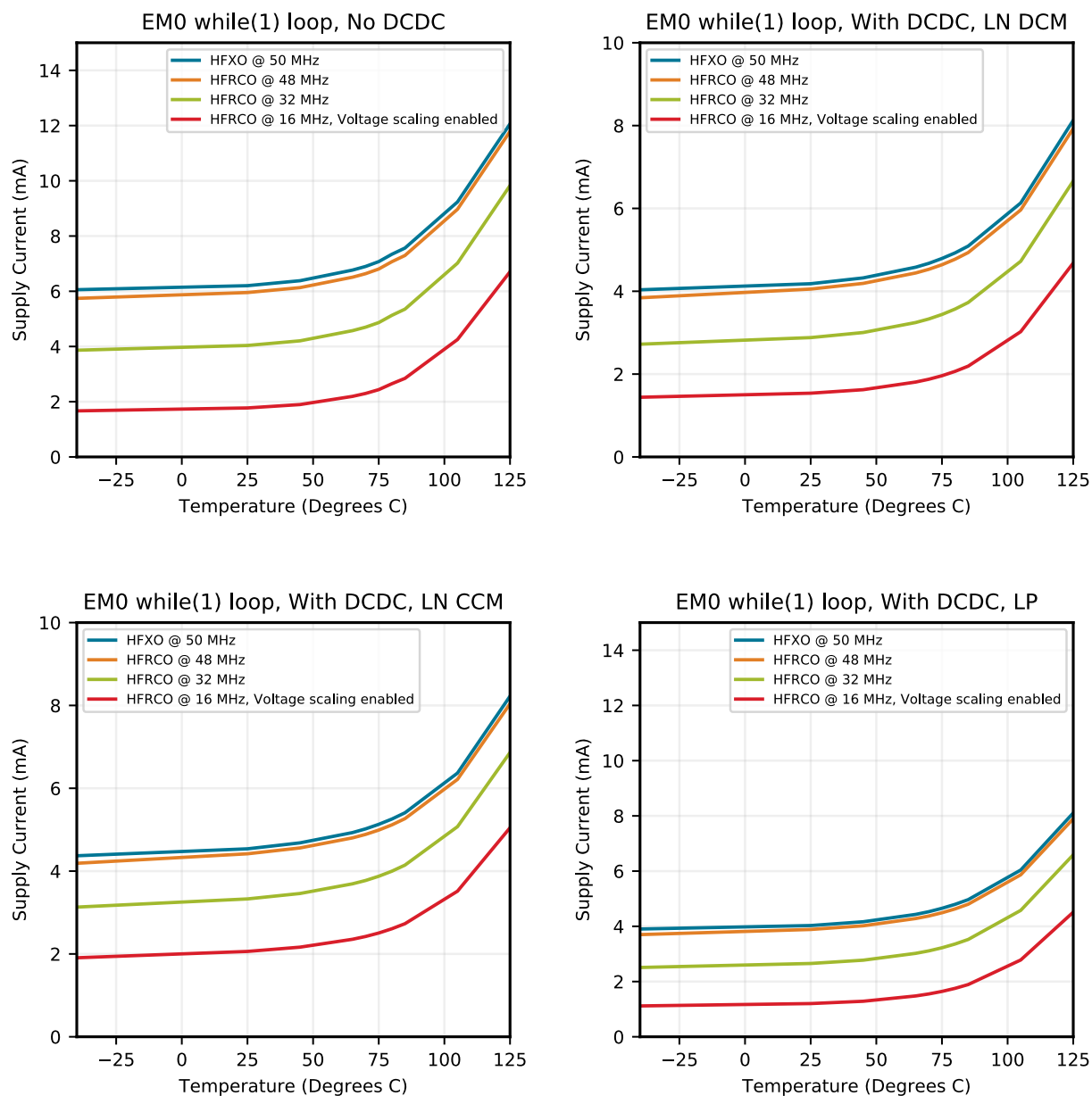
Figure 4.24. EM0 Active Mode Typical Supply Current vs. Temperature

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.
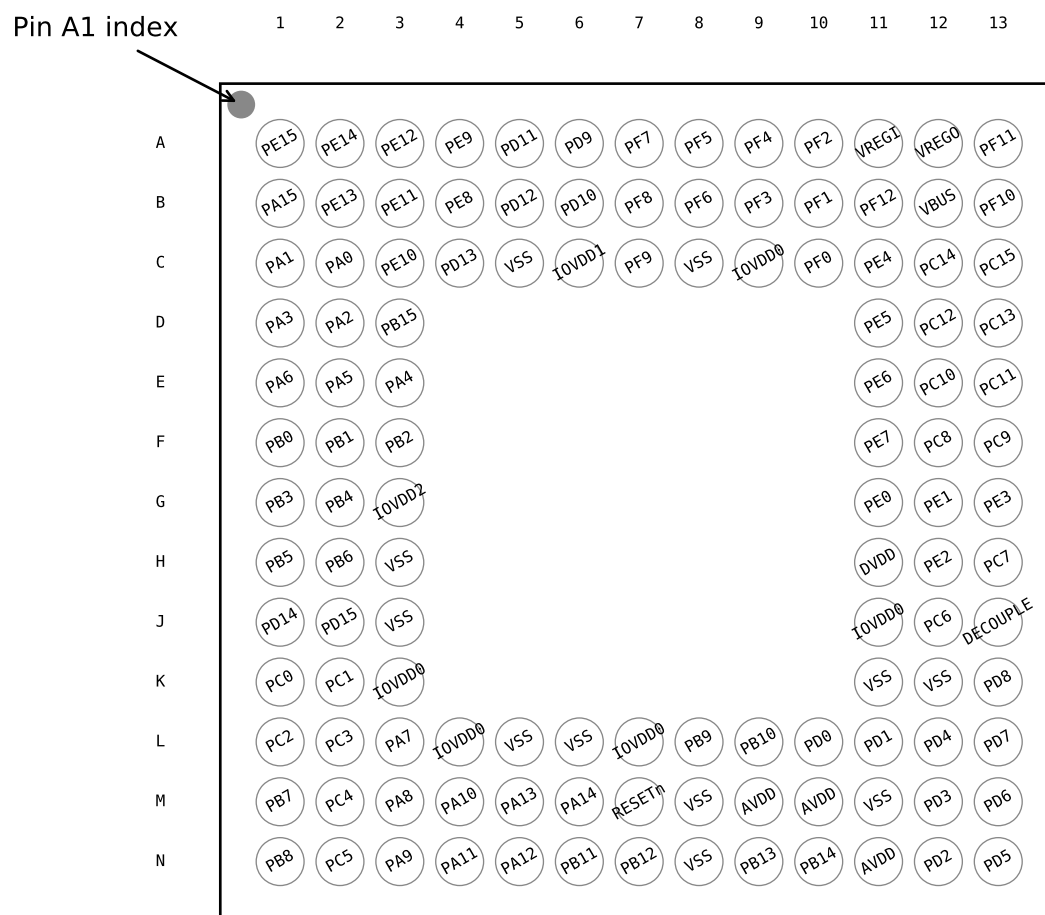
5.5 EFM32GG11B4xx in BGA120 Device Pinout

Figure 5.5. EFM32GG11B4xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.5. EFM32GG11B4xx in BGA120 Device Pinout

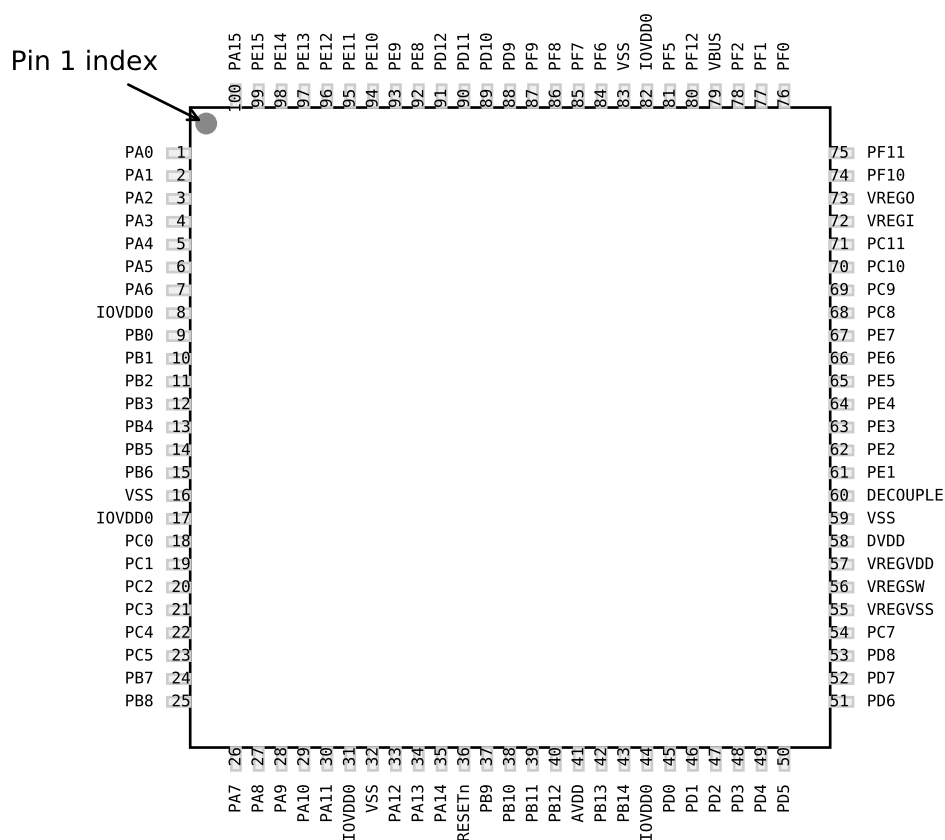| Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF4	A9	GPIO	PF2	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs

5.8 EFM32GG11B8xx in QFP100 Device Pinout

Figure 5.8. EFM32GG11B8xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.8. EFM32GG11B8xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 59 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB9	37	GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	45	GPIO (5V)	PD1	46	GPIO
PD2	47	GPIO (5V)	PD3	48	GPIO
PD4	49	GPIO	PD5	50	GPIO
PD6	51	GPIO	PD7	52	GPIO
PD8	53	GPIO	PC7	54	GPIO
VREGVSS	55	Voltage regulator VSS	VREGSW	56	DCDC regulator switching node
VREGVDD	57	Voltage regulator VDD input	DVDD	58	Digital power supply.
DECOUPLE	60	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE1	61	GPIO (5V)
PE2	62	GPIO	PE3	63	GPIO
PE4	64	GPIO	PE5	65	GPIO
PE6	66	GPIO	PE7	67	GPIO
PC8	68	GPIO (5V)	PC9	69	GPIO (5V)
PC10	70	GPIO (5V)	PC11	71	GPIO (5V)
VREGI	72	Input to 5 V regulator.	VREGO	73	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PF10	74	GPIO (5V)	PF11	75	GPIO (5V)
PF0	76	GPIO (5V)	PF1	77	GPIO (5V)

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF14	BUSDY BUSCX		TIM1_CC1 #6 TIM4_CC1 #1 TIM5_CC2 #7 WTIM3_CC1 #7	I2C2_SCL #4	
PF11	BUSCY BUSDX	EBI_NANDWEn #5	TIM5_CC2 #6 WTIM3_CC2 #3 PCNT2_S1IN #3	US5_CTS #2 U1_RX #1 I2C2_SCL #2 USB_DP	
PF10	BUSDY BUSCX	EBI_ARDY #5	TIM5_CC1 #6 WTIM3_CC1 #3 PCNT2_S0IN #3	US5_RTS #2 U1_TX #1 I2C2_SDA #2 USB_DM	
PF0	BUSDY BUSCX	EBI_A24 #1	TIM0_CC0 #4 WTIM0_CC1 #4 LE- TIM0_OUT0 #2	US2_TX #5 CAN0_RX #1 US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	PRS_CH15 #2 ACMP3_O #0 DBG_SWCLKTCK BOOT_TX
PA0	BUSBY BUSAX LCD_SEG13	EBI_AD09 #0 EBI_CSTFT #3	TIM0_CC0 #0 TIM0_CC1 #7 TIM3_CC0 #4 PCNT0_S0IN #4	ETH_RMIITXEN #0 ETH_MIITXCLK #0 SDIO_DAT0 #1 US1_RX #5 US3_TX #0 QSPI0_CS0 #1 LEU0_RX #4 I2C0_SDA #0	CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
PD11	LCD_SEG30	EBI_CS2 #0 EBI_HSNC #1	TIM4_CC0 #6 WTIM3_CC2 #0	ETH_RMIICRSDV #1 SDIO_DAT5 #0 QSPI0_DQ2 #0 ETH_MIIRXD3 #2 US4_CLK #1	
PD10	LCD_SEG29	EBI_CS1 #0 EBI_VSNC #1	TIM4_CC2 #5 WTIM3_CC1 #0	ETH_RMIIREFCLK #1 SDIO_DAT6 #0 QSPI0_DQ1 #0 ETH_MIIRXD2 #2 US4_RX #1	CMU_CLK2 #5 CMU_CLKI0 #5
PD9	LCD_SEG28	EBI_CS0 #0 EBI_DTEN #1	TIM4_CC1 #5 WTIM3_CC0 #0	ETH_RMIIRXD0 #1 SDIO_DAT7 #0 QSPI0_DQ0 #0 ETH_MIIRXD1 #2 US4_TX #1	
PF9	BUSCY BUSDX LCD_SEG27	EBI_REn #4 EBI_BL1 #1	TIM4_CC0 #5	ETH_RMIIRXD1 #1 US2_CS #4 QSPI0_DQS #0 ETH_MIIRXD0 #2 ETH_TSUTMRTOG #3 SDIO_WP #0 U0_RTS #0 U1_CTS #1	ETM_TD0 #1
PF8	BUSDY BUSCX LCD_SEG26	EBI_WEn #4 EBI_BL0 #1	TIM0_CC2 #1 TIM4_CC2 #4	ETH_RMIITXEN #1 US2_CLK #4 QSPI0_CS1 #0 ETH_MIIRXDV #2 ETH_TSUEXTCLK #3 SDIO_CD #0 U0_CTS #0 U1_RTS #1	ETM_TCLK #1 GPIO_EM4WU8

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
BU_STAT	0: PE3		Backup Power Domain status, whether or not the system is in backup mode.
BU_VIN	0: PD8		Battery input for Backup Power Domain.
BU_VOUT	0: PE2		Power output for Backup Power Domain.
CAN0_RX	0: PC0 1: PF0 2: PD0 3: PB9	4: PG8 5: PD14 6: PE0 7: PI12	CAN0 RX.
CAN0_TX	0: PC1 1: PF2 2: PD1 3: PB10	4: PG9 5: PD15 6: PE1 7: PI13	CAN0 TX.
CAN1_RX	0: PC2 1: PF1 2: PD3 3: PC9	4: PC12 5: PA12 6: PG10 7: PI14	CAN1 RX.
CAN1_TX	0: PC3 1: PF3 2: PD4 3: PC10	4: PC11 5: PA13 6: PG11 7: PI15	CAN1 TX.
CMU_CLK0	0: PA2 1: PC12 2: PD7 3: PG2	4: PF2 5: PA12	Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA1 1: PD8 2: PE12 3: PG1	4: PF3 5: PB11	Clock Management Unit, clock output number 1.
CMU_CLK2	0: PA0 1: PA3 2: PD6 3: PG0	4: PA3 5: PD10	Clock Management Unit, clock output number 2.
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	4: PE1 5: PD10 6: PE12 7: PB11	Clock Management Unit, clock input number 0.
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A10	0: PE3 1: PD6 2: PC10 3: PB10		External Bus Interface (EBI) address output pin 10.
EBI_A11	0: PE4 1: PD7 2: PI6 3: PB11		External Bus Interface (EBI) address output pin 11.
EBI_A12	0: PE5 1: PD8 2: PI7 3: PB12		External Bus Interface (EBI) address output pin 12.
EBI_A13	0: PE6 1: PC7 2: PI8 3: PD0		External Bus Interface (EBI) address output pin 13.
EBI_A14	0: PE7 1: PE2 2: PI9 3: PD1		External Bus Interface (EBI) address output pin 14.
EBI_A15	0: PC8 1: PE3 2: PI10 3: PD2		External Bus Interface (EBI) address output pin 15.
EBI_A16	0: PB0 1: PE4 2: PH4 3: PD3		External Bus Interface (EBI) address output pin 16.
EBI_A17	0: PB1 1: PE5 2: PH5 3: PD4		External Bus Interface (EBI) address output pin 17.
EBI_A18	0: PB2 1: PE6 2: PH6 3: PD5		External Bus Interface (EBI) address output pin 18.
EBI_A19	0: PB3 1: PE7 2: PH7 3: PD6		External Bus Interface (EBI) address output pin 19.
EBI_A20	0: PB4 1: PC8 2: PH8 3: PD7		External Bus Interface (EBI) address output pin 20.
EBI_A21	0: PB5 1: PC9 2: PH9 3: PC7		External Bus Interface (EBI) address output pin 21.
EBI_A22	0: PB6 1: PC10 2: PH10 3: PE4		External Bus Interface (EBI) address output pin 22.

6. BGA192 Package Specifications
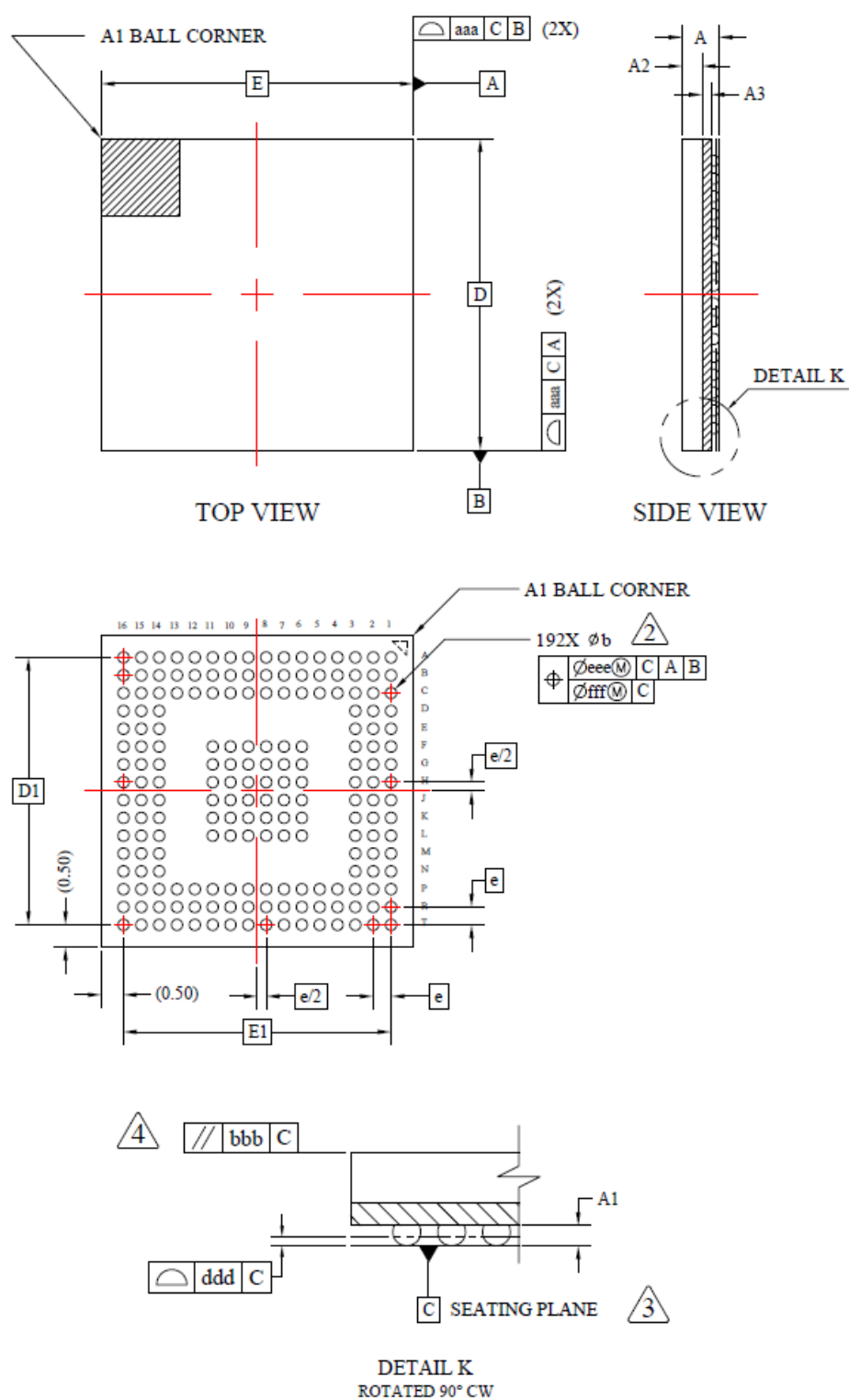
6.1 BGA192 Package Dimensions

Figure 6.1. BGA192 Package Drawing

Table 6.1. BGA192 Package Dimensions

Dimension	Min	Typ	Max
A	0.77	0.83	0.89
A1	0.13	0.18	0.23
A3	0.16	0.20	0.24
A2		0.45 REF	
D		7.00 BSC	
e		0.40 BSC	
E		7.00 BSC	
D1		6.00 BSC	
E1		6.00 BSC	
b	0.20	0.25	0.30
aaa		0.10	
bbb		0.10	
ddd		0.08	
eee		0.15	
fff		0.05	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

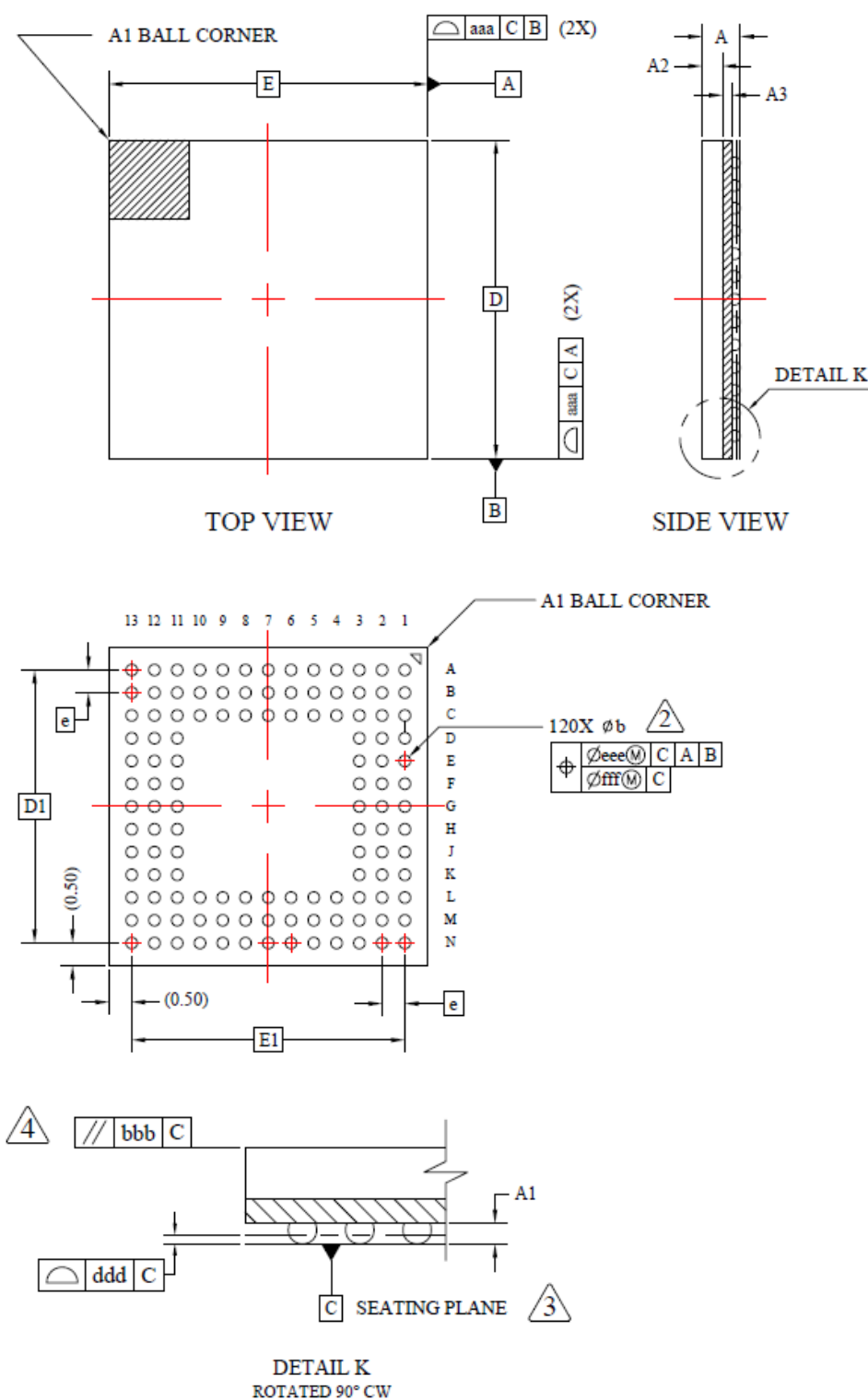# 8. BGA120 Package Specifications

8.1 BGA120 Package Dimensions

Figure 8.1. BGA120 Package Drawing

Table 9.1. BGA112 Package Dimensions

Dimension	Min	Typ	Max
A	-	-	1.30
A1	0.55	0.60	0.65
A2	0.21 BSC		
A3	0.30	0.35	0.40
d	0.43	0.48	0.53
D	10.00 BSC		
D1	8.00 BSC		
E	10.00 BSC		
E1	8.00 BSC		
e1	0.80 BSC		
e2	0.80 BSC		
L1	1.00 REF		
L2	1.00 REF		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
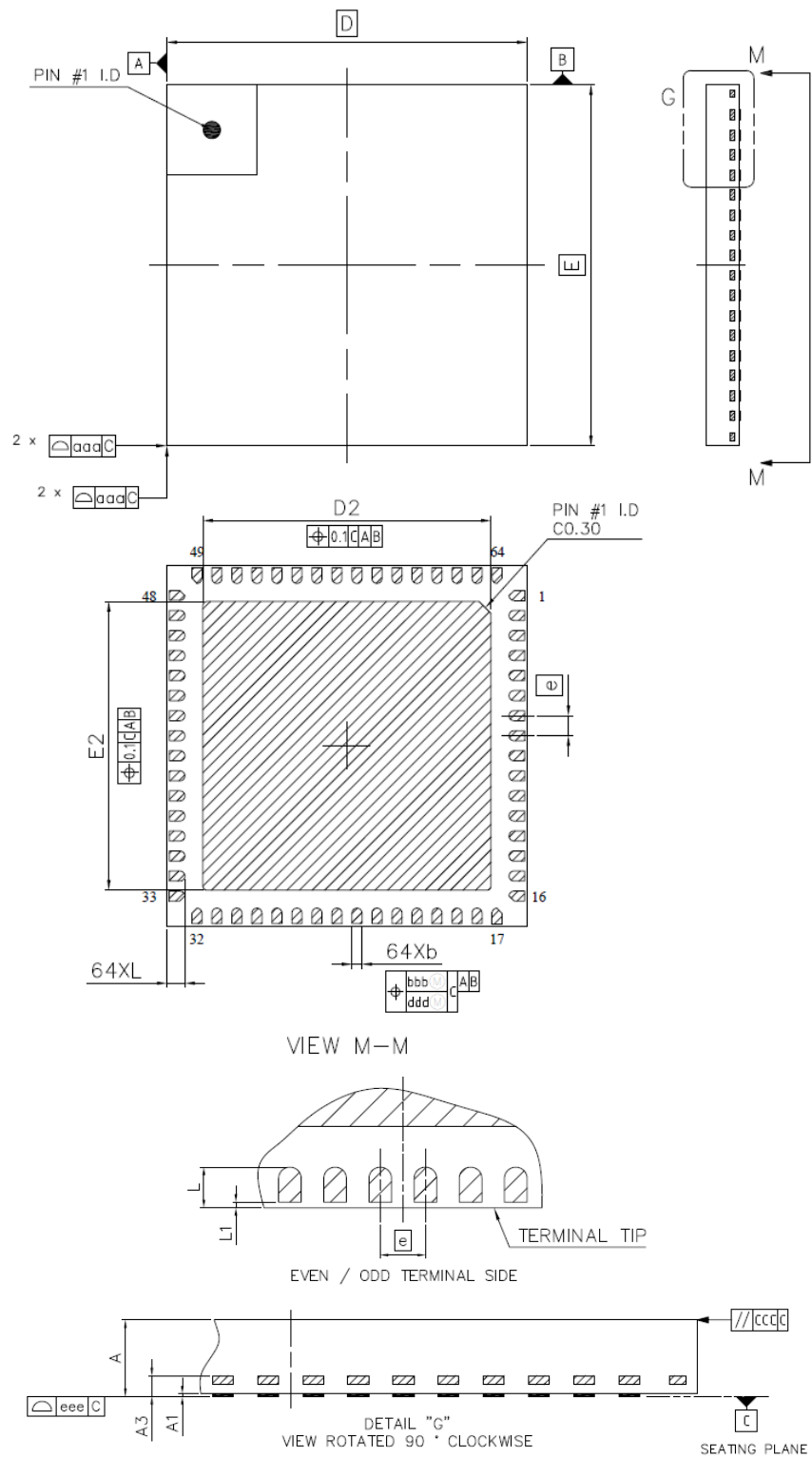
12. QFN64 Package Specifications

12.1 QFN64 Package Dimensions

Figure 12.1.   QFN64 Package Drawing