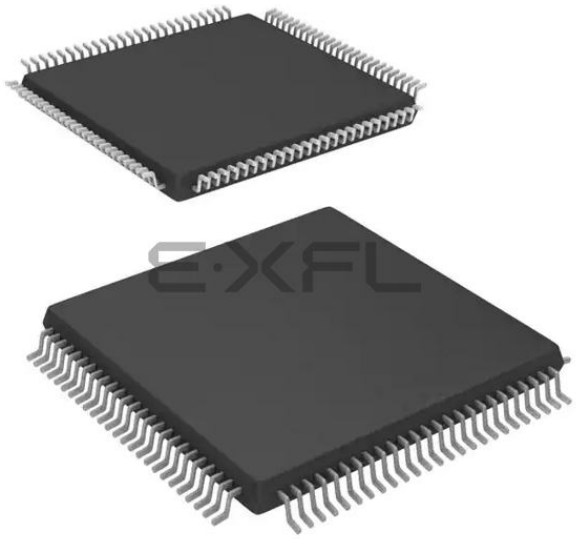
# Silicon Labs - EFM32GG11B420F2048GQ100-BR Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 83 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.8V |
| Data Converters | A/D 16x12b SAR; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b420f2048gq100-br |

### 4.1.5 5V Regulator

$V_{VREGI}$ = 5 V, $V_{VREGO}$ = 3.3 V, $C_{VREGI}$ = 10 µF, $C_{VREGO}$ = 4.7 µF, unless otherwise specified.

**Table 4.5. 5V Regulator**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VREGI or VBUS input voltage range | $V_{VREGI}$ | Regulating output | 2.7 | — | 5.5 | V |
| | | Bypass mode enabled | 2.7 | — | 3.8 | V |
| VREGO output voltage | $V_{VREGO}$ | Regulating output, 3.3 V setting | 3.1 | 3.3 | 3.5 | V |
| | | EM4S open-loop output, $I_{OUT}$ < 100 µA | 1.8 | — | 3.8 | V |
| Voltage output step size | $V_{VREGO\_SS}$ | | — | 0.1 | — | V |
| Resistance in Bypass Mode | $R_{BYP}$ | Bypass mode enabled | — | 1.2 | TBD | Ω |
| Output current | $I_{OUT}$ | EM0 or EM1, $V_{VREGI}$ > $V_{VREGO}$ + 0.6 V | — | — | 200 | mA |
| | | EM0 or EM1, $V_{VREGI}$ > $V_{VREGO}$ + 0.3 V | — | — | 100 | mA |
| | | EM2, EM3, or EM4H, $V_{VREGI}$ > $V_{VREGO}$ + 0.6 V | — | — | 2 | mA |
| | | EM2, EM3, or EM4H, $V_{VREGI}$ > $V_{VREGO}$ + 0.3 V | — | — | 0.5 | mA |
| | | EM4S | — | — | 20 | µA |
| Load regulation | $LR_{VREGO}$ | EM0 or EM1 | — | 0.10 | — | mV/mA |
| | | EM2, EM3, or EM4H | — | 2.5 | — | mV/mA |
| DC power supply rejection | $PSR_{DC}$ | | — | 40 | — | dB |
| VREGI or VBUS bypass capacitance | $C_{VREGI}$ | | — | 10 | — | µF |
| VREGO bypass capacitance | $C_{VREGO}$ | | 1 | 4.7 | 10 | µF |
| Supply current consumption | $I_{VREGI}$ | EM0 or EM1, No load | — | 29 | — | µA |
| | | EM2, EM3, or EM4H, No load | — | 270 | — | nA |
| | | EM4S, No load | — | 70 | — | nA |
| VREGI and VBUS detection high threshold | $V_{DET\_H}$ | | TBD | 1.18 | — | V |
| VREGI and VBUS detection low threshold | $V_{DET\_L}$ | | — | 1.12 | TBD | V |
| Current monitor transfer ratio | $IMON_{XF}$ | Translation of current through VREGO path to voltage at ADC input | — | 0.35 | — | mA/mV |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM4H mode, with voltage scaling enabled | $I_{EM4H\_VS}$ | 128 byte RAM retention, RTCC running from LFXO | — | 0.94 | — | µA |
| | | 128 byte RAM retention, CRYOTIMER running from ULFRCO | — | 0.62 | — | µA |
| | | 128 byte RAM retention, no RTCC | — | 0.62 | — | µA |
| Current consumption in EM4S mode | $I_{EM4S}$ | No RAM retention, no RTCC | — | 0.13 | — | µA |
| Current consumption of peripheral power domain 1, with voltage scaling enabled, DCDC in LP mode[3] | $I_{PD1\_VS}$ | Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[4] | — | 0.68 | — | µA |
| Current consumption of peripheral power domain 2, with voltage scaling enabled, DCDC in LP mode[3] | $I_{PD2\_VS}$ | Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[4] | — | 0.28 | — | µA |

**Note:**

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

### 4.1.12 General-Purpose I/O (GPIO)

**Table 4.20. General-Purpose I/O (GPIO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | GPIO pins | — | — | IOVDD*0.3 | V |
| Input high voltage | $V_{IH}$ | GPIO pins | IOVDD*0.7 | — | — | V |
| Output high voltage relative to IOVDD | $V_{OH}$ | Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK | IOVDD*0.8 | — | — | V |
| | | Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK | IOVDD*0.6 | — | — | V |
| | | Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG | IOVDD*0.8 | — | — | V |
| | | Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG | IOVDD*0.6 | — | — | V |
| Output low voltage relative to IOVDD | $V_{OL}$ | Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK | — | — | IOVDD*0.2 | V |
| | | Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK | — | — | IOVDD*0.4 | V |
| | | Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG | — | — | IOVDD*0.2 | V |
| | | Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG | — | — | IOVDD*0.4 | V |
| Input leakage current | $I_{IOLEAK}$ | All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C | — | 0.1 | TBD | nA |
| | | LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C | — | 0.1 | TBD | nA |
| | | All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C | — | — | TBD | nA |
| | | LFXO Pins, GPIO ≤ IOVDD, T > 85 °C | — | — | TBD | nA |
| Input leakage current on 5VTOL pads above IOVDD | $I_{5VTOLLEAK}$ | IOVDD < GPIO ≤ IOVDD + 2 V | — | 3.3 | TBD | µA |
| I/O pin pull-up/pull-down resistor | $R_{PUD}$ | | TBD | 40 | TBD | kΩ |
| Pulse width of pulses removed by the glitch suppression filter | $t_{IOGLITCH}$ | | 15 | 25 | 35 | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

### 4.1.24 USART SPI

#### SPI Master Timing

**Table 4.34. SPI Master Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period [1] [3] [2] | $t_{SCLK}$ | All USARTs except USART2 | 2 * $t_{HFPERCLK}$ | — | — | ns |
| | | USART2 | 2 * $t_{HFPERBCLK}$ | — | — | ns |
| CS to MOSI [1] [3] | $t_{CS\_MO}$ | USART2, location 4, IOVDD = 1.8 V | -3.2 | — | 6.8 | ns |
| | | USART2, location 4, IOVDD = 3.0 V | -2.3 | — | 6.0 | ns |
| | | USART2, location 5, IOVDD = 1.8 V | -8.1 | — | 6.3 | ns |
| | | USART2, location 5, IOVDD = 3.0 V | -7.3 | — | 4.4 | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | -15 | — | 13 | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | -13 | — | 11 | ns |
| SCLK to MOSI [1] [3] | $t_{SCLK\_MO}$ | USART2, location 4, IOVDD = 1.8 V | -0.3 | — | 9.2 | ns |
| | | USART2, location 4, IOVDD = 3.0 V | -0.3 | — | 8.6 | ns |
| | | USART2, location 5, IOVDD = 1.8 V | -3.6 | — | 5.0 | ns |
| | | USART2, location 5, IOVDD = 3.0 V | -3.4 | — | 3.2 | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | -10 | — | 11 | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | -9 | — | 11 | ns |
| MISO setup time [1] [3] | $t_{SU\_MI}$ | USART2, location 4, IOVDD = 1.8 V | 39.7 | — | — | ns |
| | | USART2, location 4, IOVDD = 3.0 V | 22.4 | — | — | ns |
| | | USART2, location 5, IOVDD = 1.8 V | 49.2 | — | — | ns |
| | | USART2, location 5, IOVDD = 3.0 V | 30.0 | — | — | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | 55 | — | — | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | 36 | — | — | ns |

### RMII Receive Timing

Timing is specified with 3.0 V ≤ IOVDD ≤ 3.8 V, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

**Table 4.45. Ethernet RMII Receive Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| REF_CLK frequency | $F_{REF\_CLK}$ | Output slew rate set to 7 | — | 50 | — | MHz |
| REF_CLK duty cycle | $DC_{REF\_CLK}$ | | 35 | — | 65 | % |
| Setup time, RXD[1:0], CRS_DV, RX_ER valid to REF_CLK | $t_{SU}$ | | 4 | — | — | ns |
| Hold time, REF_CLK to RXD[1:0], CRS_DV, RX_ER change | $t_{HD}$ | | 2 | — | — | ns |

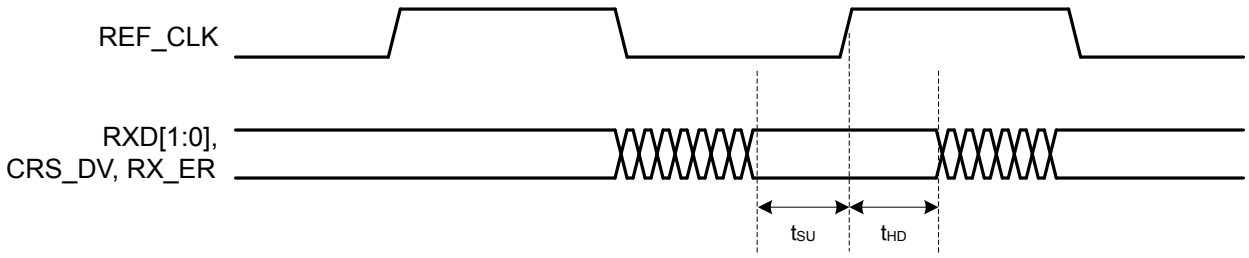


**Figure 4.12. Ethernet RMII Receive Timing**

# 5. Pin Definitions

## 5.1 EFM32GG11B8xx in BGA192 Device Pinout

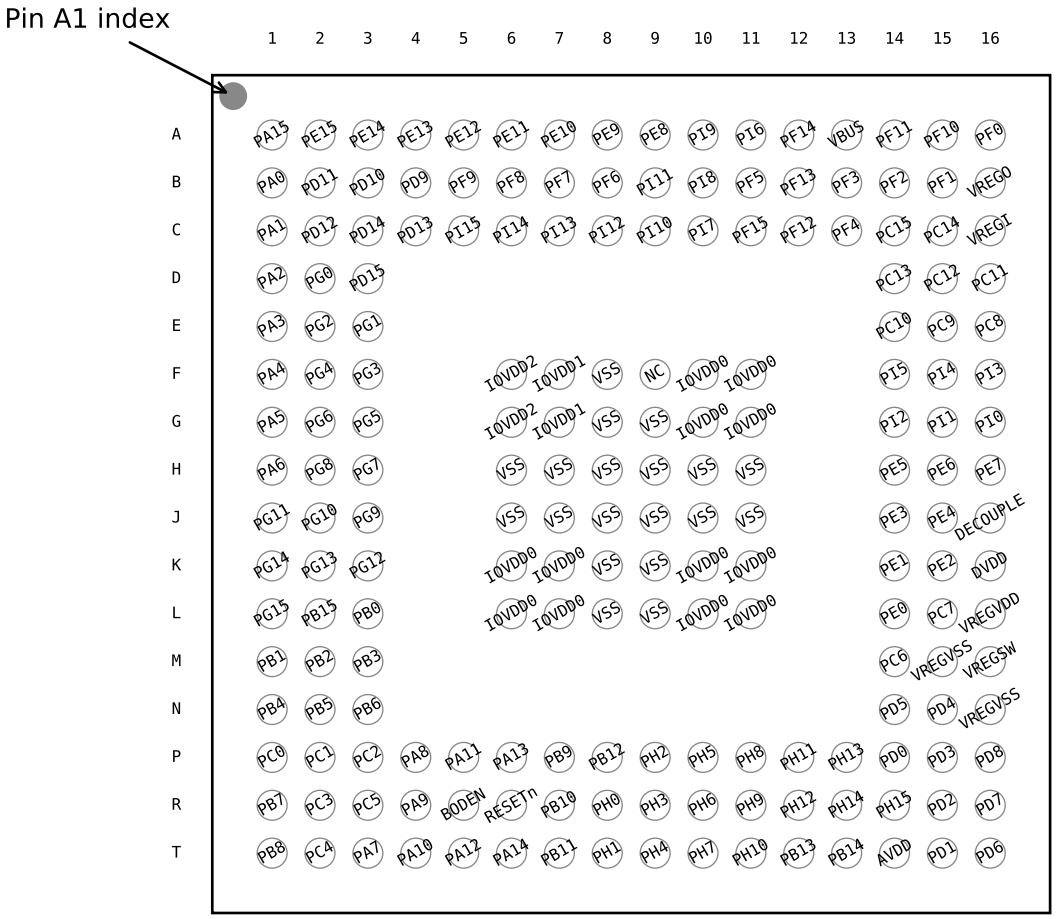


**Figure 5.1. EFM32GG11B8xx in BGA192 Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

**Table 5.1. EFM32GG11B8xx in BGA192 Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PA15 | A1 | GPIO | PE15 | A2 | GPIO |
| PE14 | A3 | GPIO | PE13 | A4 | GPIO |
| PE12 | A5 | GPIO | PE11 | A6 | GPIO |
| PE10 | A7 | GPIO | PE9 | A8 | GPIO |
| PE8 | A9 | GPIO | PI9 | A10 | GPIO (5V) |
| PI6 | A11 | GPIO (5V) | PF14 | A12 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PC1 | K2 | GPIO (5V) | PE0 | K12 | GPIO (5V) |
| VREGSW | K13 | DCDC regulator switching node | PC2 | L1 | GPIO (5V) |
| PC3 | L2 | GPIO (5V) | PA7 | L3 | GPIO |
| PB9 | L13 | GPIO (5V) | PB10 | L14 | GPIO (5V) |
| PD1 | L17 | GPIO | PC6 | L18 | GPIO |
| PC7 | L19 | GPIO | VREGVSS | L20 | Voltage regulator VSS |
| PB7 | M1 | GPIO | PC4 | M2 | GPIO |
| PA8 | M3 | GPIO | PA10 | M4 | GPIO |
| PA13 | M5 | GPIO (5V) | PA14 | M6 | GPIO |
| RESETn | M7 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB12 | M8 | GPIO |
| PD0 | M9 | GPIO (5V) | PD2 | M10 | GPIO (5V) |
| PD3 | M11 | GPIO | PD4 | M12 | GPIO |
| PD8 | M13 | GPIO | PB8 | N1 | GPIO |
| PC5 | N2 | GPIO | PA9 | N3 | GPIO |
| PA11 | N4 | GPIO | PA12 | N5 | GPIO (5V) |
| PB11 | N6 | GPIO | BODEN | N7 | Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. |
| PB13 | N8 | GPIO | PB14 | N9 | GPIO |
| AVDD | N10 | Analog power supply. | PD5 | N11 | GPIO |
| PD6 | N12 | GPIO | PD7 | N13 | GPIO |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PC1 | J1 | GPIO (5V) | PC3 | J2 | GPIO (5V) |
| PD15 | J3 | GPIO (5V) | PA12 | J4 | GPIO (5V) |
| PA9 | J5 | GPIO | PA10 | J6 | GPIO |
| PB9 | J7 | GPIO (5V) | PB10 | J8 | GPIO (5V) |
| PD2 | J9 | GPIO (5V) | PD3 | J10 | GPIO |
| PD4 | J11 | GPIO | PB7 | K1 | GPIO |
| PC4 | K2 | GPIO | PA13 | K3 | GPIO (5V) |
| PA11 | K5 | GPIO | RESETn | K6 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| AVDD | K8<br>K9<br>L10 | Analog power supply. | PD1 | K11 | GPIO |
| PB8 | L1 | GPIO | PC5 | L2 | GPIO |
| PA14 | L3 | GPIO | PB11 | L5 | GPIO |
| PB12 | L6 | GPIO | PB13 | L8 | GPIO |
| PB14 | L9 | GPIO | PD0 | L11 | GPIO (5V) |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

### 5.17 EFM32GG11B5xx in QFN64 Device Pinout

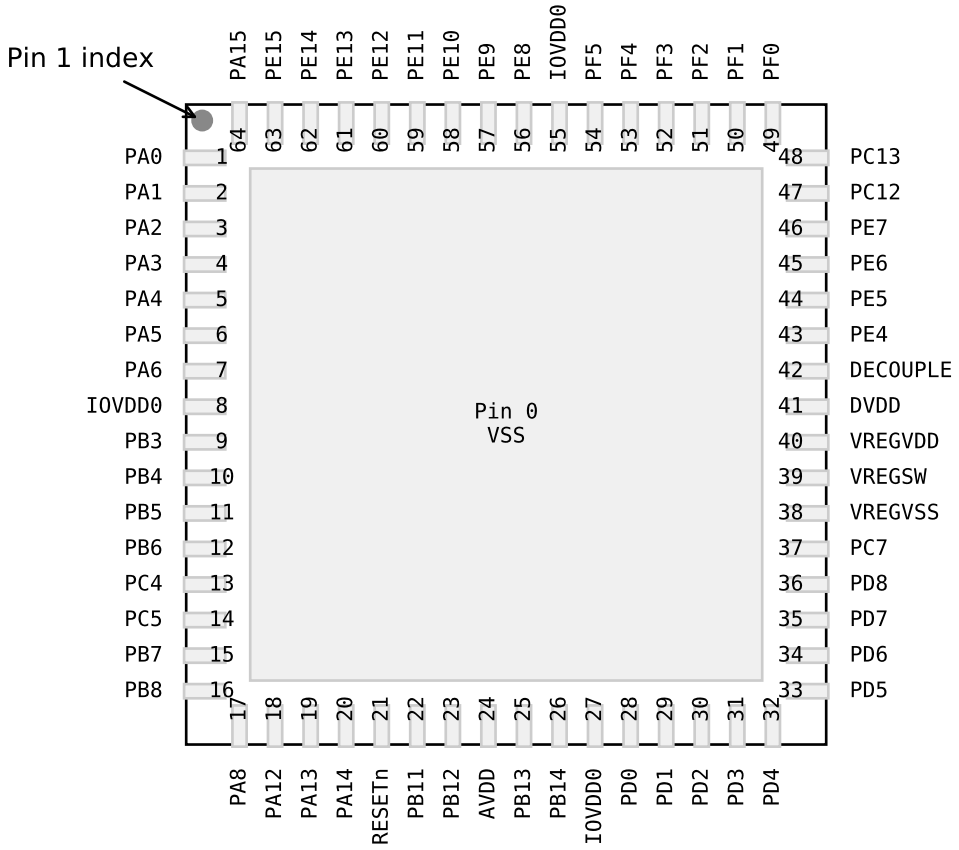


**Figure 5.17. EFM32GG11B5xx in QFN64 Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

**Table 5.17. EFM32GG11B5xx in QFN64 Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| VSS | 0 | Ground | PA0 | 1 | GPIO |
| PA1 | 2 | GPIO | PA2 | 3 | GPIO |
| PA3 | 4 | GPIO | PA4 | 5 | GPIO |
| PA5 | 6 | GPIO | PA6 | 7 | GPIO |
| IOVDD0 | 8<br>27<br>55 | Digital IO power supply 0. | PB3 | 9 | GPIO |
| PB4 | 10 | GPIO | PB5 | 11 | GPIO |

| Alternate | LOCATION | | |
|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| BU_STAT | 0: PE3 | | Backup Power Domain status, whether or not the system is in backup mode. |
| BU_VIN | 0: PD8 | | Battery input for Backup Power Domain. |
| BU_VOUT | 0: PE2 | | Power output for Backup Power Domain. |
| CAN0_RX | 0: PC0<br>1: PF0<br>2: PD0<br>3: PB9 | 4: PG8<br>5: PD14<br>6: PE0<br>7: PI12 | CAN0 RX. |
| CAN0_TX | 0: PC1<br>1: PF2<br>2: PD1<br>3: PB10 | 4: PG9<br>5: PD15<br>6: PE1<br>7: PI13 | CAN0 TX. |
| CAN1_RX | 0: PC2<br>1: PF1<br>2: PD3<br>3: PC9 | 4: PC12<br>5: PA12<br>6: PG10<br>7: PI14 | CAN1 RX. |
| CAN1_TX | 0: PC3<br>1: PF3<br>2: PD4<br>3: PC10 | 4: PC11<br>5: PA13<br>6: PG11<br>7: PI15 | CAN1 TX. |
| CMU_CLK0 | 0: PA2<br>1: PC12<br>2: PD7<br>3: PG2 | 4: PF2<br>5: PA12 | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | 0: PA1<br>1: PD8<br>2: PE12<br>3: PG1 | 4: PF3<br>5: PB11 | Clock Management Unit, clock output number 1. |
| CMU_CLK2 | 0: PA0<br>1: PA3<br>2: PD6<br>3: PG0 | 4: PA3<br>5: PD10 | Clock Management Unit, clock output number 2. |
| CMU_CLKI0 | 0: PD4<br>1: PA3<br>2: PB8<br>3: PB13 | 4: PE1<br>5: PD10<br>6: PE12<br>7: PB11 | Clock Management Unit, clock input number 0. |
| DBG_SWCLKTCK | 0: PF0 | | Debug-interface Serial Wire clock input and JTAG Test Clock.<br>Note that this function is enabled to the pin out of reset, and has a built-in pull down. |
| DBG_SWDIOTMS | 0: PF1 | | Debug-interface Serial Wire data input / output and JTAG Test Mode Select.<br>Note that this function is enabled to the pin out of reset, and has a built-in pull up. |

| Alternate | LOCATION | | |
|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| EBI_AD08 | 0: PA15<br>1: PC1<br>2: PG8 | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | 0: PA0<br>1: PC2<br>2: PG9 | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | 0: PA1<br>1: PC3<br>2: PG10 | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | 0: PA2<br>1: PC4<br>2: PG11 | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | 0: PA3<br>1: PC5<br>2: PG12 | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | 0: PA4<br>1: PA7<br>2: PG13 | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | 0: PA5<br>1: PA8<br>2: PG14 | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | 0: PA6<br>1: PA9<br>2: PG15 | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | 0: PF3<br>1: PB9<br>2: PC4<br>3: PB5 | 4: PC11<br>5: PC11 | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | 0: PF2<br>1: PD13<br>2: PB15<br>3: PB4 | 4: PC13<br>5: PF10 | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | 0: PF6<br>1: PF8<br>2: PB10<br>3: PC1 | 4: PF6<br>5: PF6 | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | 0: PF7<br>1: PF9<br>2: PB11<br>3: PC3 | 4: PF7<br>5: PF7 | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | 0: PD9<br>1: PA10<br>2: PC0<br>3: PB0 | 4: PE8 | External Bus Interface (EBI) Chip Select output 0. |

| Alternate | LOCATION | | |
|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| LCD_SEG7 | 0: PE11 | | LCD segment line 7. |
| LCD_SEG8 | 0: PE12 | | LCD segment line 8. |
| LCD_SEG9 | 0: PE13 | | LCD segment line 9. |
| LCD_SEG10 | 0: PE14 | | LCD segment line 10. |
| LCD_SEG11 | 0: PE15 | | LCD segment line 11. |
| LCD_SEG12 | 0: PA15 | | LCD segment line 12. |
| LCD_SEG13 | 0: PA0 | | LCD segment line 13. |
| LCD_SEG14 | 0: PA1 | | LCD segment line 14. |
| LCD_SEG15 | 0: PA2 | | LCD segment line 15. |
| LCD_SEG16 | 0: PA3 | | LCD segment line 16. |
| LCD_SEG17 | 0: PA4 | | LCD segment line 17. |
| LCD_SEG18 | 0: PA5 | | LCD segment line 18. |
| LCD_SEG19 | 0: PA6 | | LCD segment line 19. |

| Alternate | LOCATION | | |
|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| US3_RTS | 0: PA5<br>1: PC1<br>2: PA14<br>3: PC15 | 4: PG5<br>5: PG11 | USART3 Request To Send hardware flow control output. |
| US3_RX | 0: PA1<br>1: PE7<br>2: PB7<br>3: PG7 | 4: PG1<br>5: PI13 | USART3 Asynchronous Receive.<br>USART3 Synchronous mode Master Input / Slave Output (MISO). |
| US3_TX | 0: PA0<br>1: PE6<br>2: PB3<br>3: PG6 | 4: PG0<br>5: PI12 | USART3 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART3 Synchronous mode Master Output / Slave Input (MOSI). |
| US4_CLK | 0: PC4<br>1: PD11<br>2: PI2<br>3: PI8 | 4: PH6 | USART4 clock input / output. |
| US4_CS | 0: PC5<br>1: PD12<br>2: PI3<br>3: PI9 | 4: PH7 | USART4 chip select input / output. |
| US4_CTS | 0: PA7<br>1: PD13<br>2: PI4<br>3: PI10 | 4: PH8 | USART4 Clear To Send hardware flow control input. |
| US4_RTS | 0: PA8<br>1: PD14<br>2: PI5<br>3: PI11 | 4: PH9 | USART4 Request To Send hardware flow control output. |
| US4_RX | 0: PB8<br>1: PD10<br>2: PI1<br>3: PI7 | 4: PH5 | USART4 Asynchronous Receive.<br>USART4 Synchronous mode Master Input / Slave Output (MISO). |
| US4_TX | 0: PB7<br>1: PD9<br>2: PI0<br>3: PI6 | 4: PH4 | USART4 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART4 Synchronous mode Master Output / Slave Input (MOSI). |
| US5_CLK | 0: PB11<br>1: PD13<br>2: PF13<br>3: PH12 | | USART5 clock input / output. |
| US5_CS | 0: PB13<br>1: PD14<br>2: PF12<br>3: PH13 | | USART5 chip select input / output. |
| US5_CTS | 0: PB14<br>1: PD15<br>2: PF11<br>3: PH14 | | USART5 Clear To Send hardware flow control input. |
| US5_RTS | 0: PB12<br>1: PB15<br>2: PF10<br>3: PH15 | | USART5 Request To Send hardware flow control output. |

| Alternate | LOCATION | | |
|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| US5_RX | 0: PE9<br>1: PA7<br>2: PB1<br>3: PH11 | | USART5 Asynchronous Receive.<br>USART5 Synchronous mode Master Input / Slave Output (MISO). |
| US5_TX | 0: PE8<br>1: PA6<br>2: PF15<br>3: PH10 | | USART5 Asynchronous Transmit. Also used as receive input in half duplex communication.<br>USART5 Synchronous mode Master Output / Slave Input (MOSI). |
| USB_DM | 0: PF10 | | USB D- pin. |
| USB_DP | 0: PF11 | | USB D+ pin. |
| USB_ID | 0: PF12 | | USB ID pin. |
| USB_VBUSEN | 0: PF5 | | USB 5 V VBUS enable. |
| VDAC0_EXT | 0: PD6 | | Digital to analog converter VDAC0 external reference input pin. |
| VDAC0_OUT0 / OPA0_OUT | 0: PB11 | | Digital to Analog Converter DAC0 output channel number 0. |
| VDAC0_OUT0ALT / OPA0_OUTALT | 0: PC0<br>1: PC1<br>2: PC2<br>3: PC3 | 4: PD0 | Digital to Analog Converter DAC0 alternative output for channel 0. |
| VDAC0_OUT1 / OPA1_OUT | 0: PB12 | | Digital to Analog Converter DAC0 output channel number 1. |
| VDAC0_OUT1ALT / OPA1_OUTALT | 0: PC12<br>1: PC13<br>2: PC14<br>3: PC15 | 4: PD1 | Digital to Analog Converter DAC0 alternative output for channel 1. |
| WTIM0_CC0 | 0: PE4<br>1: PA6<br>2: PG2<br>3: PG8 | 4: PC15<br>5: PB0<br>6: PB3<br>7: PC1 | Wide timer 0 Capture Compare input / output channel 0. |
| WTIM0_CC1 | 0: PE5<br>1: PD13<br>2: PG3<br>3: PG9 | 4: PF0<br>5: PB1<br>6: PB4<br>7: PC2 | Wide timer 0 Capture Compare input / output channel 1. |

### 6.3 BGA192 Package Marking


**Figure 6.3. BGA192 Package Marking**

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

### 8.2 BGA120 PCB Land Pattern

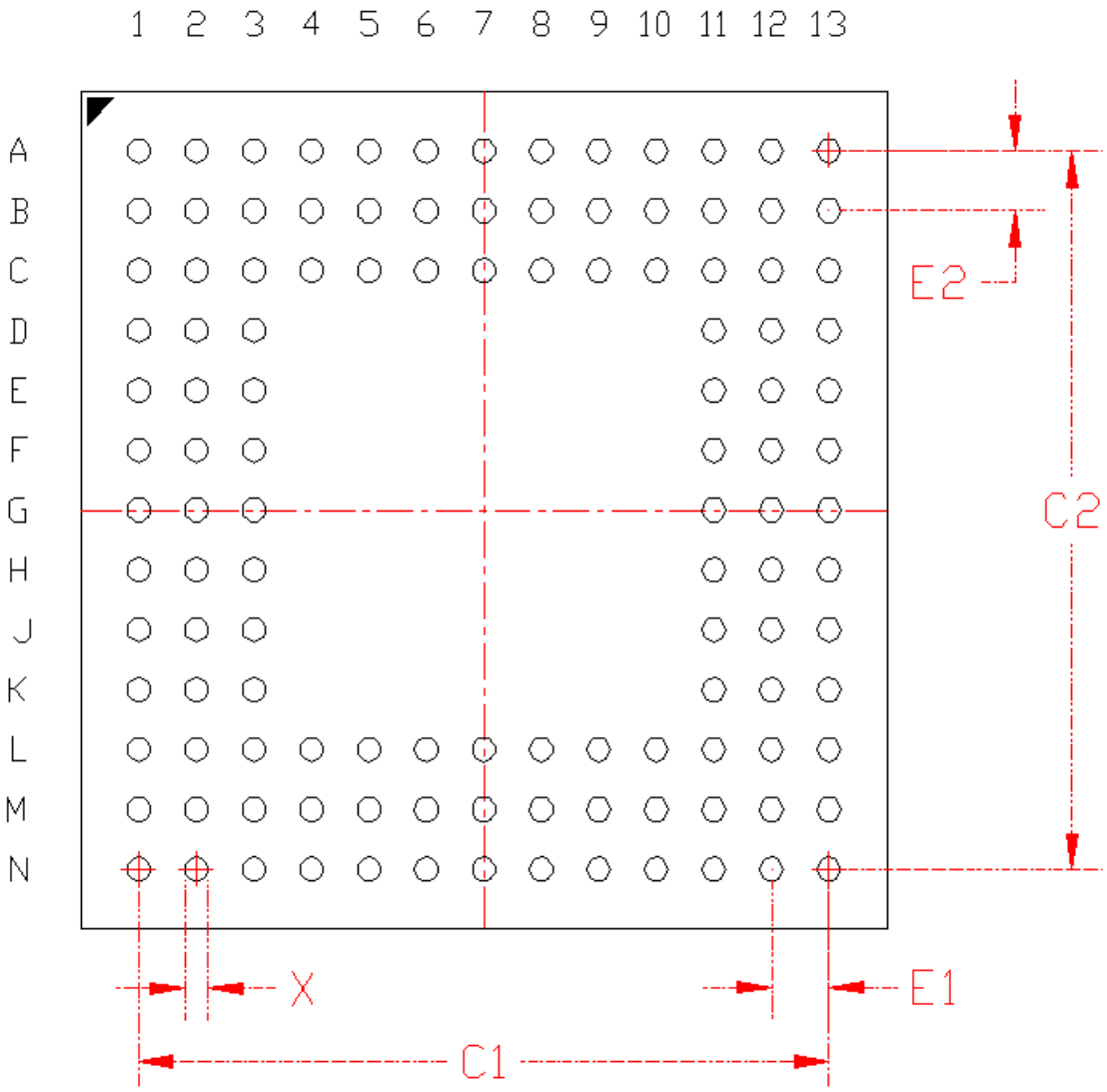


**Figure 8.2. BGA120 PCB Land Pattern Drawing**

### 8.3 BGA120 Package Marking


**Figure 8.3. BGA120 Package Marking**

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

### 9.3 BGA112 Package Marking


**Figure 9.3. BGA112 Package Marking**

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

**Table 11.1. TQFP64 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | — | 1.15 | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.09 | — | 0.20 |
| c1 | 0.09 | — | 0.16 |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| e | 0.50 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| R1 | 0.08 | — | — |
| R2 | 0.08 | — | 0.20 |
| S | 0.20 | — | — |
| θ | 0 | 3.5 | 7 |
| Θ1 | 0 | — | 0.10 |
| Θ2 | 11 | 12 | 13 |
| Θ3 | 11 | 12 | 13 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.