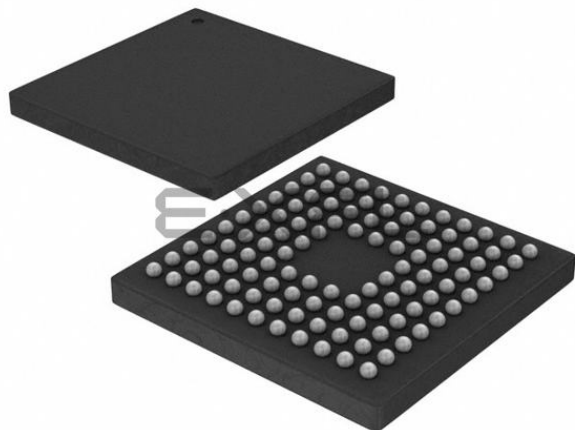




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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	87
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b420f2048il112-a

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3. System Overview

3.1 Introduction

The Giant Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Giant Gecko Series 1 Reference Manual.

A block diagram of the Giant Gecko Series 1 family is shown in [Figure 3.1 Detailed EFM32GG11 Block Diagram on page 11](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

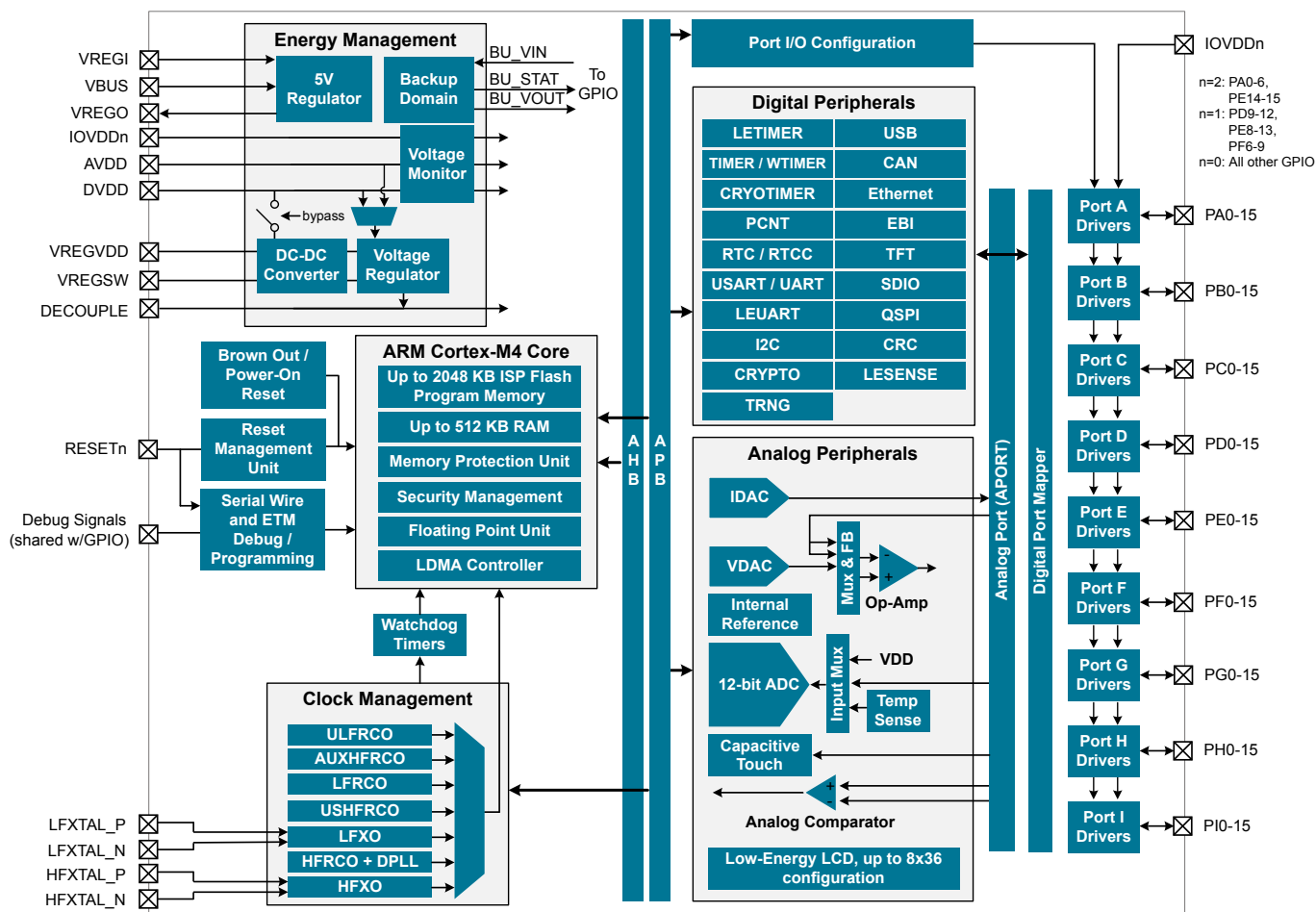


Figure 3.1. Detailed EFM32GG11 Block Diagram

3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

4.1.9 Brown Out Detector (BOD)

Table 4.11. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	V _{DVddbOD}	DVDD rising	—	—	1.62	V
		DVDD falling (EM0/EM1)	1.35	—	—	V
		DVDD falling (EM2/EM3)	TBD	—	—	V
DVDD BOD hysteresis	V _{DVddbOD_HYST}		—	18	—	mV
DVDD BOD response time	t _{DVddbOD_DELAY}	Supply drops at 0.1V/μs rate	—	2.4	—	μs
AVDD BOD threshold	V _{AVddbOD}	AVDD rising	—	—	1.8	V
		AVDD falling (EM0/EM1)	1.62	—	—	V
		AVDD falling (EM2/EM3)	TBD	—	—	V
AVDD BOD hysteresis	V _{AVddbOD_HYST}		—	20	—	mV
AVDD BOD response time	t _{AVddbOD_DELAY}	Supply drops at 0.1V/μs rate	—	2.4	—	μs
EM4 BOD threshold	V _{EM4dBOD}	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V _{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t _{EM4BOD_DELAY}	Supply drops at 0.1V/μs rate	—	300	—	μs

4.1.10 Oscillators

4.1.10.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.12. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	k Ω
Supported range of crystal load capacitance ¹	$C_{\text{LFXO_CL}}$		6	—	18	pF
On-chip tuning cap range ²	$C_{\text{LFXO_T}}$	On each of LFX TAL_N and LFX TAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup ³	I_{LFXO}	ESR = 70 k Ω m, C_L = 7 pF, GAIN ⁴ = 2, AGC ⁴ = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR = 70 k Ω m, C_L = 7 pF, GAIN ⁴ = 2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be $C_{\text{LFXO_T}}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output fall time, From 70% to 30% of V _{IO}	t _{IOOF}	C _L = 50 pF, DRIVESTRENGTH ¹ = STRONG, SLEWRATE ¹ = 0x6	—	1.8	—	ns
		C _L = 50 pF, DRIVESTRENGTH ¹ = WEAK, SLEWRATE ¹ = 0x6	—	4.5	—	ns
Output rise time, From 30% to 70% of V _{IO}	t _{IOOR}	C _L = 50 pF, DRIVESTRENGTH ¹ = STRONG, SLEWRATE = 0x6 ¹	—	2.2	—	ns
		C _L = 50 pF, DRIVESTRENGTH ¹ = WEAK, SLEWRATE ¹ = 0x6	—	7.4	—	ns
Note: 1. In GPIO_Pn_CTRL register.						

4.1.14 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.22. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	V _{RESOLUTION}		6	—	12	Bits
Input voltage range ⁵	V _{ADCIN}	Single ended	—	—	V _{FS}	V
		Differential	-V _{FS} /2	—	V _{FS} /2	V
Input range of external reference voltage, single ended and differential	V _{ADCREFIN_P}		1	—	V _{AVDD}	V
Power supply rejection ²	PSRR _{ADC}	At DC	—	80	—	dB
Analog input common mode rejection ratio	CMRR _{ADC}	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continuous operation. WAR-MUPMODE ⁴ = KEEPADC-WARM	I _{ADC_CONTINUOUS_LP}	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³	—	270	TBD	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 ³	—	125	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 ³	—	80	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR-MUPMODE ⁴ = NORMAL	I _{ADC_NORMAL_LP}	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³	—	45	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 ³	—	8	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ⁴ = KEEP-INSTANDBY or KEEPIN-SLOWACC	I _{ADC_STANDBY_LP}	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³	—	105	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 ³	—	70	—	μA
Current from all supplies, using internal reference buffer. Continuous operation. WAR-MUPMODE ⁴ = KEEPADC-WARM	I _{ADC_CONTINUOUS_HP}	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ³	—	325	—	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 ³	—	175	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 ³	—	125	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WAR-MUPMODE ⁴ = NORMAL	I _{ADC_NORMAL_HP}	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ³	—	85	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 ³	—	16	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE ⁴ = KEEP-INSTANDBY or KEEPIN-SLOWACC	I _{ADC_STANDBY_HP}	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ³	—	160	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 ³	—	125	—	μA
Current from HFPERCLK	I _{ADC_CLK}	HFPERCLK = 16 MHz	—	180	—	μA

4.1.15 Analog Comparator (ACMP)

Table 4.23. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL ¹	—	—	$V_{ACMPVDD}$	V
Supply voltage	$V_{ACMPVDD}$	BIASPROG ⁴ ≤ 0x10 or FULL- BIAS ⁴ = 0	1.8	—	$V_{VREGVDD_MAX}$	V
		0x10 < BIASPROG ⁴ ≤ 0x20 and FULLBIAS ⁴ = 1	2.1	—	$V_{VREGVDD_MAX}$	V
Active current not including voltage reference ²	I_{ACMP}	BIASPROG ⁴ = 1, FULLBIAS ⁴ = 0	—	50	—	nA
		BIASPROG ⁴ = 0x10, FULLBIAS ⁴ = 0	—	306	—	nA
		BIASPROG ⁴ = 0x02, FULLBIAS ⁴ = 1	—	6.5	—	μA
		BIASPROG ⁴ = 0x20, FULLBIAS ⁴ = 1	—	74	TBD	μA
Current consumption of inter- nal voltage reference ²	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	μA
		VADIV selected as input using VDD/1	—	2.4	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
MISO hold time ^{1 3}	t_{H_MI}	USART2, location 4, IOVDD = 1.8 V	-11.6	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	-11.6	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	-9.1	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	-9.1	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	-8	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	-8	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. t_{H_PERCLK} is one period of the selected HPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

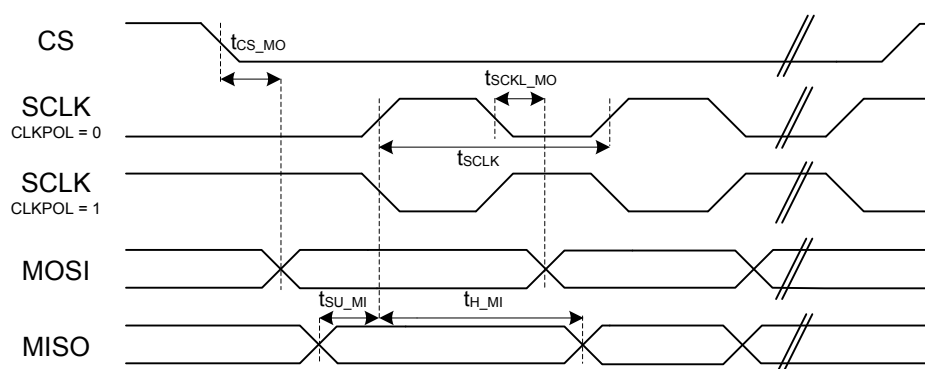


Figure 4.1. SPI Master Timing Diagram

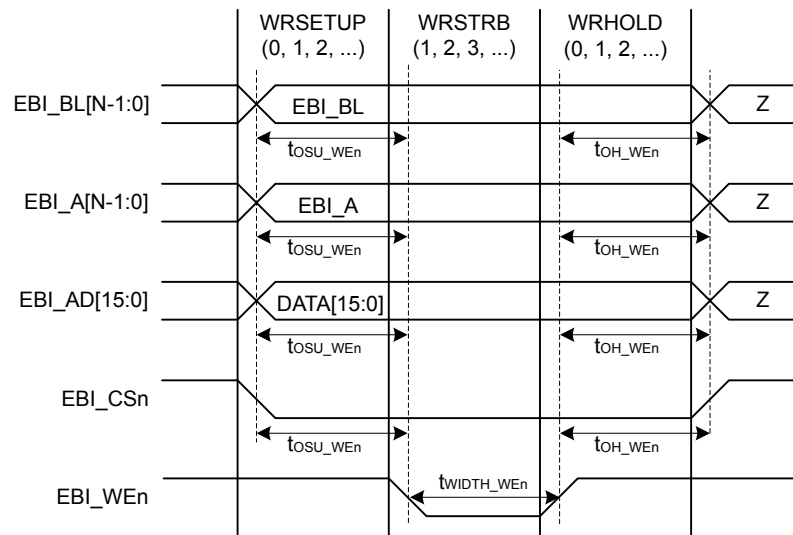


Figure 4.3. EBI Write Enable Output Timing Diagram

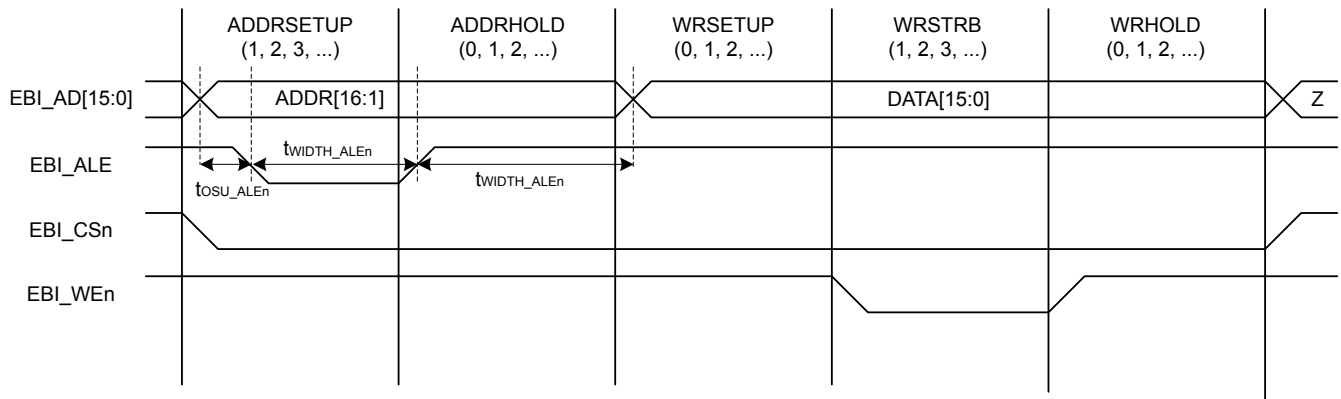


Figure 4.4. EBI Address Latch Enable Output Timing Diagram

EBI TFT Output Timing

All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.39. EBI TFT Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, EBI_DCLK to EBI_AD invalid	t_{OH_DCLK}	IOVDD $\geq$ 1.62 V	-23 + (TFTHOLD * t_{HFCOR-} ECLK)	—	—	ns
		IOVDD $\geq$ 3.0 V	-12 + (TFTHOLD * t_{HFCOR-} ECLK)	—	—	ns
Output setup time, EBI_AD valid to EBI_DCLK	t_{OSU_DCLK}	IOVDD $\geq$ 1.62 V	-11 + (TFTSET- UP * t_{HFCOR-} ECLK)	—	—	ns
		IOVDD $\geq$ 3.0 V	-9 + (TFTSET- UP * t_{HFCOR-} ECLK)	—	—	ns

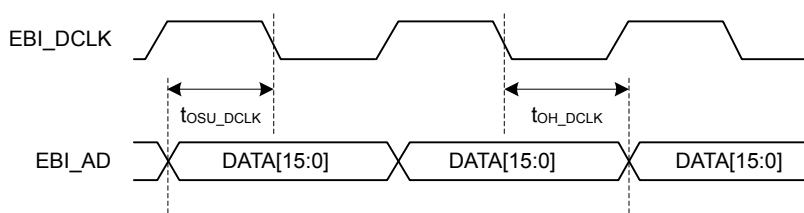


Figure 4.6. EBI TFT Output Timing

SDIO MMC DDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Table 4.53. SDIO MMC DDR Mode Timing (Location 0, 3V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.13	2.37	—	ns
Clock fall time	t_F		1.01	2.02	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		3	—	—	ns
Input setup time, DAT[0:7] valid to SD_CLK	t_{ISU2X}		5.3	—	—	ns
Input hold time, SD_CLK to DAT[0:7] change	t_{IH2X}		2.5	—	—	ns
Output delay time, SD_CLK to DAT[0:7] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:7] change	t_{OH2X}		3	—	—	ns

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF13	B9	GPIO (5V)
PF4	B10	GPIO	PF3	B11	GPIO
NC	B12	No Connect.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 L12 L15	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L16	Digital IO power supply 0.
PF2	C10	GPIO	PF1	C11	GPIO (5V)
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PF0	D11	GPIO (5V)
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PC9	E11	GPIO (5V)
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE6	F11	GPIO
PE7	F12	GPIO	PC8	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE3	G11	GPIO
PE4	G12	GPIO	PE5	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
DECOUPLE	H13	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PD14	J1	GPIO (5V)
PD15	J2	GPIO (5V)	PE1	J12	GPIO (5V)
VREGVDD	J13	Voltage regulator VDD input	PC0	K1	GPIO (5V)

5.14 EFM32GG11B4xx in QFP64 Device Pinout

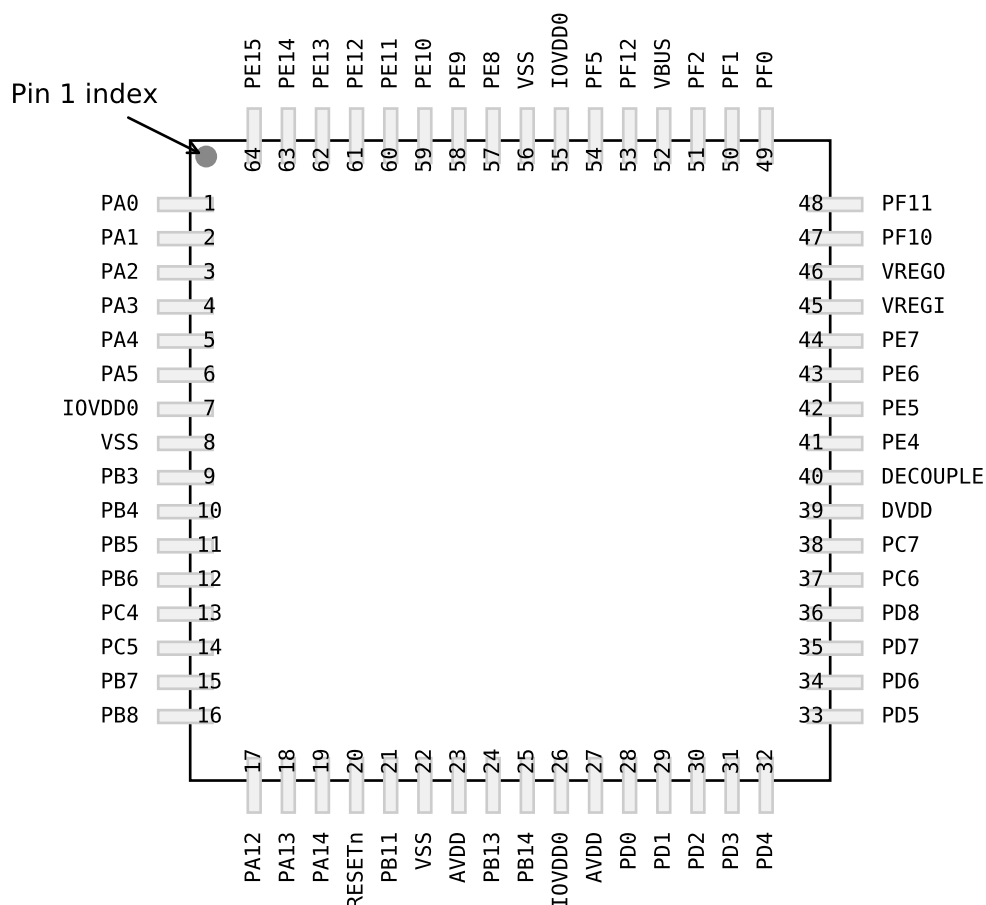


Figure 5.14. EFM32GG11B4xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.14. EFM32GG11B4xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

5.18 EFM32GG11B4xx in QFN64 Device Pinout

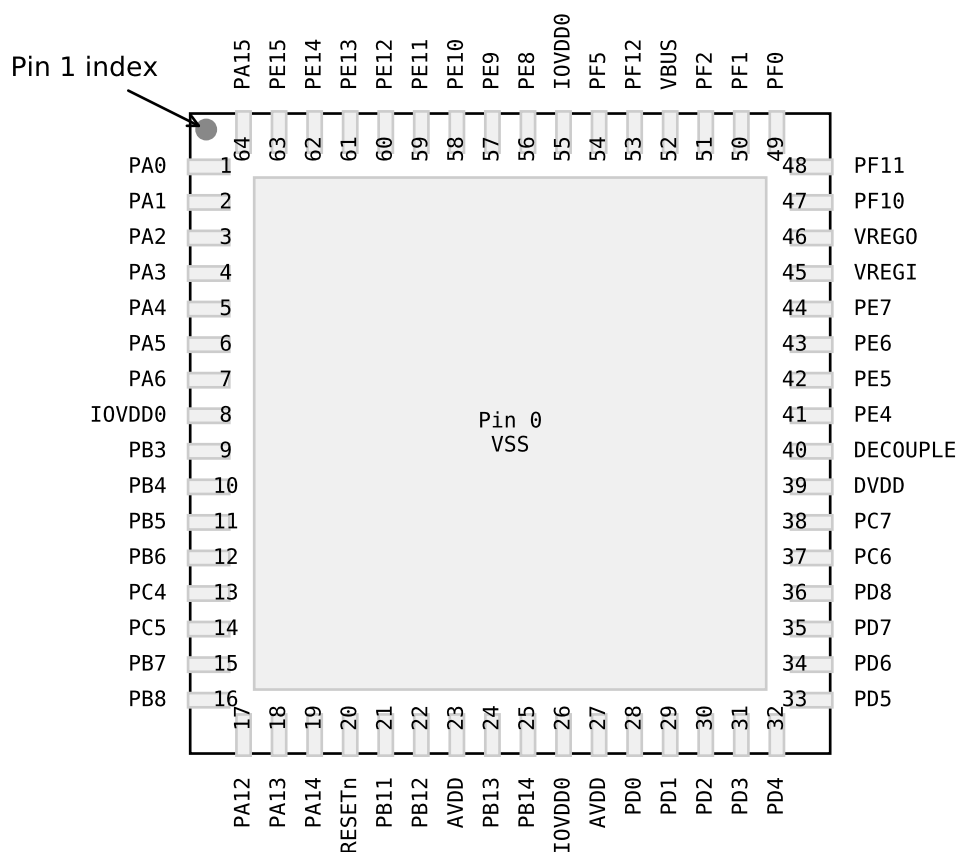


Figure 5.18. EFM32GG11B4xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.18. EFM32GG11B4xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO (5V)
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	VREGI	45	Input to 5 V regulator.
VREGO	46	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs	PF10	47	GPIO (5V)
PF11	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PRS_CH20	0: PB4 1: PC12 2: PE2		Peripheral Reflex System PRS, channel 20.
PRS_CH21	0: PB5 1: PC13 2: PB11		Peripheral Reflex System PRS, channel 21.
PRS_CH22	0: PB7 1: PE0 2: PF6		Peripheral Reflex System PRS, channel 22.
PRS_CH23	0: PB8 1: PE1 2: PF7		Peripheral Reflex System PRS, channel 23.
QSPI0_CS0	0: PF7 1: PA0 2: PG9		Quad SPI 0 Chip Select 0.
QSPI0_CS1	0: PF8 1: PA1 2: PG10		Quad SPI 0 Chip Select 1.
QSPI0_DQ0	0: PD9 1: PA2 2: PG1		Quad SPI 0 Data 0.
QSPI0_DQ1	0: PD10 1: PA3 2: PG2		Quad SPI 0 Data 1.
QSPI0_DQ2	0: PD11 1: PA4 2: PG3		Quad SPI 0 Data 2.
QSPI0_DQ3	0: PD12 1: PA5 2: PG4		Quad SPI 0 Data 3.
QSPI0_DQ4	0: PE8 1: PB3 2: PG5		Quad SPI 0 Data 4.
QSPI0_DQ5	0: PE9 1: PB4 2: PG6		Quad SPI 0 Data 5.
QSPI0_DQ6	0: PE10 1: PB5 2: PG7		Quad SPI 0 Data 6.

Table 12.1. QFN64 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.203 REF		
D	9.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.