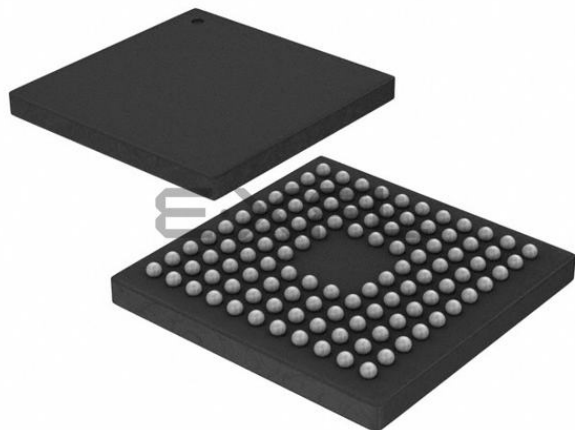




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	87
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b420f2048il112-b

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3. System Overview

3.1 Introduction

The Giant Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Giant Gecko Series 1 Reference Manual.

A block diagram of the Giant Gecko Series 1 family is shown in [Figure 3.1 Detailed EFM32GG11 Block Diagram on page 11](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

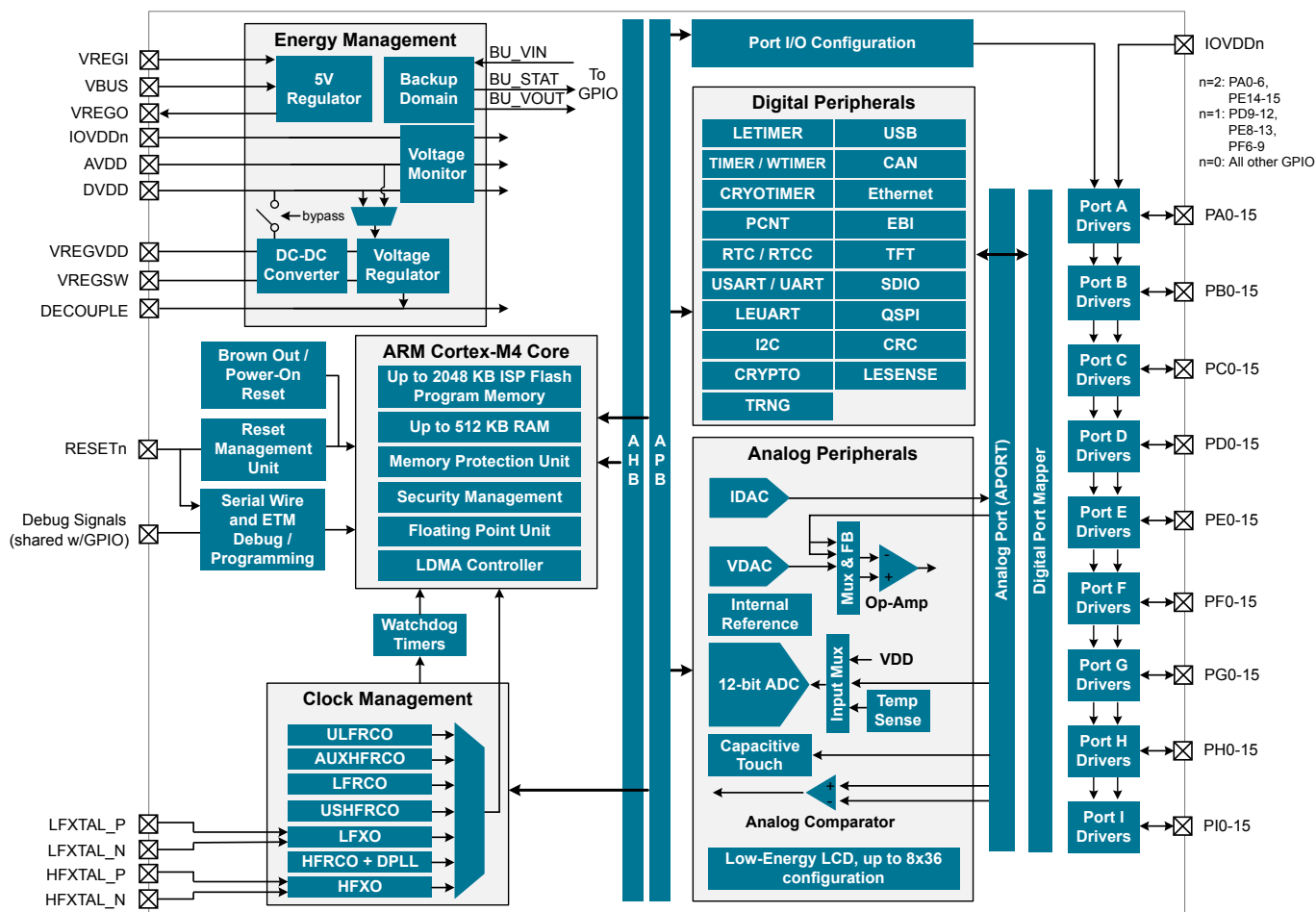


Figure 3.1. Detailed EFM32GG11 Block Diagram

3.12 Configuration Summary

The features of the EFM32GG11 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA, SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	I ² S, SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	IrDA, SmartCard, High-Speed	US2_TX, US2_RX, US2_CLK, US2_CS
USART3	I ² S, SmartCard	US3_TX, US3_RX, US3_CLK, US3_CS
USART4	I ² S, SmartCard	US4_TX, US4_RX, US4_CLK, US4_CS
USART5	SmartCard	US5_TX, US5_RX, US5_CLK, US5_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
TIMER2	with DTI	TIM2_CC[2:0], TIM2_CDTI[2:0]
TIMER3	-	TIM3_CC[2:0]
TIMER4	with DTI	TIM4_CC[2:0], TIM4_CDTI[2:0]
TIMER5	-	TIM5_CC[2:0]
TIMER6	with DTI	TIM6_CC[2:0], TIM6_CDTI[2:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]
WTIMER1	-	WTIM1_CC[3:0]
WTIMER2	-	WTIM2_CC[2:0]
WTIMER3	-	WTIM3_CC[2:0]

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 μ H (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 μ F (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V _{DCDC_I}	Bypass mode, I _{DCDC_LOAD} = 50 mA	1.8	—	V _{VREGVDD_MAX}	V
		Low noise (LN) mode, 1.8 V output, I _{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I _{DCDC_LOAD} = 10 mA	2.4	—	V _{VREGVDD_MAX}	V
		Low noise (LN) mode, 1.8 V output, I _{DCDC_LOAD} = 200 mA	2.6	—	V _{VREGVDD_MAX}	V
Output voltage programmable range ¹	V _{DCDC_O}		1.8	—	V _{VREGVDD}	V
Regulation DC accuracy	ACC _{DC}	Low Noise (LN) mode, 1.8 V target output	TBD	—	TBD	V
Regulation window ⁴	WIN _{REG}	Low Power (LP) mode, LPCMPBIASEMxx ³ = 0, 1.8 V target output, I _{DCDC_LOAD} ≤ 75 μ A	TBD	—	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx ³ = 3, 1.8 V target output, I _{DCDC_LOAD} ≤ 10 mA	TBD	—	TBD	V
Steady-state output ripple	V _R		—	3	—	mVpp
Output voltage under/overshoot	V _{OV}	CCM Mode (LNFORCECCM ³ = 1), Load changes between 0 mA and 100 mA	—	25	TBD	mV
		DCM Mode (LNFORCECCM ³ = 0), Load changes between 0 mA and 10 mA	—	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM ³ = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM ³ = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V _{REG}	Input changes between V _{VREGVDD_MAX} and 2.4 V	—	0.1	—	%
DC load regulation	I _{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

4.1.7 Current Consumption

4.1.7.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.7. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	72 MHz HFRCO, CPU running Prime from flash	—	120	—	μA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	120	TBD	μA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	140	—	μA/MHz
		50 MHz crystal, CPU running while loop from flash	—	123	—	μA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	122	TBD	μA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	124	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	126	TBD	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	131	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	319	TBD	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I _{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	107	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	262	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	72 MHz HFRCO	—	57	TBD	μA/MHz
		50 MHz crystal	—	60	—	μA/MHz
		48 MHz HFRCO	—	59	TBD	μA/MHz
		32 MHz HFRCO	—	61	—	μA/MHz
		26 MHz HFRCO	—	63	TBD	μA/MHz
		16 MHz HFRCO	—	68	—	μA/MHz
		1 MHz HFRCO	—	255	TBD	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I _{EM1_VS}	19 MHz HFRCO	—	55	—	μA/MHz
		1 MHz HFRCO	—	210	—	μA/MHz

4.1.13 Voltage Monitor (VMON)

Table 4.21. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I _{SENSE})	I _{VMON}	In EM0 or EM1, 1 supply monitored, T ≤ 85 °C	—	6.0	TBD	μA
		In EM0 or EM1, 4 supplies monitored, T ≤ 85 °C	—	14.9	TBD	μA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I _{SENSE}	In EM0 or EM1	—	2	—	μA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V _{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N _{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t _{VMON_RES}	Supply drops at 1V/μs rate	—	460	—	ns
Hysteresis	V _{VMON_HYST}		—	26	—	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	f_{ADCRATE}		—	—	1	Msp/s
Conversion time ¹	t_{ADCCONV}	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	t_{ADCSTART}	WARMUPMODE ⁴ = NORMAL	—	—	5	μs
		WARMUPMODE ⁴ = KEEPIN-STANDBY	—	—	2	μs
		WARMUPMODE ⁴ = KEEPINSLOWACC	—	—	1	μs
SNDR at 1Msp/s and $f_{\text{IN}} = 10\text{kHz}$	SNDR_{ADC}	Internal reference ⁷ , differential measurement	TBD	67	—	dB
		External reference ⁶ , differential measurement	—	68	—	dB
Spurious-free dynamic range (SFDR)	SFDR_{ADC}	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing codes	TBD	—	TBD	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	TBD	—	TBD	LSB
Offset error	$V_{\text{ADCOFFSETERR}}$		TBD	0	TBD	LSB
Gain error in ADC	V_{ADCGAIN}	Using internal reference	—	-0.2	TBD	%
		Using external reference	—	-1	—	%
Temperature sensor slope	$V_{\text{TS_SLOPE}}$		—	-1.84	—	mV/°C

Note:

- Derived from ADCCLK.
- PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
- In ADCn_BIASPROG register.
- In ADCn_CNTL register.
- The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
- External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is $\pm 1.25\text{ V}$.
- Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is $\pm 1.25\text{ V}$. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD. 2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$. 3. ± 100 mV differential drive. 4. In ACMPn_CTRL register. 5. In ACMPn_HYSTERESIS registers. 6. In ACMPn_INPUTSEL register.						

4.1.21 Pulse Counter (PCNT)

Table 4.29. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.22 Analog Port (APORT)

Table 4.30. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current ^{2 1}	I_{APORT}	Operation in EM0/EM1	—	7	—	μA
		Operation in EM2/EM3	—	915	—	nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by multiplying the duty cycle of the requests by the specified continuous current number.
2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

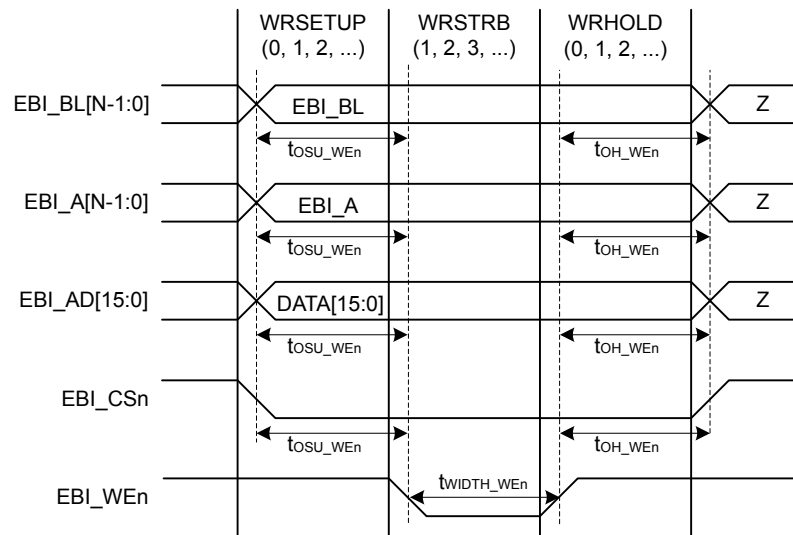


Figure 4.3. EBI Write Enable Output Timing Diagram

EBI Address Latch Enable Output Timing

Timing applies to multiplexed addressing modes D8A24ALE and D16A16ALE for both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.37. EBI Address Latch Enable Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_ALE edge to EBI_AD invalid ^{1 2}	t_{OH_ALEn}	IOVDD $\geq$ 1.62 V	-22 + (ADDR-HOLD * $t_{HFCOR-ECLK}$)	—	—	ns
		IOVDD $\geq$ 3.0 V	-11 + (ADDR-HOLD * $t_{HFCOR-ECLK}$)	—	—	ns
Output setup time, from EBI_AD valid to leading EBI_ALE edge	t_{OSU_ALEn}	IOVDD $\geq$ 1.62 V	-12	—	—	ns
		IOVDD $\geq$ 3.0 V	-9	—	—	ns
EBI_ALEn pulse width ¹	t_{WIDTH_ALEn}	IOVDD $\geq$ 1.62 V	-4 + ((ADDR-SETUP + 1) * $t_{HFCOR-ECLK}$)	—	—	ns
		IOVDD $\geq$ 3.0 V	-3 + ((ADDR-SETUP + 1) * $t_{HFCOR-ECLK}$)	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALEn can be moved to the left by setting HALFALE=1. This decreases the length of t_{WIDTH_ALEn} and increases the length of t_{OSU_ALEn} by $t_{HFCORECLK} - 1/2 * t_{HFCLKNODIV}$.
2. The figure shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

RMII Receive Timing

Timing is specified with $3.0\text{ V} \leq \text{IOVDD} \leq 3.8\text{ V}$, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.45. Ethernet RMII Receive Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REF_CLK frequency	$F_{\text{REF_CLK}}$	Output slew rate set to 7	—	50	—	MHz
REF_CLK duty cycle	$DC_{\text{REF_CLK}}$		35	—	65	%
Setup time, RXD[1:0], CRS_DV, RX_ER valid to REF_CLK	t_{SU}		4	—	—	ns
Hold time, REF_CLK to RXD[1:0], CRS_DV, RX_ER change	t_{HD}		2	—	—	ns

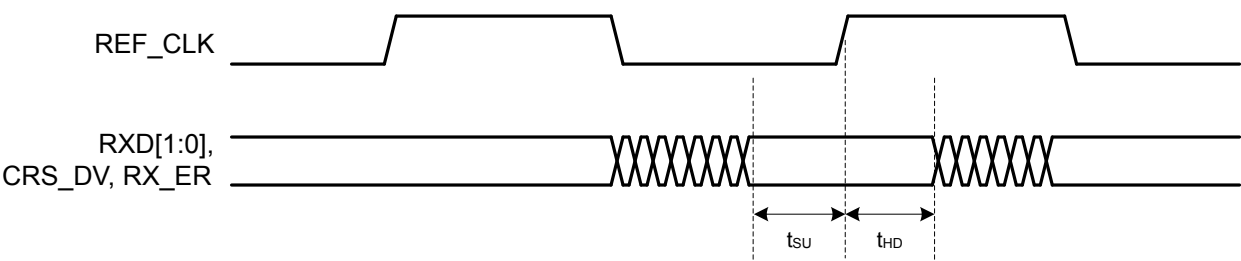


Figure 4.12. Ethernet RMII Receive Timing

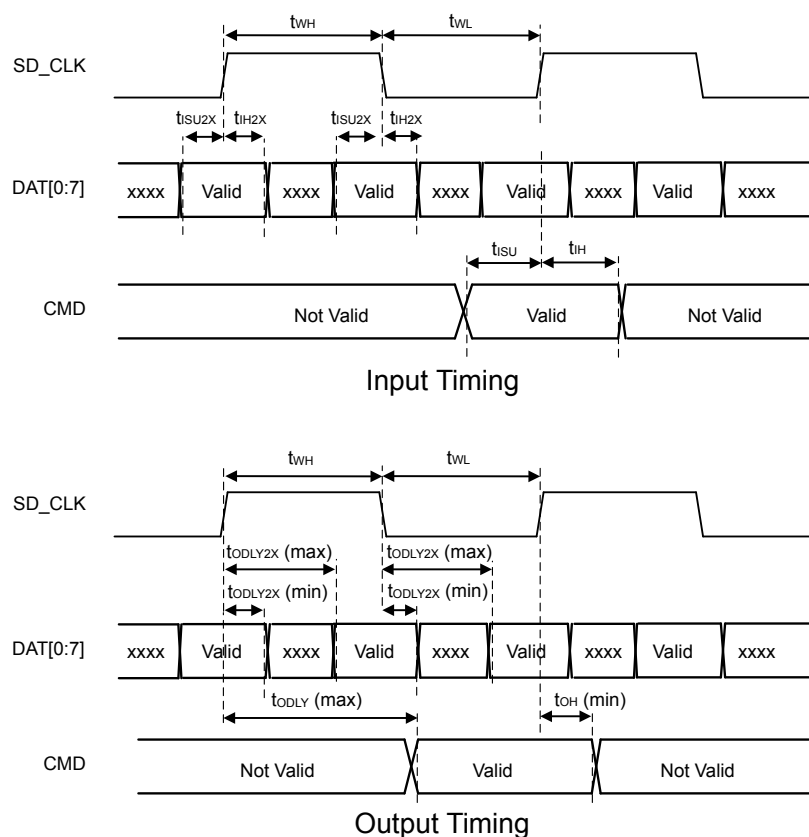


Figure 4.20. SDIO MMC DDR Mode Timing

4.1.28 Quad SPI (QSPI)

4.1.28.1 QSPI SDR Mode

QSPI SDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 23, RX DLL = 48, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.54. QSPI SDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full SCLK period	T		$(1/F_{SCLK}) * 0.95$	—	—	ns
Output valid	t_{OV}		—	—	$T/2 - 2.4$	ns
Output hold	t_{OH}		$T/2 - 32.9$	—	—	ns
Input setup	t_{SU}		$36.2 - T/2$	—	—	ns
Input hold	t_{H}		$T/2 - 3.3$	—	—	ns

4.1.28.2 QSPI DDR Mode

QSPI DDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 35, RX DLL = 70, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.56. QSPI DDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Half SCLK period	T/2	HFXO	$(1/F_{SCLK})^*$ 0.4 - 0.4	—	—	ns
		HFRCO, AUXHFRCO, USHFRCO	$(1/F_{SCLK})^*$ 0.44	—	—	ns
Output valid	t _{OV}		—	—	T/2 - 5.0	ns
Output hold	t _{OH}		T/2 - 39.4	—	—	ns
Input setup	t _{SU}		33.1	—	—	ns
Input hold	t _H		-0.9	—	—	ns

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

5.7 EFM32GG11B3xx in BGA112 Device Pinout

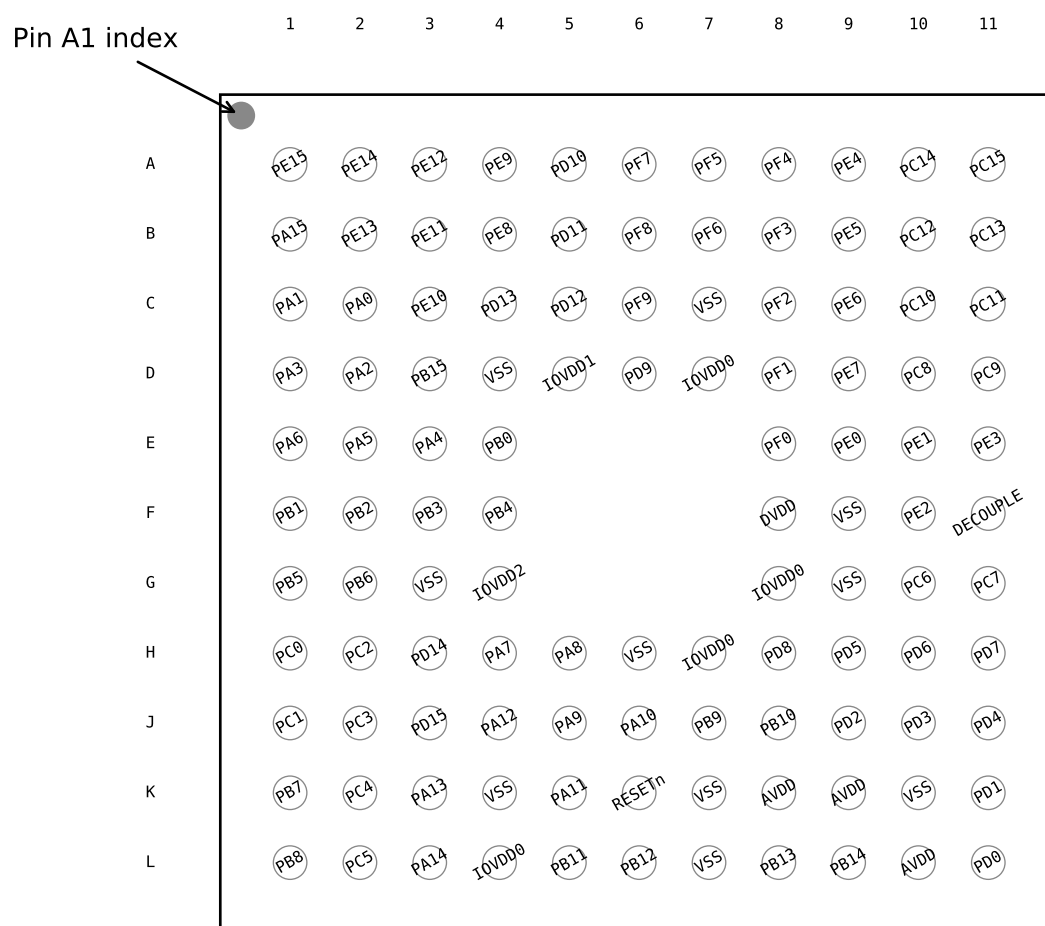


Figure 5.7. EFM32GG11B3xx in BGA112 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.7. EFM32GG11B3xx in BGA112 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD10	A5	GPIO	PF7	A6	GPIO
PF5	A7	GPIO	PF4	A8	GPIO
PE4	A9	GPIO	PC14	A10	GPIO (5V)
PC15	A11	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_AD08	0: PA15 1: PC1 2: PG8		External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	0: PA0 1: PC2 2: PG9		External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	0: PA1 1: PC3 2: PG10		External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	0: PA2 1: PC4 2: PG11		External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	0: PA3 1: PC5 2: PG12		External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	0: PA4 1: PA7 2: PG13		External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	0: PA5 1: PA8 2: PG14		External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	0: PA6 1: PA9 2: PG15		External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	0: PF3 1: PB9 2: PC4 3: PB5	4: PC11 5: PC11	External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	0: PF2 1: PD13 2: PB15 3: PB4	4: PC13 5: PF10	External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	0: PF6 1: PF8 2: PB10 3: PC1	4: PF6 5: PF6	External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	0: PF7 1: PF9 2: PB11 3: PC3	4: PF7 5: PF7	External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	0: PD9 1: PA10 2: PC0 3: PB0	4: PE8	External Bus Interface (EBI) Chip Select output 0.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US1_CTS	0: PB9 1: PD4 2: PF3 3: PC6	4: PC12 5: PB13 6: PH2	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PB10 1: PD5 2: PF4 3: PC7	4: PC13 5: PB14 6: PH3	USART1 Request To Send hardware flow control output.
US1_RX	0: PC1 1: PD1 2: PD6 3: PF7	4: PC2 5: PA0 6: PA2	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PC0 1: PD0 2: PD7 3: PF6	4: PC1 5: PF2 6: PA14	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	0: PC4 1: PB5 2: PA9 3: PA15	4: PF8 5: PF2	USART2 clock input / output.
US2_CS	0: PC5 1: PB6 2: PA10 3: PB11	4: PF9 5: PF5	USART2 chip select input / output.
US2_CTS	0: PC1 1: PB12 2: PA11 3: PB10	4: PC12 5: PD6	USART2 Clear To Send hardware flow control input.
US2_RTS	0: PC0 1: PB15 2: PA12 3: PC14	4: PC13 5: PD8	USART2 Request To Send hardware flow control output.
US2_RX	0: PC3 1: PB4 2: PA8 3: PA14	4: PF7 5: PF1	USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	0: PC2 1: PB3 2: PA7 3: PA13	4: PF6 5: PF0	USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
US3_CLK	0: PA2 1: PD7 2: PD4 3: PG8	4: PG2 5: PI14	USART3 clock input / output.
US3_CS	0: PA3 1: PE4 2: PC14 3: PC0	4: PG3 5: PI15	USART3 chip select input / output.
US3_CTS	0: PA4 1: PE5 2: PD6 3: PG10	4: PG4 5: PG9	USART3 Clear To Send hardware flow control input.

Table 5.29. CSEN Bus and Pin Mapping

Port	CEXT																																			
	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0			
	BUSCY	BUSCX	BUSAY	BUSAX	PF15	PF14	PF13	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	BUSBY	BUSBX	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0		
CEXT_SENSE																																				
APORT4Y	APORT4X	APORT2Y	APORT2X																																	
BUSDY	BUSDX	BUSBY	BUSBX																																	
	PF15		PB15																																	
PF14		PB14																																		
	PF13		PB13																																	
PF12		PB12																																		
	PF11		PB11																																	
PF10		PB10																																		
	PF9		PB9																																	
PF8																																				
	PF7																																			
PF6		PB6																																		
	PF5		PB5																																	
PF4		PB4																																		
	PF3		PB3																																	
PF2		PB2																																		
	PF1		PB1																																	
PF0		PB0																																		
	PE15		PA15																																	
PE14		PA14																																		
	PE13		PA13																																	
PE12		PA12																																		
	PE11		PA11																																	
PE10		PA10																																		
	PE9		PA9																																	
PE8		PA8																																		
	PE7		PA7																																	
PE6		PA6																																		
	PE5		PA5																																	
PE4		PA4																																		
			PA3																																	
		PA2																																		
	PE1		PA1																																	
PE0		PA0																																		

Table 5.30. IDAC0 Bus and Pin Mapping

APORT1Y	APORT1X	Port
BUSCY	BUSCX	Bus
PF15		CH31
	PF14	CH30
PF13		CH29
	PF12	CH28
PF11		CH27
	PF10	CH26
PF9		CH25
	PF8	CH24
PF7		CH23
	PF6	CH22
PF5		CH21
	PF4	CH20
PF3		CH19
	PF2	CH18
PF1		CH17
	PF0	CH16
PE15		CH15
	PE14	CH14
PE13		CH13
	PE12	CH12
PE11		CH11
	PE10	CH10
PE9		CH9
	PE8	CH8
PE7		CH7
	PE6	CH6
PE5		CH5
	PE4	CH4
		CH3
		CH2
PE1		CH1
	PE0	CH0