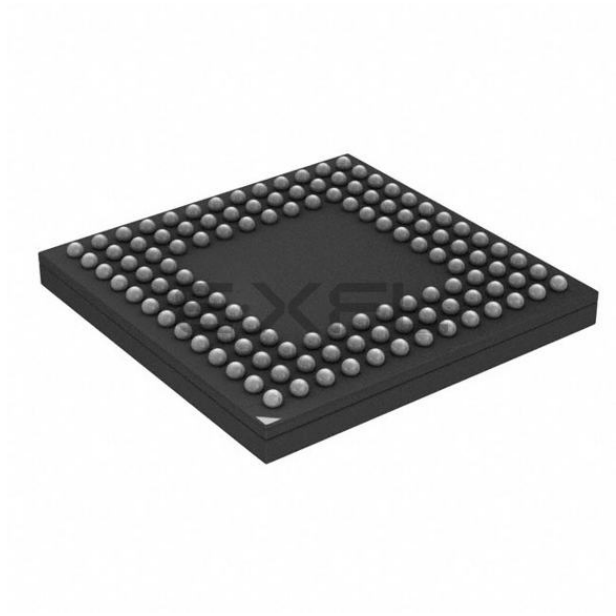
Silicon Labs - EFM32GG11B420F2048IL120-AR Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b420f2048il120-ar

3.2.4 EM2 and EM3 Power Domains

The EFM32GG11 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 13. If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

Table 3.1. EM2 and EM3 Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	PCNT1
ADC0	PCNT2
LETIMER0	CSEN
LESENSE	VDAC0
APORT	LEUART0
-	LEUART1
-	LETIMER1
-	I2C0
-	I2C1
-	I2C2
-	IDAC
-	ADC1
-	ACMP2
-	ACMP3
-	LCD
-	RTC

3.3 General Purpose Input/Output (GPIO)

EFM32GG11 has up to 144 General Purpose Input/Output pins. GPIO are organized on three independent supply rails, allowing for interface to multiple logic levels in the system simultaneously. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32GG11. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.94	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.62	—	µA
		128 byte RAM retention, no RTCC	—	0.62	—	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.13	—	µA
Current consumption of peripheral power domain 1, with voltage scaling enabled, DCDC in LP mode[3]	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[4]	—	0.68	—	µA
Current consumption of peripheral power domain 2, with voltage scaling enabled, DCDC in LP mode[3]	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[4]	—	0.28	—	µA

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.8 Wake Up Times

Table 4.10. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	11.8	—	µs
		Code execution from RAM	—	4.1	—	µs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	11.8	—	µs
		Code execution from RAM	—	4.1	—	µs
Wake up from EM4H[1]	t_{EM4H_WU}	Executing from flash	—	94	—	µs
Wake up from EM4S[1]	t_{EM4S_WU}	Executing from flash	—	294	—	µs
Time from release of reset source to first instruction execution	t_{RESET}	Soft Pin Reset released	—	55	—	µs
		Any other reset released	—	359	—	µs
Power mode scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz[4] [2]	—	31.8	—	µs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz[3]	—	4.3	—	µs

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/µs for approximately 20 µs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 µs + 29 HFCLKs.
4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 µs + 28 HFCLKs.

4.1.14 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.22. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range[5]	V_{ADCIN}	Single ended	—	—	V_{FS}	V
		Differential	$-V_{FS}/2$	—	$V_{FS}/2$	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[2]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_LP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	270	TBD	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [3]	—	125	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [3]	—	80	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_LP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	45	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [3]	—	8	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_LP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	105	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	70	—	µA
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_HP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	325	—	µA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [3]	—	175	—	µA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [3]	—	125	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	85	—	µA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	16	—	µA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	160	—	µA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	125	—	µA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	180	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

4.1.24 USART SPI

SPI Master Timing

Table 4.34. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}	All USARTs except USART2	2 * $t_{HFPERCLK}$	—	—	ns
		USART2	2 * $t_{HFPERBCLK}$	—	—	ns
CS to MOSI [1] [3]	t_{CS_MO}	USART2, location 4, IOVDD = 1.8 V	-3.2	—	6.8	ns
		USART2, location 4, IOVDD = 3.0 V	-2.3	—	6.0	ns
		USART2, location 5, IOVDD = 1.8 V	-8.1	—	6.3	ns
		USART2, location 5, IOVDD = 3.0 V	-7.3	—	4.4	ns
		All other USARTs and locations, IOVDD = 1.8 V	-15	—	13	ns
		All other USARTs and locations, IOVDD = 3.0 V	-13	—	11	ns
SCLK to MOSI [1] [3]	t_{SCLK_MO}	USART2, location 4, IOVDD = 1.8 V	-0.3	—	9.2	ns
		USART2, location 4, IOVDD = 3.0 V	-0.3	—	8.6	ns
		USART2, location 5, IOVDD = 1.8 V	-3.6	—	5.0	ns
		USART2, location 5, IOVDD = 3.0 V	-3.4	—	3.2	ns
		All other USARTs and locations, IOVDD = 1.8 V	-10	—	11	ns
		All other USARTs and locations, IOVDD = 3.0 V	-9	—	11	ns
MISO setup time [1] [3]	t_{SU_MI}	USART2, location 4, IOVDD = 1.8 V	39.7	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	22.4	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	49.2	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	30.0	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	55	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	36	—	—	ns

EBI Address Latch Enable Output Timing

Timing applies to multiplexed addressing modes D8A24ALE and D16A16ALE for both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.37. EBI Address Latch Enable Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_ALE edge to EBI_AD invalid[1] [2]	t_{OH_ALEn}	IOVDD ≥ 1.62 V	-22 + (ADDRHOLD * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-11 + (ADDRHOLD * $t_{HFCORECLK}$)	—	—	ns
Output setup time, from EBI_AD valid to leading EBI_ALE edge	t_{OSU_ALEn}	IOVDD ≥ 1.62 V	-12	—	—	ns
		IOVDD ≥ 3.0 V	-9	—	—	ns
EBI_ALEn pulse width[1]	t_{WIDTH_ALEn}	IOVDD ≥ 1.62 V	-4 + ((ADDRSETUP + 1) * $t_{\{\}HFCORECLK\{\}}$)	—	—	ns
		IOVDD ≥ 3.0 V	-3 + ((ADDRSETUP + 1) * $t_{\{\}HFCORECLK\{\}}$)	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALEn can be moved to the left by setting HALFALE=1. This decreases the length of t_{WIDTH_ALEn} and increases the length of t_{OSU_ALEn} by $t_{HFCORECLK}$ - 1/2 * $t_{HFCLKNODIV}$.
2. The figure shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

SDIO SDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.48. SDIO SDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		0.99	4.68	—	ns
Clock fall time	t_F		0.90	3.64	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}		8	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}		1.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}		0	—	35	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}		0.8	—	—	ns

SDIO MMC DDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Table 4.52. SDIO MMC DDR Mode Timing (Location 0, 1.8V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	18	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	25.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	25.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.13	5.21	—	ns
Clock fall time	t_F		1.01	4.10	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		3	—	—	ns
Input setup time, DAT[0:7] valid to SD_CLK	t_{ISU2X}		5.3	—	—	ns
Input hold time, SD_CLK to DAT[0:7] change	t_{IH2X}		2.5	—	—	ns
Output delay time, SD_CLK to DAT[0:7] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:7] change	t_{OH2X}		3	—	—	ns

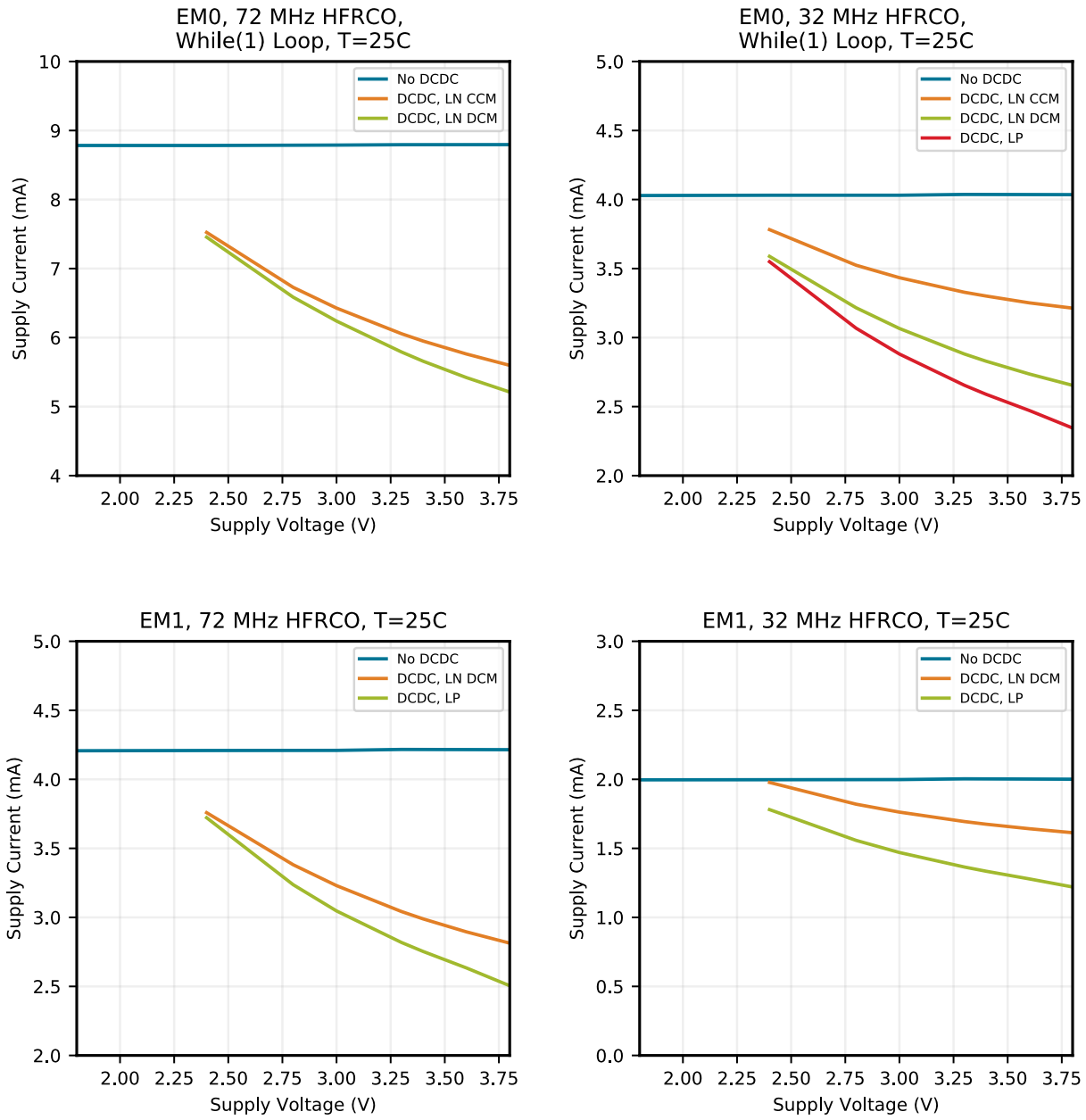

Figure 4.27. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	K2	GPIO (5V)	PE0	K12	GPIO (5V)
VREGSW	K13	DCDC regulator switching node	PC2	L1	GPIO (5V)
PC3	L2	GPIO (5V)	PA7	L3	GPIO
PB9	L13	GPIO (5V)	PB10	L14	GPIO (5V)
PD1	L17	GPIO	PC6	L18	GPIO
PC7	L19	GPIO	VREGVSS	L20	Voltage regulator VSS
PB7	M1	GPIO	PC4	M2	GPIO
PA8	M3	GPIO	PA10	M4	GPIO
PA13	M5	GPIO (5V)	PA14	M6	GPIO
RESETn	M7	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB12	M8	GPIO
PD0	M9	GPIO (5V)	PD2	M10	GPIO (5V)
PD3	M11	GPIO	PD4	M12	GPIO
PD8	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	BODEN	N7	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.
PB13	N8	GPIO	PB14	N9	GPIO
AVDD	N10	Analog power supply.	PD5	N11	GPIO
PD6	N12	GPIO	PD7	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.13 EFM32GG11B5xx in QFP64 Device Pinout

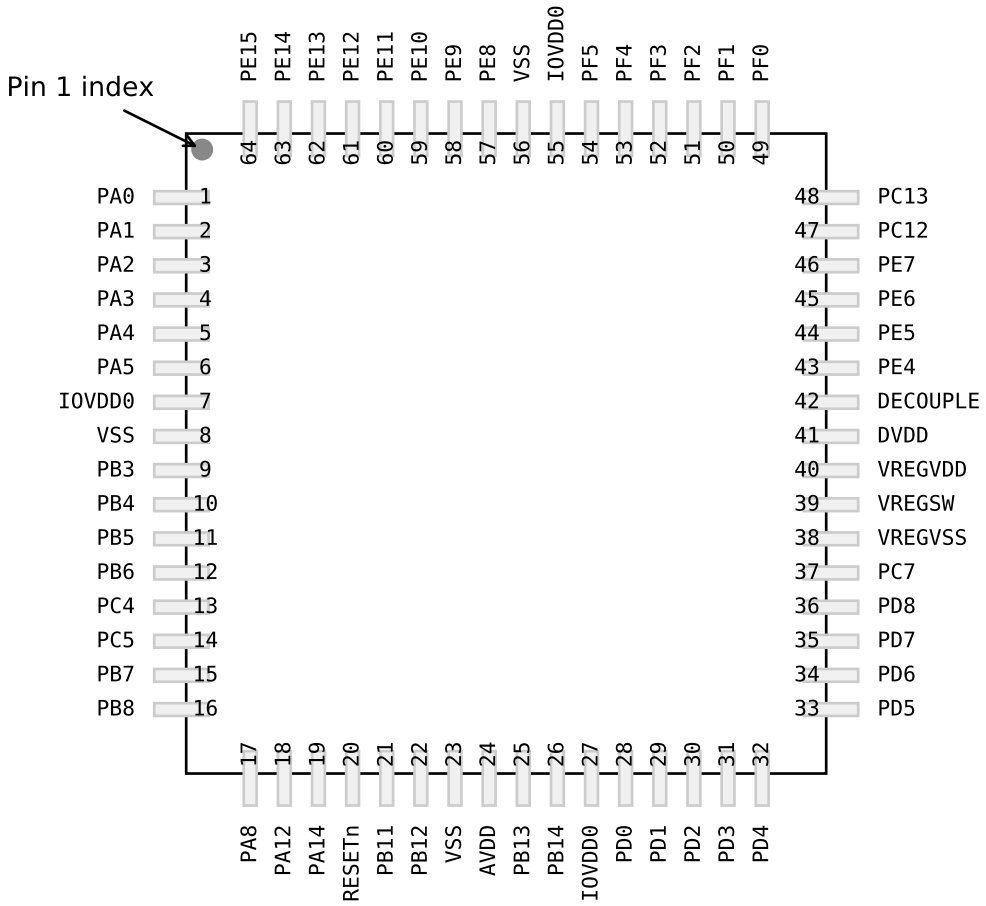

Figure 5.13. EFM32GG11B5xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.13. EFM32GG11B5xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA9	18	GPIO
PA10	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO (5V)
PC9	42	GPIO (5V)	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			

Note:
1. GPIO with 5V tolerance are indicated by (5V).

5.19 EFM32GG11B1xx in QFN64 Device Pinout

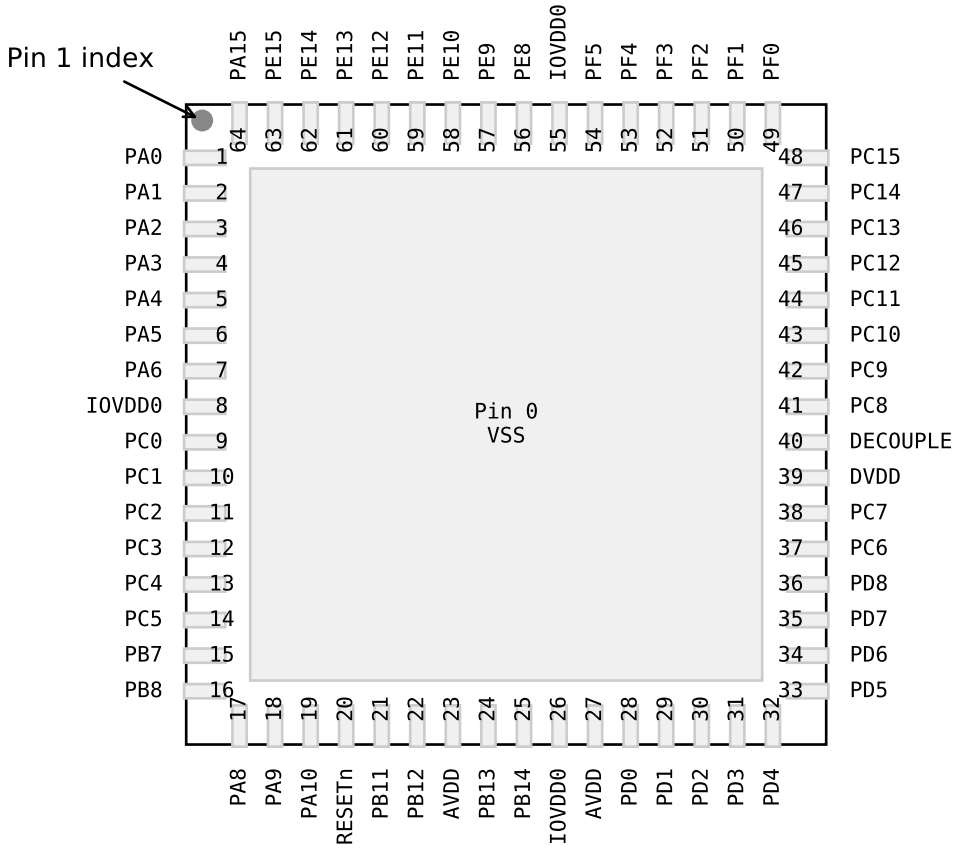

Figure 5.19. EFM32GG11B1xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.19. EFM32GG11B1xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PC0	9	GPIO (5V)
PC1	10	GPIO (5V)	PC2	11	GPIO (5V)

6.2 BGA192 PCB Land Pattern

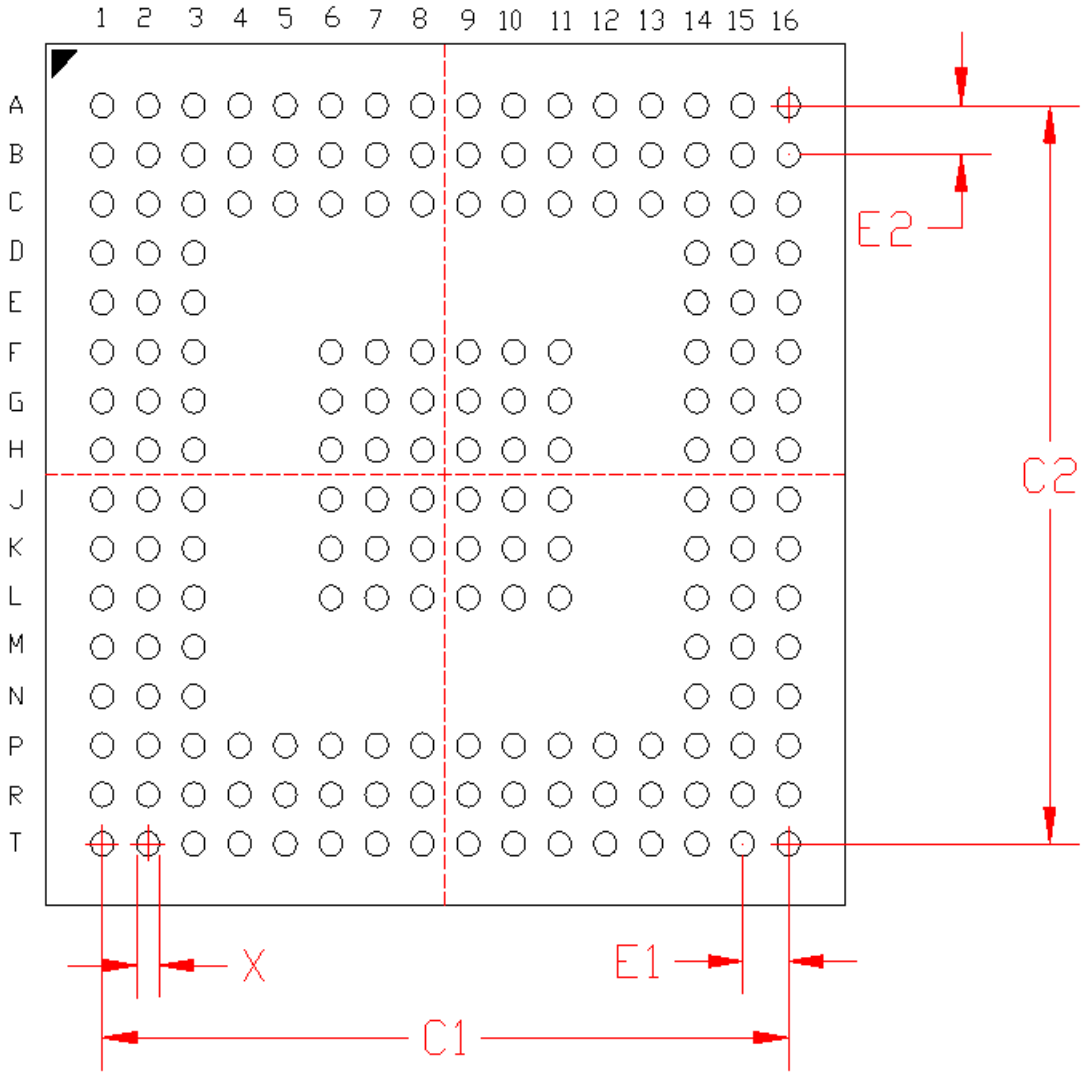

Figure 6.2. BGA192 PCB Land Pattern Drawing

Table 8.2. BGA120 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.20	
C1		6.00	
C2		6.00	
E1		0.5	
E2		0.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10.2 TQFP100 PCB Land Pattern

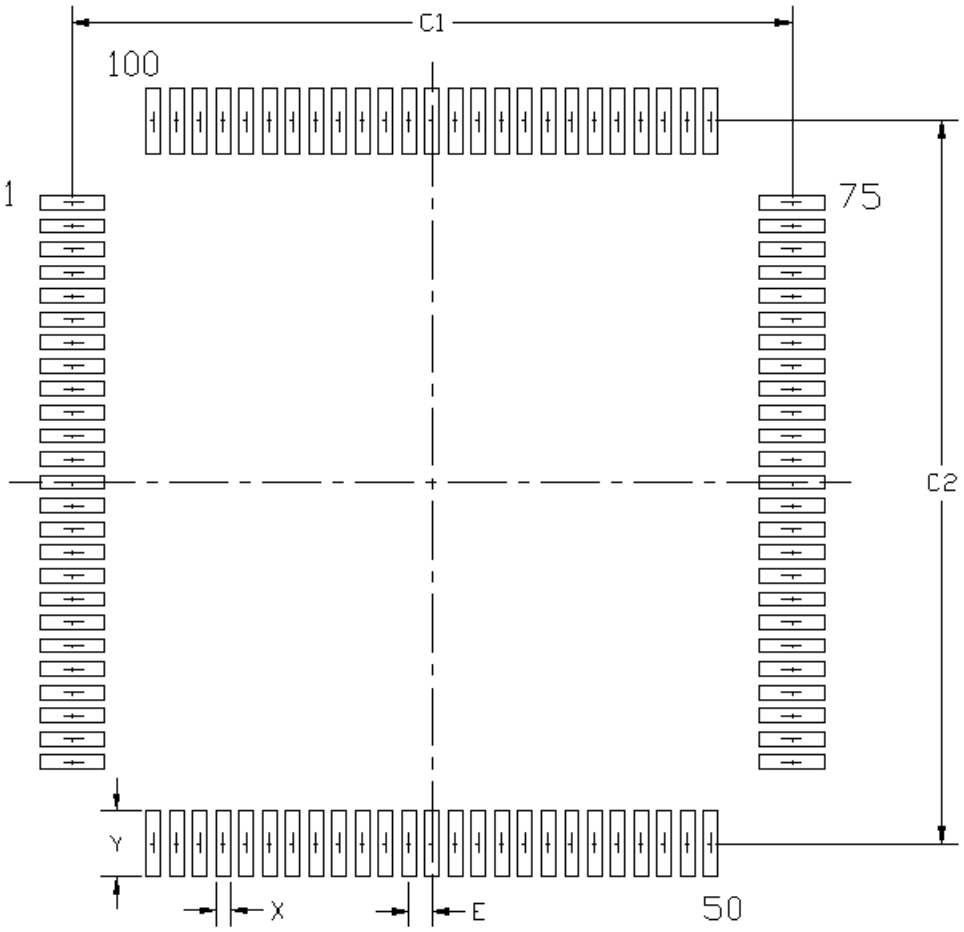

Figure 10.2. TQFP100 PCB Land Pattern Drawing

Table 11.2. TQFP64 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11.3 TQFP64 Package Marking

Figure 11.3. TQFP64 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

Table 12.1. QFN64 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.203 REF		
D	9.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

13. Revision History

Revision 0.6

March, 2018

- Removed "Confindential" watermark.
- Updated 4.1 Electrical Characteristics and 4.2 Typical Performance Curves with latest characterization data.

Revision 0.2

October, 2017

- Updated memory maps to latest formatting and to include all peripherals.
- Updated all electrical specifications tables with latest characterization results.
- **Absolute Maximum Ratings** Table:
  - Removed redundant I_{VSSMAX} line.
  - Added footnote to clarify V_{DIGPIN} specification for 5V tolerant GPIO.
- **General Operating Conditions** Table:
  - Removed dV_{DD} specification and redundant footnote about shorting VREGVDD and AVDD together.
  - Added footnote about IOVDD voltage restriction when CSEN peripheral is used with chopping enabled.
- **Flash Memory Characteristics** Table: Added timing measurement clarification for Device Erase and Mass Erase.
- **Analog to Digital Converter (ADC)** Table:
  - Added header text for general specification conditions.
  - Added footnote for clarification of input voltage limits.
- Minor typographical corrections, including capitalization, mis-spellings and punctuation marks, throughout document.
- Minor formatting and styling updates, including table formats, TOC location, and boilerplate information throughout document.

Revision 0.1

April 27th, 2017

Initial release.