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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b420f2048im64-a

Email: info@E-XFL.COM

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Figure 2.1. Ordering Code Key

4.1.10.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Frequency accuracy	f _{AUXHFRCO_ACC}	At production calibrated frequen- cies, across supply voltage and temperature	TBD	_	TBD	%
Start-up time	t _{AUXHFRCO}	f _{AUXHFRCO} ≥ 19 MHz	—	400	_	ns
		4 < f _{AUXHFRCO} < 19 MHz	—	1.4	_	μs
		f _{AUXHFRCO} ≤ 4 MHz	—	2.5		μs
Current consumption on all	IAUXHFRCO	f _{AUXHFRCO} = 50 MHz	—	289	TBD	μA
supplies		f _{AUXHFRCO} = 48 MHz	—	276	TBD	μA
		f _{AUXHFRCO} = 38 MHz	—	227	TBD	μA
		f _{AUXHFRCO} = 32 MHz	—	186	TBD	μA
		f _{AUXHFRCO} = 26 MHz	—	158	TBD	μA
		f _{AUXHFRCO} = 19 MHz	—	126	TBD	μA
		f _{AUXHFRCO} = 16 MHz	—	114	TBD	μA
		f _{AUXHFRCO} = 13 MHz	—	88	TBD	μA
		f _{AUXHFRCO} = 7 MHz	—	59	TBD	μA
		f _{AUXHFRCO} = 4 MHz	—	33	TBD	μA
		f _{AUXHFRCO} = 2 MHz	—	28	TBD	μA
		f _{AUXHFRCO} = 1 MHz	—	26	TBD	μA
Coarse trim step size (% of period)	SS _{AUXHFR-} CO_COARSE		_	0.8	_	%
Fine trim step size (% of pe- riod)	SS _{AUXHFR-} CO_FINE		—	0.1	_	%
Period jitter	PJ _{AUXHFRCO}			0.2		% RMS

Table 4.16. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Note: 1. ACMPVDD is a supply ch 2. The total ACMP current is I _{ACMPREF} . 3. ± 100 mV differential drive 4. In ACMPn_CTRL register 5. In ACMPn_HYSTERESIS 6. In ACMPn_INPUTSEL reg	osen by the s the sum of the c. registers. gister.	etting in ACMPn_CTRL_PWRS	EL and may be IOVDE and its internal voltage), AVDD or D\ e reference. I _A	VDD. Acmptotal = I	ACMP +

SDIO HS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Clock frequency during data transfer	F _{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	_	—	45	MHz
		Using HFXO	_	_	TBD	MHz
Clock low time	t _{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	10.0	_		ns
		Using HFXO	TBD	—	_	ns
Clock high time	t _{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	10.0	_	_	ns
		Using HFXO	TBD	_	_	ns
Clock rise time	t _R		1.69	3.23	_	ns
Clock fall time	t _F		1.42	2.79	_	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t _{ISU}		6	_		ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t _{IH}		2.5	_		ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	todly		0	—	13	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t _{OH}		2	—	—	ns

Table 4.47. SDIO HS Mode Timing (Location 0)





Figure 4.14. SDIO HS Mode Timing



Figure 4.19. SDIO MMC DDR Mode Timing



Figure 4.27. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 4.7 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz



Figure 4.29. DC-DC Converter Typical Performance Characteristics

PB2M3GPIOPB3M3GPIOPC6M1GPIOVRECVSM1value regulator VSSVREGWM4DCO regulator switching nodePB4N1GPIOPB5M2GPIOPD4M3GPIOPD5M1GPIOPD4M2GPIOPC0P1GPIO(SV)PA6P2GPIO(SV)PH1P5GPIO(SV)PH2P4GPIOPH2P1GPIO(SV)PH1P12GPIOPH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P14GPIO(SV)PH3P1GPIO(SV)PH1P14GPIO(SV)PH3P3GPIO(SV)PH1P14GPIO(SV)PH3P3GPIO(SV)PH1P14GPIO(SV)PH4P3GPIO(SV)PH2R2GPIO(SV)PH3P3GPIO(SV)PH3R4GPIO(SV)PH4S1GPIO(SV)GPICR2GPIO(SV)PS0R3GPIO(SV)GPISR4GPIO(SV)PS0R4GPIO(SV)GPISR4 <td< th=""><th>Pin Name</th><th>Pin(s)</th><th>Description</th><th>Pin Name</th><th>Pin(s)</th><th>Description</th></td<>	Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC6M14GPI0VREGVSM15Voltage regulator VSSVREGSWM16DCDC regulator switching nodePP84N1GPI0PB65N2GPI0PP80N3GPI0PD55N14GPI0PP10PP2GPI0PC0P1GPI0PP10PP2GPI0PC1P3GPI0PP10PP2GPI0PC2P3GPI0GPI0PP3GPI0PC1P4GPI0GPI0PP3GPI0PC2P3GPI0GPI0PP41GPI0PC3P3GPI0GPI0PP3GPI0PH3P16GPI0PP30PP3GPI0PH3P17GPI0GPI0PP40GPI0PH3P13GPI0PP10P11GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30R2GPI0PH3P13GPI0PP30R4GPI0PH3P13GPI0PP30R4GPI0P14P13GPI0PP30R4GPI0P15R14GPI0GP10R4GP10P16R13GPI0PP40R16GP10P17R13GPI0GP10R14GP10P14R14GP10GP10R14 <td< td=""><td>PB2</td><td>M2</td><td>GPIO</td><td>PB3</td><td>M3</td><td>GPIO</td></td<>	PB2	M2	GPIO	PB3	M3	GPIO
VREGSWM14DCD regulator switching nodePB4N1CPI0PB5N2GPI0PPB6N3GPI0PD5N14GPI0PD4N15GPI0PC0P3GPI0 (5V)PA1PA2GPI0PA1P5GPI0PA3P6GPI0PA1P5GPI0PA3P6GPI0P14P7GPI0 (5V)PH12P8GPI0P14P1GPI0 (5V)PH13P10GPI0 (5V)P14P1GPI0 (5V)PH14P12GPI0 (5V)P14P13GPI0 (5V)PH10P12GPI0 (5V)P143P13GPI0 (5V)PH10P14GPI0 (5V)P143P14GPI0 (5V)PH10P14GPI0 (5V)P143P15GPI0 (5V)PD0P14GPI0 (5V)P15GPI0 (5V)PD0P14GPI0 (5V)P16R1GPI0 (5V)GPI0 (5V)Restingut active low. To apply an extractive low. To apply an extractina	PC6	M14	GPIO	VREGVSS	M15 N16	Voltage regulator VSS
PB5N2GPIOPB6N3GPIOPD5N14GPIOPD4N15GPIOPC0P1GPIO (5V)PC1P2GPIO (5V)PC1P3GPIO (5V)PA8P4GPIO (5V)PB9P7GPIO (5V)PB12P8GPIO (5V)PH8P1GPIO (5V)PH10P12GPIO (5V)PH3P13GPIO (5V)PD0PH10P12GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3SP15GPIO (5V)PD0P14GPIO (5V)PD3P15GPIO (5V)PD0P14GPIO (5V)PD4N14GPIO (5V)PD1PA9R4PD5R3GPIO (5V)FPA9R4GPIO (5V)PD5R3GPIO (5V)PH4R4GPIO (5V)PH4R4GPIO (5V)PH4R14GPIO (5V)PH4R14GPIO (5V)PH10R14GPIO (5V)PH4R14GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH4R14GPIO (5V)PH4<	VREGSW	M16	DCDC regulator switching node	PB4	N1	GPIO
PD5N14GP0PD4N15GP10PC0P1GP10 (5V)PC1P2GP10 (5V)PC2P3GP10 (5V)PA8P4GP10 (5V)PB9P7GP10 (5V)PB12P8GP10 (5V)PH2P9GP10 (5V)PH11P12GP10 (5V)PH3P11GP10 (5V)PH11P12GP10 (5V)PH3P13GP10 (5V)PD0P14GP10 (5V)PH3P13GP10 (5V)PD0P14GP10 (5V)PH3P15GP10 (5V)PD0P14GP10 (5V)PB7R1GP10 (5V)PD0P14GP10 (5V)PB7R3GP10 - Controlled to failed to main extension may be of the single active tow. To apply an extend extension exten	PB5	N2	GPIO	PB6	N3	GPIO
PC0P1GPI0 (5V)PC1P2GPI0 (5V)PC2P3GPI0 (5V)PA8P4GPI0PA11P5GPI0 (5V)PA13P6GPI0 (5V)PB9P7GPI0 (5V)PB12P8GPI0 (5V)PH2P9GPI0 (5V)PH15P10GPI0 (5V)PH3P11GPI0 (5V)PH11P12GPI0 (5V)PH3P13GPI0 (5V)PH10P14GPI0 (5V)PH3P13GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0 (5V)PD0P14GPI0 (5V)PD3R1GPI0 (5V)PD3R2GPI0 (5V)PC5R3GPI0 (5V)PA9R4GPI0 (5V)PC5R3GPI0 (5V)PA9R4GPI0 (5V)BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to M20D.R68GPI0 (5V)PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH10R14GPI0 (5V)PH4R13GPI0 (5V)PH10R14GPI0 (5V)PH4R13GPI0 (5V)PH10R14GPI0 (5V)PH4R15GPI0 (5V)PA14T6GPI0PH4R13GPI0 (5V)PA14T6GPI0PH4R13GPI0 (5V)PA14T6GPI0 (5V)PH4T3GPI0 (5V) <td>PD5</td> <td>N14</td> <td>GPIO</td> <td>PD4</td> <td>N15</td> <td>GPIO</td>	PD5	N14	GPIO	PD4	N15	GPIO
PC2 P3 GPIO (5V) PA8 P4 GPIO PA11 P5 GPIO PA13 P6 GPIO (5V) PB9 P7 GPIO (5V) PB12 P8 GPIO PH2 P9 GPIO (5V) PH5 P10 GPIO PH3 P11 GPIO (5V) PH11 P12 GPIO (5V) PH3 P13 GPIO (5V) PD0 P14 GPIO (5V) PH3 P13 GPIO (5V) PD0 P14 GPIO (5V) PD3 P15 GPIO PD3 P15 GPIO (5V) PD3 P15 GPIO PC3 R2 GPIO (5V) PD5 R3 GPIO PA9 R4 GPIO BODEN R5 Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. RESETn R6 GPIO (5V) PB10 R7 GPIO (5V) PH0 R8 GPIO (5V) PH3 R9 GPIO (5V) PH10 R1 GPIO	PC0	P1	GPIO (5V)	PC1	P2	GPIO (5V)
PA11 P5 GPIO PA13 P6 GPIO (5V) PB9 P7 GPIO (5V) PB12 P8 GPIO PH2 P9 GPIO (5V) PH5 P10 GPIO PH8 P11 GPIO (5V) PH11 P12 GPIO (5V) PH3 P13 GPIO (5V) PD0 P14 GPIO (5V) PD3 P15 GPIO (5V) PD0 P14 GPIO (5V) PD3 P15 GPIO PD3 P15 GPIO PD4 PB7 R1 GPIO PC3 R2 GPIO (5V) PC5 R3 GPIO PA9 R4 GPIO BODEN R5 Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. RESETn R6 Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and left the internal pul-upensure that reset is released. PB10 R7 GPIO (5V) PH0 R8 GPIO (5V) PH3 R9 GPIO (5V) P	PC2	P3	GPIO (5V)	PA8	P4	GPIO
PB9P7GPIO (5V)PB12P8GPIOPH2P9GPIO (5V)PH5P10GPIOPH8P11GPIO (5V)PD11P12GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD2P23R2GPIO (5V)PB7R1GPIOPA9R4GPIOPC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin wyb be left disconnected or tied to AVDD.RESETNR6Reset input, active low. To apply an ex- terral reset source to this pin, it is re- arrest only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIOPH4R13GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PD7R16GPIOPH4T3GPIO (5V)PA14T6GPIOPH4T3GPIO (5V)PA14T6GPIOPH4T3GPIO (5V)PH11T8GPIO (5V)PH4T9GPIO (5V)PH41T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH3T12GPIOPH4T13GPIO (5V)PH3T12GPIOPH4T14GPIO (5V)PH3	PA11	P5	GPIO	PA13	P6	GPIO (5V)
PH2P9GPI0 (5V)PH5P10GPI0PH8P11GPI0 (5V)PH11P12GPI0 (5V)PH3P13GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0PD0P14GPI0 (5V)PB7R1GPI0PC3R2GPI0 (5V)PC5R3GPI0PA9R4GPI0BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin out during reset, and let the internal pull-up ensure that reset is released.PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH6R10GPI0PH4R13GPI0 (5V)PH12R12GPI0 (5V)PH4R13GPI0 (5V)PH15R14GPI0 (5V)PH4R13GPI0 (5V)PD7R16GPI0PH3T1GPI0 (5V)PD7R16GPI0PH4T3GPI0 (5V)PA14T6GPI0PH4T3GPI0 (5V)PA14T6GPI0PH4T7GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T1GPI0 (5V)PB13T12GPI0PH4<	PB9	P7	GPIO (5V)	PB12	P8	GPIO
PH8P11GPIO (5V)PH11P12GPIO (5V)PH13P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD8P16GPIOPB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENRsBrown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETNR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and left the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIOPH4R13GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPA3T3GPIO (5V)PD7R16GPIOPH4R13GPIO (5V)PD7R16GPIOPH4R13GPIO (5V)PD7R16GPIOPA7T3GPIOPA14T6GPIOPA11T7GPIOPH1T8GPIO (5V)PH4T9GPIO (5V)PH1T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH3T12GPIOPH4T9GPIOAVDDAVDDT	PH2	P9	GPIO (5V)	PH5	P10	GPIO
PH13P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD8P16GPIOPB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPA7T3GPIO (5V)PA14T6GPIOPA12T5GPIO (5V)PA14T6GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH3T12GPIOPH4T9GPIO (5V)PH3T12GPIOPH4T13GPIOAVDDT14Analog power supply.PH4T15GPIO <td>PH8</td> <td>P11</td> <td>GPIO (5V)</td> <td>PH11</td> <td>P12</td> <td>GPIO (5V)</td>	PH8	P11	GPIO (5V)	PH11	P12	GPIO (5V)
PD3P15GPI0PD8P16GPI0PB7R1GPI0PC3R2GPI0 (5V)PC5R3GPI0PA9R4GPI0BC5R3GPI0PA9R4GPI0BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnReset input, active low. To apply an ex- ternal reset source to this pin, it is re- quied to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH6R10GPI0PH3R9GPI0 (5V)PH6R10GPI0 (5V)PH3R1GPI0 (5V)PH12R12GPI0 (5V)PH4R13GPI0 (5V)PH15R14GPI0 (5V)PD2R15GPI0 (5V)PD7R16GPI0PB8T1GPI0PA10T4GPI0PA12T5GPI0 (5V)PA14T6GPI0PA14T9GPI0 (5V)PH1T8GPI0 (5V)PH4T9GPI0 (5V)PB13T12GPI0PH4T13GPI0 (5V)PB13T12GPI0PB14T13GPI0AVDDT14Analog power supply.PB14T15GPI0PD6T16GPI0	PH13	P13	GPIO (5V)	PD0	P14	GPIO (5V)
PB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnReset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R13GPIO (5V)PH15R14GPIO (5V)PH14R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPA12T5GPIO (5V)PA14T6GPIOPH14T9GPIO (5V)PH1T10GPIO (5V)PH14T1GPIO (5V)PA14T6GPIOPH15T11GPIO (5V)PA14T6GPIOPH10T11GPIO (5V)PH1T10GPIO (5V)PH14T9GPIO (5V)PH3T12GPIOPH4T9GPIO (5V)PH3T12GPIOPH10T11GPIO (5V)PH3T12GPIOPH10T11GPIO (5V)PH3T14 </td <td>PD3</td> <td>P15</td> <td>GPIO</td> <td>PD8</td> <td>P16</td> <td>GPIO</td>	PD3	P15	GPIO	PD8	P16	GPIO
PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIO (5V)PH4R11GPIO (5V)PH6R10GPIO (5V)PH4R13GPIO (5V)PH12R12GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PD7R16GPIOPA7T3GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PH3T12GPIOPH10T11GPIO (5V)PH6T14Analog power supply.PB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PB7	R1	GPIO	PC3	R2	GPIO (5V)
BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- termal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensurePB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R1GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PD7R16GPIOPA12T5GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PB13T12GPIOPH10T11GPIO (5V)PB13T12GPIOPB14T13GPIO (5V)PD6T16GPIOPD1T15GPIOPD6T16GPIO	PC5	R3	GPIO	PA9	R4	GPIO
PB10 R7 GPIO (5V) PH0 R8 GPIO (5V) PH3 R9 GPIO (5V) PH6 R10 GPIO PH9 R11 GPIO (5V) PH12 R12 GPIO (5V) PH14 R13 GPIO (5V) PH12 R14 GPIO (5V) PD14 R13 GPIO (5V) PH12 R14 GPIO (5V) PD2 R15 GPIO (5V) PD7 R16 GPIO PD2 R15 GPIO (5V) PD7 R16 GPIO PB8 T1 GPIO (5V) PD7 R16 GPIO PB4 T3 GPIO (5V) PC4 T2 GPIO PA12 T5 GPIO (5V) PA14 T6 GPIO PB11 T7 GPIO (5V) PH1 T8 GPIO (5V) PH4 T9 GPIO (5V) PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14	BODEN	R5	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	RESETn	R6	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PH3R9GPIO (5V)PH6R10GPIOPH9R11GPIO (5V)PH12R12GPIO (5V)PH14R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIO (5V)PB8T1GPIO (5V)PC4T2GPIOPA7T3GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PB10	R7	GPIO (5V)	PH0	R8	GPIO (5V)
PH9 R11 GPIO (5V) PH12 R12 GPIO (5V) PH14 R13 GPIO (5V) PH15 R14 GPIO (5V) PD2 R15 GPIO (5V) PD7 R16 GPIO PB8 T1 GPIO (5V) PC4 T2 GPIO PA7 T3 GPIO PA10 T4 GPIO PA12 T5 GPIO (5V) PA10 T4 GPIO PA12 T5 GPIO (5V) PA14 T6 GPIO PB11 T7 GPIO PH1 T8 GPIO (5V) PH10 T1 GPIO PH1 T8 GPIO (5V) PH4 T9 GPIO PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH3	R9	GPIO (5V)	PH6	R10	GPIO
PH14 R13 GPIO (5V) PH15 R14 GPIO (5V) PD2 R15 GPIO (5V) PD7 R16 GPIO PB8 T1 GPIO (5V) PC4 T2 GPIO PA7 T3 GPIO (5V) PA10 T4 GPIO PA12 T5 GPIO (5V) PA14 T6 GPIO PB11 T7 GPIO (5V) PA14 T6 GPIO (5V) PH44 T9 GPIO (5V) PH1 T8 GPIO (5V) PH4 T9 GPIO (5V) PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO (5V) AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH9	R11	GPIO (5V)	PH12	R12	GPIO (5V)
PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIOPC4T2GPIOPA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PH14	R13	GPIO (5V)	PH15	R14	GPIO (5V)
PB8T1GPIOPC4T2GPIOPA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PD2	R15	GPIO (5V)	PD7	R16	GPIO
PA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PB8	T1	GPIO	PC4	T2	GPIO
PA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PA7	Т3	GPIO	PA10	T4	GPIO
PB11 T7 GPIO PH1 T8 GPIO (5V) PH4 T9 GPIO PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PA12	T5	GPIO (5V)	PA14	Т6	GPIO
PH4 T9 GPIO PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PB11	T7	GPIO	PH1	Т8	GPIO (5V)
PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH4	Т9	GPIO	PH7	T10	GPIO (5V)
PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH10	T11	GPIO (5V)	PB13	T12	GPIO
PD1 T15 GPIO PD6 T16 GPIO	PB14	T13	GPIO	AVDD	T14	Analog power supply.
	PD1	T15	GPIO	PD6	T16	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 59 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	v. To apply an ex- this pin, it is re- is pin low during PB9 37 GPIO (5V) nal pull-up ensure		GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	45	GPIO (5V)	PD1	46	GPIO
PD2	47	GPIO (5V)	PD3	48	GPIO
PD4	49	GPIO	PD5	50	GPIO
PD6	51	GPIO	PD7	52	GPIO
PD8	53	GPIO	PC7	54	GPIO
VREGVSS	55	Voltage regulator VSS	VREGSW	56	DCDC regulator switching node
VREGVDD	57	Voltage regulator VDD input	DVDD	58	Digital power supply.
DECOUPLE	60	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE1	61	GPIO (5V)
PE2	62	GPIO	PE3	63	GPIO
PE4	64	GPIO	PE5	65	GPIO
PE6	66	GPIO	PE7	67	GPIO
PC8	68	GPIO (5V)	PC9	69	GPIO (5V)
PC10	70	GPIO (5V)	PC11	71	GPIO (5V)
VREGI	72	Input to 5 V regulator.	VREGO	73	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs
PF10	74	GPIO (5V)	PF11	75	GPIO (5V)
PF0	76	GPIO (5V)	PF1	77	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA12	17	GPIO (5V)	PA13	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	VREGI	45	Input to 5 V regulator.
VREGO	46	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs	PF10	47	GPIO (5V)
PF11	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			
Note:			_		

1. GPIO with 5V tolerance are indicated by (5V).



Figure 5.17. EFM32GG11B5xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA12	18	GPIO (5V)	PA13	19	GPIO (5V)
PA14	20	GPIO	RESETn	21	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	22	GPIO	PB12	23	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD7	35	GPIO	PD8	36	GPIO
PC7	37	GPIO	VREGVSS	38	Voltage regulator VSS
VREGSW	39	DCDC regulator switching node	VREGVDD	40	Voltage regulator VDD input
DVDD	41	Digital power supply.	DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling ca-pacitor is required at this pin.
PE4	43	GPIO	PE5	44	GPIO
PE6	45	GPIO	PE7	46	GPIO
PC12	47	GPIO (5V)	PC13	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	PF3	52	GPIO
PF4	53	GPIO	PF5	54	GPIO
PE8	56	GPIO	PE9	57	GPIO
PE10	58	GPIO	PE11	59	GPIO
PE12	60	GPIO	PE13	61	GPIO
PE14	62	GPIO	PE15	63	GPIO
PA15	64	GPIO			
Note:					

1. GPIO with 5V tolerance are indicated by (5V).

5.20 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 5.21 Alternate Functionality Overview for a list of GPIO locations available for each function.

GPIO Name	Pin Alternate Functionality / Description					
	Analog	EBI	Timers	Communication	Other	
PA15	BUSAY BUSBX LCD_SEG12	EBI_AD08 #0	TIM3_CC2 #0	ETH_MIIRXCLK #0 ETH_MDIO #3 US2_CLK #3	PRS_CH15 #0	
PE15	BUSCY BUSDX LCD_SEG11	EBI_AD07 #0	TIM2_CDTI2 #2 TIM3_CC1 #0	ETH_RMIITXD0 #0 ETH_MIIRXD3 #0 SDIO_CMD #1 US0_RTS #0 QSPI0_DQS #1 LEU0_RX #2	PRS_CH14 #2 ETM_TD3 #4	
PE14	BUSDY BUSCX LCD_SEG10	EBI_AD06 #0	TIM2_CDTI1 #2 TIM3_CC0 #0	ETH_RMIITXD1 #0 ETH_MIIRXD2 #0 SDIO_CLK #1 US0_CTS #0 QSPI0_SCLK #1 LEU0_TX #2	PRS_CH13 #2 ETM_TD2 #4	
PE13	BUSCY BUSDX LCD_SEG9	EBI_AD05 #0	TIM1_CC3 #1 TIM2_CC2 #3 LE- TIM0_OUT1 #4	SDIO_CLK #0 ETH_MIIRXD1 #0 US0_TX #3 US0_CS #0 U1_RX #4 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 ETM_TD1 #4 GPIO_EM4WU5	
PE12	BUSDY BUSCX LCD_SEG8	EBI_AD04 #0	TIM1_CC2 #1 TIM2_CC1 #3 WTIM0_CDTI2 #0 LETIM0_OUT0 #4	SDIO_CMD #0 ETH_MIIRXD0 #0 US0_RX #3 US0_CLK #0 U1_TX #4 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_ALTEX6 PRS_CH1 #3 ETM_TD0 #4	
PE11	BUSCY BUSDX LCD_SEG7	EBI_AD03 #0 EBI_CS3 #4	TIM1_CC1 #1 TIM4_CC2 #7 WTIM0_CDTI1 #0	SDIO_DAT0 #0 QSPI0_DQ7 #0 ETH_MIIRXDV #0 US0_RX #0	LES_ALTEX5 PRS_CH3 #2 ETM_TCLK #4	
PE10	BUSDY BUSCX LCD_SEG6	EBI_AD02 #0 EBI_CS2 #4	TIM1_CC0 #1 TIM4_CC1 #7 WTIM0_CDTI0 #0	SDIO_DAT1 #0 QSPI0_DQ6 #0 ETH_MIIRXER #0 US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9	
PE9	BUSCY BUSDX LCD_SEG5	EBI_AD01 #0 EBI_CS1 #4	TIM4_CC0 #7 PCNT2_S1IN #1	SDIO_DAT2 #0 QSPI0_DQ5 #0 US5_RX #0	PRS_CH8 #2	
PE8	BUSDY BUSCX LCD_SEG4	EBI_AD00 #0 EBI_CS0 #4	TIM2_CDTI0 #2 TIM4_CC2 #6 PCNT2_S0IN #1	SDIO_DAT3 #0 QSPI0_DQ4 #0 US5_TX #0 I2C2_SDA #0	PRS_CH3 #1	
PI9		EBI_A14 #2	TIM1_CC3 #7 TIM4_CC1 #3	US4_CS #3		
PI6		EBI_A11 #2	TIM1_CC0 #7 TIM4_CC1 #2 WTIM3_CC0 #5	US4_TX #3		

Table 5.20. GPIO Functionality Table

Alternate	LOCA				
Functionality	0 - 3	4 - 7	Description		
ETH_MDIO	0: PB3 1: PD13 2: PC0 3: PA15		Ethernet Management Data I/O.		
ETH_MIICOL	0: PB2 1: PG15 2: PB4		Ethernet MII Collision Detect.		
ETH_MIICRS	0: PB1 1: PG14 2: PB3		Ethernet MII Carrier Sense.		
ETH_MIRXCLK	0: PA15 1: PG7 2: PD12		Ethernet MII Receive Clock.		
ETH_MIRXD0	0: PE12 1: PG11 2: PF9		Ethernet MII Receive Data Bit 0.		
ETH_MIIRXD1	0: PE13 1: PG10 2: PD9		Ethernet MII Receive Data Bit 1.		
ETH_MIIRXD2	0: PE14 1: PG9 2: PD10		Ethernet MII Receive Data Bit 2.		
ETH_MIIRXD3	0: PE15 1: PG8 2: PD11		Ethernet MII Receive Data Bit 3.		
ETH_MIIRXDV	0: PE11 1: PG12 2: PF8		Ethernet MII Receive Data Valid.		
ETH_MIIRXER	0: PE10 1: PG13 2: PF7		Ethernet MII Receive Error.		
ETH_MIITXCLK	0: PA0 1: PG0		Ethernet MII Transmit Clock.		
ETH_MIITXD0	0: PA4 1: PG4		Ethernet MII Transmit Data Bit 0.		
ETH_MIITXD1	0: PA3 1: PG3		Ethernet MII Transmit Data Bit 1.		

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_CH11	0: PC11		LESENSE channel 11.
LES_CH12	0: PC12		LESENSE channel 12.
LES_CH13	0: PC13		LESENSE channel 13.
LES_CH14	0: PC14		LESENSE channel 14.
LES_CH15	0: PC15		LESENSE channel 15.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8 7: PB9	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9 7: PB10	Low Energy Timer LETIM0, output channel 1.
LETIM1_OUT0	0: PA7 1: PA11 2: PA12 3: PC2	4: PB5 5: PB2 6: PG0 7: PG2	Low Energy Timer LETIM1, output channel 0.
LETIM1_OUT1	0: PA6 1: PA13 2: PA14 3: PC3	4: PB6 5: PB1 6: PG1 7: PG3	Low Energy Timer LETIM1, output channel 1.
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	0: PC7 1: PA6 2: PD3 3: PB1	4: PB5 5: PH1	LEUART1 Receive input.
LEU1_TX	0: PC6 1: PA5 2: PD2 3: PB0	4: PB4 5: PH0	LEUART1 Transmit output. Also used as receive input in half duplex communication.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM3_CC2	0: PD11 1: PC10 2: PC13 3: PF11	4: PI5 5: PF6 6: PF12 7: PF15	Wide timer 3 Capture Compare input / output channel 2.

Certain alternate function locations may have non-interference priority. These locations will take precedence over any other functions selected on that pin (i.e. another alternate function enabled to the same pin inadvertently).

Some alternate functions may also have high speed priority on certain locations. These locations ensure the fastest possible paths to the pins for timing-critical signals.

The following table lists the alternate functions and locations with special priority.

Table 5.22. Alternate Functionality Priority

Alternate Functionality	Location	Priority
CMU_CLK2	1: PA3 5: PD10	High Speed High Speed
CMU_CLKI0	1: PA3 5: PD10	High Speed High Speed
ETH_RMIICRSDV	0: PA4 1: PD11	High Speed High Speed
ETH_RMIIREFCLK	0: PA3 1: PD10	High Speed High Speed
ETH_RMIIRXD0	0: PA2 1: PD9	High Speed High Speed
ETH_RMIIRXD1	0: PA1 1: PF9	High Speed High Speed
ETH_RMIIRXER	0: PA5 1: PD12	High Speed High Speed
ETH_RMIITXD0	0: PE15 1: PF7	High Speed High Speed
ETH_RMIITXD1	0: PE14 1: PF6	High Speed High Speed
ETH_RMIITXEN	0: PA0 1: PF8	High Speed High Speed
QSPI0_CS0	0: PF7	High Speed
QSPI0_CS1	0: PF8	High Speed
QSPI0_DQ0	0: PD9	High Speed
QSPI0_DQ1	0: PD10	High Speed
QSPI0_DQ2	0: PD11	High Speed
QSPI0_DQ3	0: PD12	High Speed
QSPI0_DQ4	0: PE8	High Speed
QSPI0_DQ5	0: PE9	High Speed
QSPI0_DQ6	0: PE10	High Speed
QSPI0_DQ7	0: PE11	High Speed

Table 7.2. BGA152 PCB Land Pattern Dimensions

Dimension	Min	Nom	Мах	
X	0.20			
C1	6.50			
C2	6.50			
E1	0.5			
E2	0.5			

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.

3. This Land Pattern Design is based on the IPC-7351 guidelines.

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

6. The stencil thickness should be 0.125 mm (5 mils).

7. The ratio of stencil aperture to land pad size should be 1:1.

8. A No-Clean, Type-3 solder paste is recommended.

9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.



Figure 7.3. BGA152 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.

Dimension	Min	Тур	Мах	
A	-	-	1.30	
A1	0.55	0.60	0.65	
A2	0.21 BSC			
A3	0.30	0.35	0.40	
d	0.43	0.48	0.53	
D	10.00 BSC			
D1	8.00 BSC			
E	10.00 BSC			
E1	8.00 BSC			
e1	0.80 BSC			
e2	0.80 BSC			
L1	1.00 REF			
L2	1.00 REF			

Table 9.1. BGA112 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.