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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b420f2048iq100-ar

1. Feature List

The EFM32GG11 highlighted features are listed below.

- **ARM Cortex-M4 CPU platform**
 - High performance 32-bit processor @ up to 72 MHz
 - DSP instruction support and Floating Point Unit
 - Memory Protection Unit
 - Wake-up Interrupt Controller
- **Flexible Energy Management System**
 - 80 μ A/MHz in Active Mode (EM0)
 - 2.1 μ A EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Up to 2048 kB flash program memory**
 - Dual-bank with read-while-write support
- **Up to 512 kB RAM data memory**
 - 256 kB with ECC (SEC-DED)
- **Octal/Quad-SPI Flash Memory Interface**
 - Supports 3 V and 1.8 V memories
 - 1/2/4/8-bit data bus
 - Quad-SPI Execute In Place (XIP)
- **Communication Interfaces**
 - Low-energy Universal Serial Bus (USB) with Device and Host support
 - Fully USB 2.0 compliant
 - On-chip PHY and embedded 5V to 3.3V regulator
 - Crystal-free Device mode operation
 - Patent-pending Low-Energy Mode (LEM)
 - SD/MMC/SDIO Host Controller
 - SD v3.01, SDIO v3.0 and MMC v4.51
 - 1/4/8-bit bus width
 - 10/100 Ethernet MAC with MII/RMII interface
 - IEEE1588-2008 precision time stamping
 - Energy Efficient Ethernet (802.3az)
 - Up to 2 \times CAN Bus Controller
 - Version 2.0A and 2.0B up to 1 Mbps
 - 6 \times Universal Synchronous/Asynchronous Receiver/ Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
 - Triple buffered full/half-duplex operation with flow control
 - Ultra high speed (36 MHz) operation on one instance
 - 2 \times Universal Asynchronous Receiver/ Transmitter
 - 2 \times Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - 3 \times I²C Interface with SMBus support
 - Address recognition in EM3 Stop Mode
- **Up to 144 General Purpose I/O Pins**
 - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - 5 V tolerance on select pins
 - Asynchronous external interrupts
 - Output state retention and wake-up from Shutoff Mode
- **Up to 24 Channel DMA Controller**
- **Up to 24 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **External Bus Interface for up to 4x256 MB of external memory mapped space**
 - TFT Controller with Direct Drive
 - Per-pixel alpha-blending engine
- **Hardware Cryptography**
 - AES 128/256-bit keys
 - ECC B/K163, B/K233, P192, P224, P256
 - SHA-1 and SHA-2 (SHA-224 and SHA-256)
 - True Random Number Generator (TRNG)
- **Hardware CRC engine**
 - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
 - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8 \times 36 segments**
 - Voltage boost, contrast and autonomous animation
 - Patented low-energy LCD driver
- **Backup Power Domain**
 - RTCC and retention registers in a separate power domain, available down to energy mode EM4H
 - Operation from backup battery when main power absent/insufficient
- **Ultra Low-Power Precision Analog Peripherals**
 - 2 \times 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
 - On-chip temperature sensor
 - 2 \times 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
 - Digital to Analog Current Converter (IDAC)
 - Up to 4 \times Analog Comparator (ACMP)
 - Up to 4 \times Operational Amplifier (OPAMP)
 - Robust current-based capacitive sensing with up to 64 inputs and wake-on-touch (CSEN)
 - Up to 108 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
 - Supply Voltage Monitor

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3.4.2 Internal and External Oscillators

The EFM32GG11 supports two crystal oscillators and fully integrates five RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 50 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated auxiliary high frequency RC oscillator (USHFRCO) is available for timing the USB, SDIO and QSPI peripherals. The USHFRCO can be synchronized to the host's USB clock to allow the USB to operate in device mode without the additional cost of an external crystal.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode ³	I _{ACTIVE_LPM}	32 MHz HFRCO, CPU running while loop from flash	—	82	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	83	—	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	88	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	257	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode ¹	I _{ACTIVE_CCM_VS}	19 MHz HFRCO, CPU running while loop from flash	—	117	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1231	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode ³	I _{ACTIVE_LPM_VS}	19 MHz HFRCO, CPU running while loop from flash	—	72	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	219	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode ²	I _{EM1_DCM}	72 MHz HFRCO	—	42	—	μA/MHz
		50 MHz crystal	—	46	—	μA/MHz
		48 MHz HFRCO	—	46	—	μA/MHz
		32 MHz HFRCO	—	53	—	μA/MHz
		26 MHz HFRCO	—	57	—	μA/MHz
		16 MHz HFRCO	—	72	—	μA/MHz
		1 MHz HFRCO	—	663	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode ³	I _{EM1_LPM}	32 MHz HFRCO	—	42	—	μA/MHz
		26 MHz HFRCO	—	43	—	μA/MHz
		16 MHz HFRCO	—	48	—	μA/MHz
		1 MHz HFRCO	—	219	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode ²	I _{EM1_DCM_VS}	19 MHz HFRCO	—	60	—	μA/MHz
		1 MHz HFRCO	—	637	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode ³	I _{EM1_LPM_VS}	19 MHz HFRCO	—	39	—	μA/MHz
		1 MHz HFRCO	—	190	—	μA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode ³	I _{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	2.8	—	μA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	3.1	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO ⁵	—	2.1	—	μA
Current consumption in EM3 mode, with voltage scaling enabled	I _{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFR-CO	—	2.4	—	μA

4.1.10.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.13. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}	No clock doubling	4	—	50	MHz
		Clock doubler enabled	TBD	—	TBD	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	50 MHz crystal	—	—	50	Ω
		24 MHz crystal	—	—	150	Ω
		4 MHz crystal	—	—	180	Ω
Nominal on-chip tuning cap range ¹	$C_{\text{HFXO_T}}$	On each of HFXTAL_N and HFXTAL_P pins	8.7	—	51.7	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.084	—	pF
Startup time	t_{HFXO}	50 MHz crystal, ESR = 50 Ohm, $C_L = 8$ pF	—	350	—	μs
		24 MHz crystal, ESR = 150 Ohm, $C_L = 6$ pF	—	700	—	μs
		4 MHz crystal, ESR = 180 Ohm, $C_L = 18$ pF	—	3	—	ms
Current consumption after startup	I_{HFXO}	50 MHz crystal	—	880	—	μA
		24 MHz crystal	—	420	—	μA
		4 MHz crystal	—	80	—	μA

Note:

1. The effective load capacitance seen by the crystal will be $C_{\text{HFXO_T}}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.1.13 Voltage Monitor (VMON)

Table 4.21. Voltage Monitor (VMON)

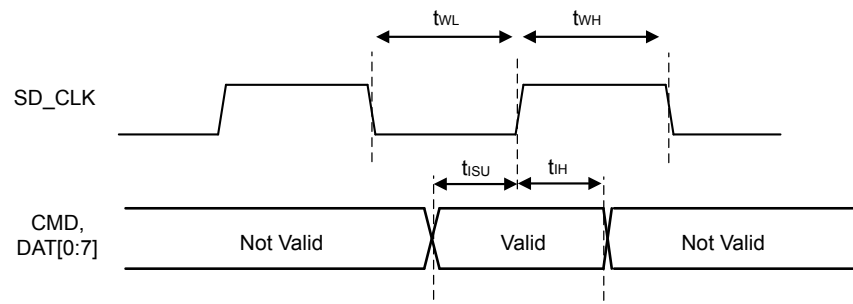
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I _{SENSE})	I _{VMON}	In EM0 or EM1, 1 supply monitored, T ≤ 85 °C	—	6.0	TBD	μA
		In EM0 or EM1, 4 supplies monitored, T ≤ 85 °C	—	14.9	TBD	μA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I _{SENSE}	In EM0 or EM1	—	2	—	μA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V _{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N _{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t _{VMON_RES}	Supply drops at 1V/μs rate	—	460	—	ns
Hysteresis	V _{VMON_HYST}		—	26	—	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	f_{ADCRATE}		—	—	1	Msp/s
Conversion time ¹	t_{ADCCONV}	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	t_{ADCSTART}	WARMUPMODE ⁴ = NORMAL	—	—	5	μs
		WARMUPMODE ⁴ = KEEPIN-STANDBY	—	—	2	μs
		WARMUPMODE ⁴ = KEEPINSLOWACC	—	—	1	μs
SNDR at 1Msp/s and $f_{\text{IN}} = 10\text{kHz}$	SNDR_{ADC}	Internal reference ⁷ , differential measurement	TBD	67	—	dB
		External reference ⁶ , differential measurement	—	68	—	dB
Spurious-free dynamic range (SFDR)	SFDR_{ADC}	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing codes	TBD	—	TBD	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	TBD	—	TBD	LSB
Offset error	$V_{\text{ADCOFFSETERR}}$		TBD	0	TBD	LSB
Gain error in ADC	V_{ADCGAIN}	Using internal reference	—	-0.2	TBD	%
		Using external reference	—	-1	—	%
Temperature sensor slope	$V_{\text{TS_SLOPE}}$		—	-1.84	—	mV/°C

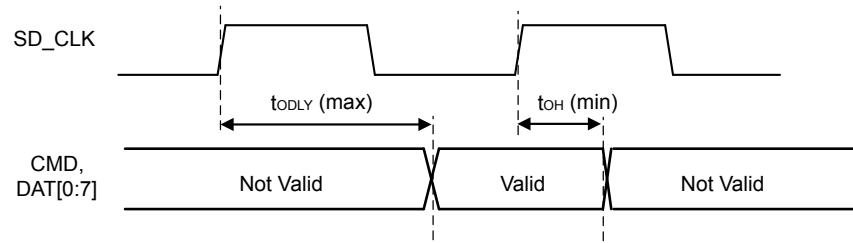
Note:

1. Derived from ADCCLK.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_BIASPROG register.
4. In ADCn_CNTL register.
5. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
6. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is $\pm 1.25\text{ V}$.
7. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is $\pm 1.25\text{ V}$. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: <ol style="list-style-type: none"> 1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD. 2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$. 3. ± 100 mV differential drive. 4. In ACMPn_CTRL register. 5. In ACMPn_HYSTERESIS registers. 6. In ACMPn_INPUTSEL register. 						

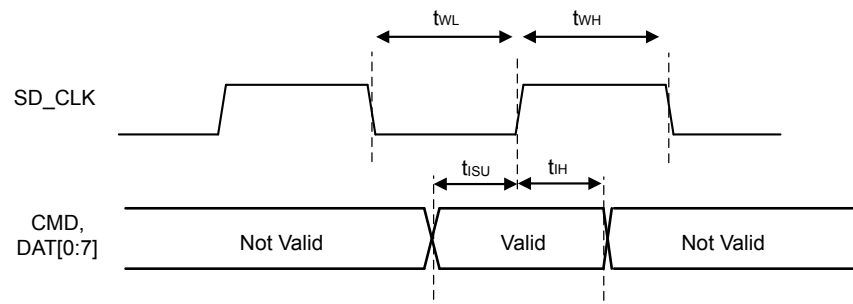


Input Timing

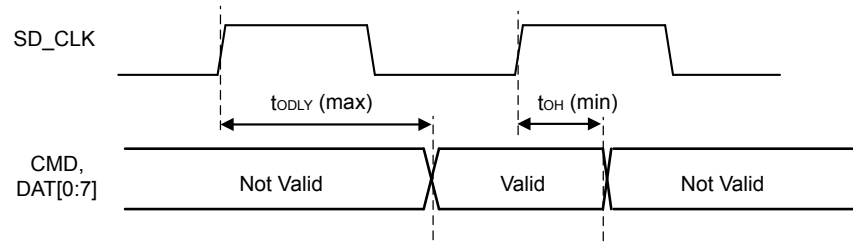


Output Timing

Figure 4.15. SDIO SDR Mode Timing



Input Timing



Output Timing

Figure 4.18. SDIO MMC SDR Mode Timing

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	M2	GPIO	PB3	M3	GPIO
PC6	M14	GPIO	VREGVSS	M15 N16	Voltage regulator VSS
VREGSW	M16	DCDC regulator switching node	PB4	N1	GPIO
PB5	N2	GPIO	PB6	N3	GPIO
PD5	N14	GPIO	PD4	N15	GPIO
PC0	P1	GPIO (5V)	PC1	P2	GPIO (5V)
PC2	P3	GPIO (5V)	PA8	P4	GPIO
PA11	P5	GPIO	PA13	P6	GPIO (5V)
PB9	P7	GPIO (5V)	PB12	P8	GPIO
PH2	P9	GPIO (5V)	PH5	P10	GPIO
PH8	P11	GPIO (5V)	PH11	P12	GPIO (5V)
PH13	P13	GPIO (5V)	PD0	P14	GPIO (5V)
PD3	P15	GPIO	PD8	P16	GPIO
PB7	R1	GPIO	PC3	R2	GPIO (5V)
PC5	R3	GPIO	PA9	R4	GPIO
BODEN	R5	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	RESETn	R6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB10	R7	GPIO (5V)	PH0	R8	GPIO (5V)
PH3	R9	GPIO (5V)	PH6	R10	GPIO
PH9	R11	GPIO (5V)	PH12	R12	GPIO (5V)
PH14	R13	GPIO (5V)	PH15	R14	GPIO (5V)
PD2	R15	GPIO (5V)	PD7	R16	GPIO
PB8	T1	GPIO	PC4	T2	GPIO
PA7	T3	GPIO	PA10	T4	GPIO
PA12	T5	GPIO (5V)	PA14	T6	GPIO
PB11	T7	GPIO	PH1	T8	GPIO (5V)
PH4	T9	GPIO	PH7	T10	GPIO (5V)
PH10	T11	GPIO (5V)	PB13	T12	GPIO
PB14	T13	GPIO	AVDD	T14	Analog power supply.
PD1	T15	GPIO	PD6	T16	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 58 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB9	37	GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41 45	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	46	GPIO (5V)	PD1	47	GPIO
PD2	48	GPIO (5V)	PD3	49	GPIO
PD4	50	GPIO	PD5	51	GPIO
PD6	52	GPIO	PD7	53	GPIO
PD8	54	GPIO	PC6	55	GPIO
PC7	56	GPIO	DVDD	57	Digital power supply.
DECOUPLE	59	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE0	60	GPIO (5V)
PE1	61	GPIO (5V)	PE2	62	GPIO
PE3	63	GPIO	PE4	64	GPIO
PE5	65	GPIO	PE6	66	GPIO
PE7	67	GPIO	PC8	68	GPIO (5V)
PC9	69	GPIO (5V)	PC10	70	GPIO (5V)
PC11	71	GPIO (5V)	VREGI	72	Input to 5 V regulator.
VREGO	73	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs	PF10	74	GPIO (5V)
PF11	75	GPIO (5V)	PF0	76	GPIO (5V)

5.12 EFM32GG11B8xx in QFP64 Device Pinout

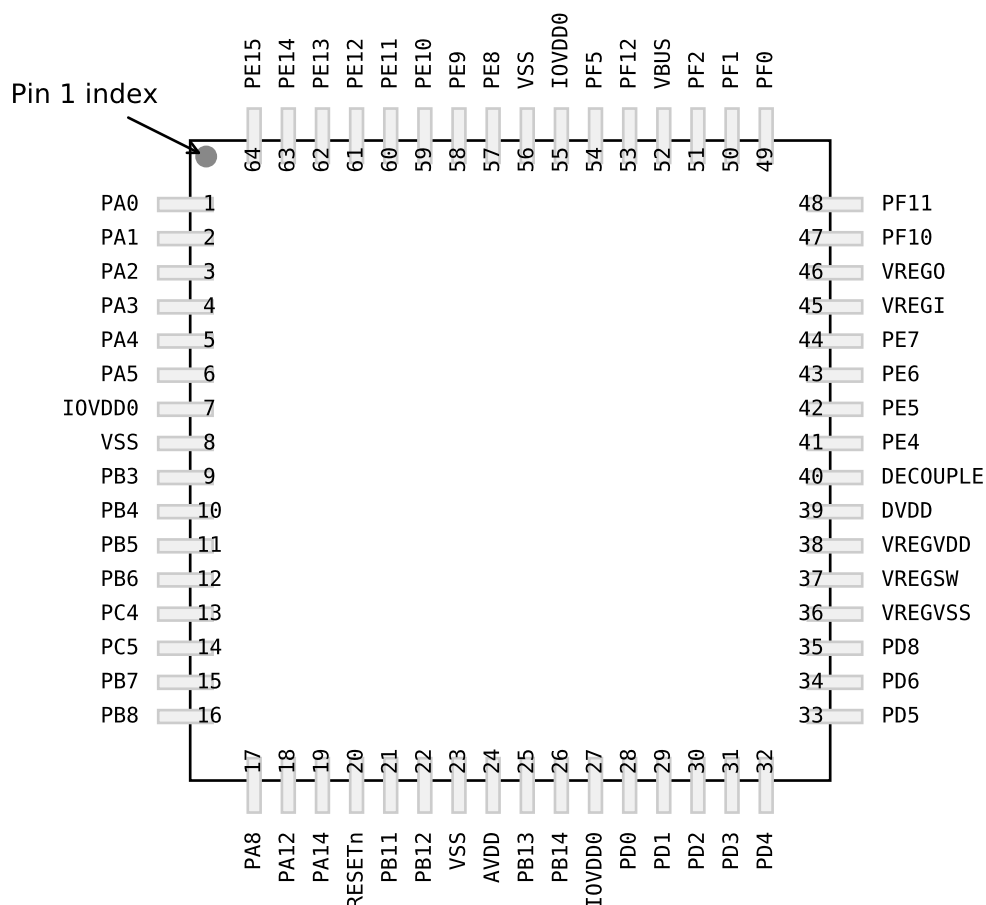


Figure 5.12. EFM32GG11B8xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.12. EFM32GG11B8xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD13		EBI_ARDY #1	TIM2_CDTI0 #1 TIM3_CC1 #6 WTIM0_CC1 #1	ETH_MDIO #1 US4_CTS #1 US5_CLK #1	ETM_TD1 #1
PI15				CAN1_TX #7 US3_CS #5	
PI14				CAN1_RX #7 US3_CLK #5	
PI13				CAN0_TX #7 US3_RX #5	
PI12				CAN0_RX #7 US3_TX #5	
PI10		EBI_A15 #2	TIM4_CC2 #3	US4_CTS #3	
PI7		EBI_A12 #2	TIM1_CC1 #7 TIM4_CC2 #2 WTIM3_CC1 #5	US4_RX #3	
PF15	BUSCY BUSDX		TIM1_CC2 #6 TIM4_CC2 #1 WTIM3_CC2 #7	US5_TX #2 I2C2_SDA #5	
PF12	BUSDY BUSCX	EBI_NANDREn #5	TIM4_CC2 #0 TIM1_CC3 #5 TIM5_CC0 #7 WTIM3_CC2 #6	US5_CS #2 I2C2_SCL #3 USB_ID	
PF4	BUSDY BUSCX LCD_SEG2	EBI_WEn #0 EBI_WEn #5	TIM4_CC1 #0 TIM0_CDTI1 #2 TIM1_CC2 #5 WTIM3_CC1 #6	US1_RTS #2 I2C2_SDA #3	PRS_CH1 #1
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BUSACMP1Y BU- SACMP1X	EBI_NANDREn #4	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LE- TIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 U1_RTS #0 LEU0_RX #5 I2C2_SCL #1	LES_CH15 PRS_CH1 #2 ACMP3_O #1 DBG_SWO #1
PC14	VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSACMP1Y BU- SACMP1X	EBI_NANDWEn #4	TIM0_CDTI1 #1 TIM1_CC1 #0 TIM1_CC3 #4 TIM5_CC0 #6 WTIM3_CC0 #3 LE- TIM0_OUT0 #5 PCNT0_S1IN #0	US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 U1_CTS #0 LEU0_TX #5 I2C2_SDA #1	LES_CH14 PRS_CH0 #2 ACMP3_O #2
PA2	BUSBY BUSAX LCD_SEG15	EBI_AD11 #0 EBI_DTEN #3	TIM0_CC2 #0 TIM3_CC2 #4	ETH_RMIIRXD0 #0 ETH_MIITXD2 #0 SDIO_DAT2 #1 US1_RX #6 US3_CLK #0 QSPIO_DQ0 #1	CMU_CLK0 #0 PRS_CH8 #1 ETM_TD0 #3
PG0	BUSACMP2Y BU- SACMP2X	EBI_AD00 #2	TIM6_CC0 #0 TIM2_CDTI0 #3 WTIM0_CDTI1 #1 LETIM1_OUT0 #6	ETH_MIITXCLK #1 US3_TX #4 QSPIO_SCLK #2	CMU_CLK2 #3

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PF6		LCD segment line 24.
LCD_SEG25	0: PF7		LCD segment line 25.
LCD_SEG26	0: PF8		LCD segment line 26.
LCD_SEG27	0: PF9		LCD segment line 27.
LCD_SEG28	0: PD9		LCD segment line 28.
LCD_SEG29	0: PD10		LCD segment line 29.
LCD_SEG30	0: PD11		LCD segment line 30.
LCD_SEG31	0: PD12		LCD segment line 31.
LCD_SEG32	0: PB0		LCD segment line 32.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.
OPA2_OUT	0: PD5		Operational Amplifier 2 output.
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.
OPA3_N	0: PC7		Operational Amplifier 3 external negative input.
OPA3_OUT	0: PD1		Operational Amplifier 3 output.
OPA3_P	0: PC6		Operational Amplifier 3 external positive input.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM0_CC2	0: PE6 1: PD14 2: PG4 3: PG10	4: PF1 5: PB2 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0	0: PE10 1: PD15 2: PA12 3: PG11	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1	0: PE11 1: PG0 2: PA13 3: PG12	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	0: PE12 1: PG1 2: PA14 3: PG13	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	4: PE3 5: PE7 6: PH8 7: PH12	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14 1: PD3 2: PD7 3: PE0	4: PE4 5: PI0 6: PH9 7: PH13	Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	0: PD0 1: PD4 2: PD8 3: PE1	4: PE5 5: PI1 6: PH10 7: PH14	Wide timer 1 Capture Compare input / output channel 2.
WTIM1_CC3	0: PD1 1: PD5 2: PC6 3: PE2	4: PE6 5: PI2 6: PH11 7: PH15	Wide timer 1 Capture Compare input / output channel 3.
WTIM2_CC0	0: PA9 1: PA12 2: PB9 3: PB12	4: PG14 5: PD3 6: PH4 7: PH7	Wide timer 2 Capture Compare input / output channel 0.
WTIM2_CC1	0: PA10 1: PA13 2: PB10 3: PG12	4: PG15 5: PD4 6: PH5 7: PH8	Wide timer 2 Capture Compare input / output channel 1.
WTIM2_CC2	0: PA11 1: PA14 2: PB11 3: PG13	4: PH0 5: PD5 6: PH6 7: PH9	Wide timer 2 Capture Compare input / output channel 2.
WTIM3_CC0	0: PD9 1: PC8 2: PC11 3: PC14	4: PI3 5: PI6 6: PB6 7: PF13	Wide timer 3 Capture Compare input / output channel 0.
WTIM3_CC1	0: PD10 1: PC9 2: PC12 3: PF10	4: PI4 5: PI7 6: PF4 7: PF14	Wide timer 3 Capture Compare input / output channel 1.

Table 5.26. ACMP3 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP3Y	BUSACMP3X	Bus
PF14	PF15	PF15	PF14	PB14	PB15	PB15	PB14			CH31
	PF13	PF13			PB13	PB13				CH30
PF12			PF12	PB12			PB12			CH29
	PF11	PF11			PB11	PB11				CH28
PF10			PF10	PB10			PB10			CH27
	PF9	PF9			PB9	PB9				CH26
PF8			PF8							CH25
	PF7	PF7								CH24
PF6			PF6	PB6			PB6			CH23
	PF5	PF5			PB5	PB5				CH22
PF4			PF4	PB4			PB4			CH21
	PF3	PF3			PB3	PB3				CH20
PF2			PF2	PB2			PB2			CH19
	PF1	PF1			PB1	PB1				CH18
PF0			PF0	PB0			PB0			CH17
	PE15	PE15			PA15	PA15				CH16
PE14			PE14	PA14			PA14			CH15
	PE13	PE13			PA13	PA13				CH14
PE12			PE12	PA12			PA12			CH13
	PE11	PE11			PA11	PA11				CH12
PE10			PE10	PA10			PA10			CH11
	PE9	PE9			PA9	PA9				CH10
PE8			PE8	PA8			PA8			CH9
	PE7	PE7			PA7	PA7				CH8
PE6			PE6	PA6			PA6	PH15	PH15	CH7
	PE5	PE5			PA5	PA5		PH14	PH14	CH6
PE4			PE4	PA4			PA4	PH13	PH13	CH5
					PA3	PA3		PH12	PH12	CH4
				PA2			PA2	PH11	PH11	CH3
	PE1	PE1			PA1	PA1		PH10	PH10	CH2
PE0			PE0	PA0			PA0	PH9	PH9	CH1
								PH8	PH8	CH0

7.3 BGA152 Package Marking



Figure 7.3. BGA152 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

11. TQFP64 Package Specifications

11.1 TQFP64 Package Dimensions

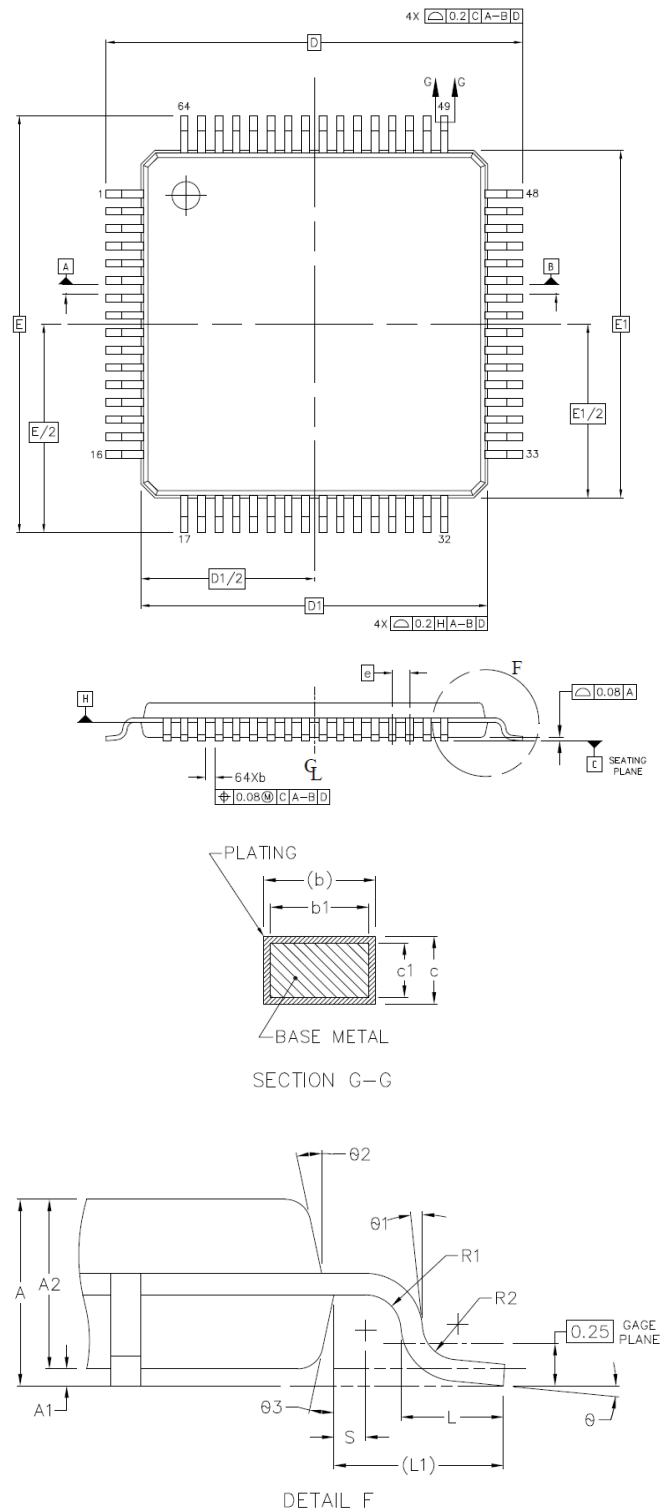


Figure 11.1. TQFP64 Package Drawing