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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	95
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b510f2048gl120-br

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.4.2 Internal and External Oscillators

The EFM32GG11 supports two crystal oscillators and fully integrates five RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 50 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (USHFRCO) is available for timing the USB, SDIO and QSPI peripherals. The USHFRCO can be syncronized to the host's USB clock to allow the USB to operate in device mode without the additional cost of an external crystal.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of wave-forms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.6.6 Quad-SPI Flash Controller (QSPI)

The QSPI provides access to to a wide range of flash devices with wide I/O busses. The I/O and clocking configuration is flexible and supports many types of devices. Up to 8-bit wide interfaces are supported. The QSPI handles opcodes, status flag polling, and timing configuration automatically.

The external flash memory is mapped directly to internal memory to allow random access to any word in the flash and direct code execution. An integrated instruction cache minimizes latency and allows efficient code execution. Execute in Place (XIP) is supported for devices with this feature.

Large data chunks can be transferred with DMA as efficiently as possible with high throughput and minimimal bus load, utilizing an integrated 1 kB SRAM FIFO.

3.6.7 SDIO Host Controller (SDIO)

The SDIO is an SD3.01 / SDIO3.0 / eMMC4.51-compliant Host Controller interface for transferring data to and from SD/MMC/SDIO devices. The module conforms to the SD Host Controller Standard Specification Version 3.00. The Host Controller handles SDIO/SD/MMC Protocol at the transmission level, packing data, adding cyclic redundancy check (CRC), Start/End bits, and checking for transaction format correctness.

3.6.8 Universal Serial Bus (USB)

The USB is a full-speed/low-speed USB 2.0 compliant host/device controller. The USB can be used in device and host-only configurations, while a clock recovery mechanism allows crystal-less operation in device mode. The USB block supports both full speed (12 MBit/s) and low speed (1.5 MBit/s) operation. When operating as a device, a special Low Energy Mode ensures the current consumption is optimized, enabling USB communications on a strict power budget. The USB device includes an internal dedicated Descriptor-Based Scatter/Gather DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes internal pull-up and pull-down resistors, as well as voltage comparators for monitoring the VBUS voltage and A/B device identification using the ID line.

3.6.9 Ethernet (ETH)

The Ethernet peripheral is compliant with IEEE 802.3-2002 for Ethernet MAC. It supports 802.1AS and IEEE 1588 precision clock synchronization protocol, as well as 802.3az Energy Efficient Ethernet. The ETH supports a wide variety of frame formats and standard operating modes such as MII/RMII. Direct Memory Access (DMA) support makes it possible to transmit and receive large frames at high data rates with minimal CPU overhead. The Ethernet peripheral supports 10 Mbps and 100 Mbps operation, and includes a total of 8 kB of dedicated dual-port RAM FIFO (4 kB for TX and 4 kB for RX).

3.6.10 Controller Area Network (CAN)

The CAN peripheral provides support for communication at up to 1 Mbps over CAN protocol version 2.0 part A and B. It includes 32 message objects with independent identifier masks and retains message RAM in EM2. Automatic retransmittion may be disabled in order to support Time Triggered CAN applications.

3.6.11 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.6.12 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSETM is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Output fall time, From 70%	t _{IOOF}	C _L = 50 pF,	_	1.8	_	ns
10 30% 01 V _{IO}		DRIVESTRENGTH ¹ = STRONG,				
		SLEWRATE ¹ = 0x6				
		C _L = 50 pF,	—	4.5	_	ns
		DRIVESTRENGTH ¹ = WEAK,				
		SLEWRATE ¹ = 0x6				
Output rise time, From 30%	tioor	C _L = 50 pF,	_	2.2		ns
to 70% of V _{IO}		DRIVESTRENGTH ¹ = STRONG,				
		SLEWRATE = 0x6 ¹				
		C _L = 50 pF,	_	7.4		ns
		DRIVESTRENGTH ¹ = WEAK,				
		SLEWRATE ¹ = 0x6				
Note:	1		1	1		
1. In GPIO_Pn_CTRL regis	ter.					

4.1.21 Pulse Counter (PCNT)

Table 4.29. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Input frequency	F _{IN}	Asynchronous Single and Quad- rature Modes	—	_	20	MHz
		Sampled Modes with Debounce filter set to 0.	_	_	8	kHz

4.1.22 Analog Port (APORT)

Table 4.30. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Supply current ^{2 1}	I _{APORT}	Operation in EM0/EM1	—	7	—	μA
		Operation in EM2/EM3		915		nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.

2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

EBI TFT Output Timing

All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.39. EBI TFT Output Timing

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Output hold time, EBI_DCLK to EBI_AD invalid	toh_dclk	IOVDD ≥ 1.62 V	-23 + (TFTHOLD ^{* t} нғсоя- есік)	_	_	ns
		IOVDD ≥ 3.0 V	-12 + (TFTHOLD ^{* t} нFCOR- ECLK)	_		ns
Output setup time, EBI_AD valid to EBI_DCLK	D t _{OSU_DCLK}	IOVDD ≥ 1.62 V	-11 + (TFTSET- UP * ^t HFCOR- ECLK)	—	_	ns
		IOVDD ≥ 3.0 V	-9 + (TFTSET- UP * t _{HFCOR-} ECLK)	_	_	ns



Figure 4.6. EBI TFT Output Timing

4.1.28.2 QSPI DDR Mode

QSPI DDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 35, RX DLL = 70, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.56. QSPI DDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Half SCLK period	T/2	HFXO	(1/F _{SCLK}) * 0.4 - 0.4	—	_	ns
		HFRCO, AUXHFRCO, USHFRCO	(1/F _{SCLK}) * 0.44	—	_	ns
Output valid	t _{OV}		—	_	T/2 - 5.0	ns
Output hold	t _{OH}		T/2 - 39.4	_	_	ns
Input setup	t _{SU}		33.1	_	_	ns
Input hold	t _H		-0.9			ns



Figure 4.28. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Supply

5. Pin Definitions

5.1 EFM32GG11B8xx in BGA192 Device Pinout

Pin A1 index	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	لا	<u>رمج</u>		(1) ³	ar th	(T)	(1)	F9	~F8	<u>(19</u>	510	(A)	(N)5	(T)	619	FO)
4	PAN	PEr C	PE	PEr	PEN	PEN	pt.	60.	60	62.	62	Pr.	100	Pr 2	Pr.	90 0
В	PAU	6017	6070	600	pry	64g	PEI	640	\$IT	628	662	PET3	643	PEL	6EJ	VREGO
С	49	6013	P014	6013	P113	PI14	PI13	PI13	P170	6IJ	pF13	PET3	PFA	673	PC14	VREGI
D	(TAG)	600	P015											PC13	C12	PC77
E	EA9	602	6CJ											¢C70	609	623
F	PAG	PGA	PG3			TONDOS	IOND)	55	MC.	TONDOG	TONDE)		619	p14	P13
G	PAS	609	PG5			TONDE	TONDI	(JS)	159.	TONDOG	TONDE)		623	617	610
н	049	608	PGT			159	159	(55)	(15 ⁵)	(15 ⁵)	(15 ⁵)			PES	PEG	PET
J	617	PG10	PG9			455	(15 ⁵)	(159)	(15 ⁵)	(15 ⁵)	159			PE3	PEA C	ECOUPLE
к	PG14	PG13	PG12			TONDE	TONDE	159	(5°).	TONDE	TONDE)		PEL	PE2	DADD
L	PG13	PB15	PB0			TONDE	TONDE	159	(5°).	TONDE	TONDE)		PEO	60)	REGUDD
М	PB ¹	682	PB3											60	REGVS	VREGSW
Ν	PBA	PB5	680											609	604	REGUSS
Ρ	609	PC3	602	849	PAI	PA13	PB9	PB12	PH2	PHS	PH8	eH1]	PH13	009	603	809
R	681	PC3	609	649	BODEN	RESET	B19	PH0	pH3	646	PH9	PHIZ	PH14	PH15	603	109
т	PB8	PCA	(TAG)	PA10	PAIZ	PALA	B 1	PHI	PHA	(PHT)	PH10	PB13	p814	AVOD	607	009

Figure 5.1. EFM32GG11B8xx in BGA192 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA15	A1	GPIO	PE15	A2	GPIO
PE14	A3	GPIO	PE13	A4	GPIO
PE12	A5	GPIO	PE11	A6	GPIO
PE10	A7	GPIO	PE9	A8	GPIO
PE8	A9	GPIO	PI9	A10	GPIO (5V)
PI6	A11	GPIO (5V)	PF14	A12	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD15	J2	GPIO (5V)	PC6	J12	GPIO
DECOUPLE	J13	Decouple output for on-chip voltage regulator. An external decoupling ca- pacitor is required at this pin.	PC0	K1	GPIO (5V)
PC1	K2	GPIO (5V)	PD8	K13	GPIO
PC2	L1	GPIO (5V)	PC3	L2	GPIO (5V)
PA7	L3	GPIO	PB9	L15	GPIO (5V)
PB10	L16	GPIO (5V)	PD0	L17	GPIO (5V)
PD1	L18	GPIO	PD4	L19	GPIO
PD7	L20	GPIO	PB7	M1	GPIO
PC4	M2	GPIO	PA8	M3	GPIO
PA10	M4	GPIO	PA13	M5	GPIO (5V)
PA14	M6	GPIO	RESETn	M7	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	M9 M10 N11	Analog power supply.	PD3	M12	GPIO
PD6	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	PB12	N7	GPIO
PB13	N9	GPIO	PB14	N10	GPIO
PD2	N12	GPIO (5V)	PD5	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF3	79	GPIO	PF4	80	GPIO
PF5	81	GPIO	PF6	84	GPIO
PF7	85	GPIO	PF8	86	GPIO
PF9	87	GPIO	PD9	88	GPIO
PD10	89	GPIO	PD11	90	GPIO
PD12	91	GPIO	PE8	92	GPIO
PE9	93	GPIO	PE10	94	GPIO
PE11	95	GPIO	PE12	96	GPIO
PE13	97	GPIO	PE14	98	GPIO
PE15	99	GPIO	PA15	100	GPIO
NUM					

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA12	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	PB12	22	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD8	35	GPIO	VREGVSS	36	Voltage regulator VSS
VREGSW	37	DCDC regulator switching node	VREGVDD	38	Voltage regulator VDD input
DVDD	39	Digital power supply.	DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	41	GPIO	PE5	42	GPIO
PE6	43	GPIO	PE7	44	GPIO
VREGI	45	Input to 5 V regulator.	VREGO	46	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs
PF10	47	GPIO (5V)	PF11	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.
PF12	53	GPIO	PF5	54	GPIO
PE8	57	GPIO	PE9	58	GPIO
PE10	59	GPIO	PE11	60	GPIO
PE12	61	GPIO	PE13	62	GPIO
PE14	63	GPIO	PE15	64	GPIO
Note:]	•		

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCA	TION									
Functionality	0 - 3	4 - 7	Description								
PRS_CH7	0: PB13 1: PA7 2: PE7		Peripheral Reflex System PRS, channel 7.								
PRS_CH8	0: PA8 1: PA2 2: PE9		Peripheral Reflex System PRS, channel 8.								
PRS_CH9	0: PA9 1: PA3 2: PB10		Peripheral Reflex System PRS, channel 9.								
PRS_CH10	0: PA10 1: PC2 2: PD4		Peripheral Reflex System PRS, channel 10.								
PRS_CH11	0: PA11 1: PC3 2: PD5		Peripheral Reflex System PRS, channel 11.								
0: PA12 1: PB6 2: PD8			Peripheral Reflex System PRS, channel 12.								
PRS_CH13	0: PA13 1: PB9 2: PE14		Peripheral Reflex System PRS, channel 13.								
PRS_CH14	0: PA14 1: PC6 2: PE15		Peripheral Reflex System PRS, channel 14.								
PRS_CH15	0: PA15 1: PC7 2: PF0		Peripheral Reflex System PRS, channel 15.								
PRS_CH16	0: PA4 1: PB12 2: PE4		Peripheral Reflex System PRS, channel 16.								
PRS_CH17	0: PA5 1: PB15 2: PE5		Peripheral Reflex System PRS, channel 17.								
PRS_CH18 0: PB2 1: PC10 2: PC4			Peripheral Reflex System PRS, channel 18.								
PRS_CH19	0: PB3 1: PC11 2: PC5		Peripheral Reflex System PRS, channel 19.								

Alternate	LOCA	TION								
Functionality	0 - 3	4 - 7	Description							
PRS_CH20	0: PB4 1: PC12 2: PE2		Peripheral Reflex System PRS, channel 20.							
PRS_CH21	0: PB5 1: PC13 2: PB11		Peripheral Reflex System PRS, channel 21.							
PRS_CH22	0: PB7 1: PE0 2: PF6		Peripheral Reflex System PRS, channel 22.							
PRS_CH23	0: PB8 1: PE1 2: PF7		Peripheral Reflex System PRS, channel 23.							
QSPI0_CS0	0: PF7 1: PA0 2: PG9		Quad SPI 0 Chip Select 0.							
QSPI0_CS1	0: PF8 1: PA1 2: PG10		Quad SPI 0 Chip Select 1.							
QSPI0_DQ0	0: PD9 1: PA2 2: PG1		Quad SPI 0 Data 0.							
QSPI0_DQ1	0: PD10 1: PA3 2: PG2		Quad SPI 0 Data 1.							
QSPI0_DQ2	0: PD11 1: PA4 2: PG3		Quad SPI 0 Data 2.							
QSPI0_DQ3	0: PD12 1: PA5 2: PG4		Quad SPI 0 Data 3.							
QSPI0_DQ4	0: PE8 1: PB3 2: PG5		Quad SPI 0 Data 4.							
QSPI0_DQ5	0: PE9 1: PB4 2: PG6		Quad SPI 0 Data 5.							
QSPI0_DQ6	0: PE10 1: PB5 2: PG7		Quad SPI 0 Data 6.							

Alternate	LOCA	ATION								
Functionality	0 - 3	4 - 7	Description							
WTIM0_CC2	0: PE6 1: PD14 2: PG4 3: PG10	4: PF1 5: PB2 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.							
WTIM0_CDTI0	0: PE10 1: PD15 2: PA12 3: PG11	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.							
WTIM0_CDTI1	0: PE11 1: PG0 2: PA13 3: PG12	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.							
WTIM0_CDTI2	0: PE12 1: PG1 2: PA14 3: PG13	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.							
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	4: PE3 5: PE7 6: PH8 7: PH12	Wide timer 1 Capture Compare input / output channel 0.							
WTIM1_CC1	0: PB14 1: PD3 2: PD7 3: PE0	4: PE4 5: PI0 6: PH9 7: PH13	Wide timer 1 Capture Compare input / output channel 1.							
WTIM1_CC2	0: PD0 1: PD4 2: PD8 3: PE1	4: PE5 5: PI1 6: PH10 7: PH14	Wide timer 1 Capture Compare input / output channel 2.							
WTIM1_CC3	0: PD1 1: PD5 2: PC6 3: PE2	4: PE6 5: PI2 6: PH11 7: PH15	Wide timer 1 Capture Compare input / output channel 3.							
WTIM2_CC0	0: PA9 1: PA12 2: PB9 3: PB12	4: PG14 5: PD3 6: PH4 7: PH7	Wide timer 2 Capture Compare input / output channel 0.							
WTIM2_CC1	0: PA10 1: PA13 2: PB10 3: PG12	4: PG15 5: PD4 6: PH5 7: PH8	Wide timer 2 Capture Compare input / output channel 1.							
WTIM2_CC2	0: PA11 1: PA14 2: PB11 3: PG13	4: PH0 5: PD5 6: PH6 7: PH9	Wide timer 2 Capture Compare input / output channel 2.							
WTIM3_CC0	0: PD9 1: PC8 2: PC11 3: PC14	4: PI3 5: PI6 6: PB6 7: PF13	Wide timer 3 Capture Compare input / output channel 0.							
WTIM3_CC1	0: PD10 1: PC9 2: PC12 3: PF10	4: Pl4 5: Pl7 6: PF4 7: PF14	Wide timer 3 Capture Compare input / output channel 1.							

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	СНЗ	CH2	CH1	CH0
APORT0X	BUSADC1X																									2Hd	9Hd	PH5	PH4	EH4	PH2	PH1	ЬНО
APORT0Y	BUSADC1Y																									2Hd	9Hd	PH5	PH4	EH4	PH2	PH1	ЬНО
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		6A9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		6Yd		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		63d		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PFO		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.28. ADC1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	СНО
ОР	OPA0_N																																
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
ОР	A0_	P																															
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PEO
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	

Table 5.31. VDAC0 / OPA Bus and Pin Mapping

Dimension	Min	Тур	Мах							
A	0.77	0.83	0.89							
A1	0.13	0.18	0.23							
A3	0.16 0.20 0.24									
A2		0.45 REF								
D		7.00 BSC								
е	0.40 BSC									
E	7.00 BSC									
D1		6.00 BSC								
E1		6.00 BSC								
b	0.20	0.25	0.30							
ааа		0.10								
bbb		0.10								
ddd		0.08								
eee		0.15								
fff	0.05									

Table 6.1. BGA192 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. BGA152 Package Specifications

7.1 BGA152 Package Dimensions



Figure 7.1. BGA152 Package Drawing

8. BGA120 Package Specifications

8.1 BGA120 Package Dimensions



Figure 8.1. BGA120 Package Drawing