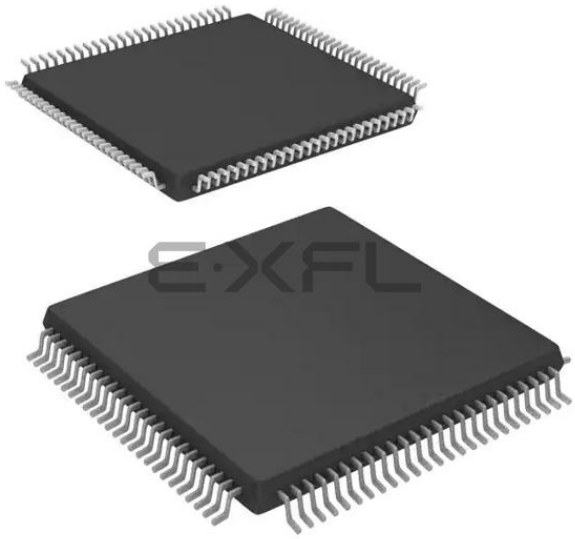
Silicon Labs - EFM32GG11B510F2048GQ100-BR Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b510f2048gq100-br

3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.
6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and $THETA_{JA}$.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN64 Package	$THETA_{JA\_QFN64}$	4-Layer PCB, Air velocity = 0 m/s	—	17.8	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	15.4	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	13.8	—	°C/W
Thermal resistance, TQFP64 Package	$THETA_{JA\_TQFP64}$	4-Layer PCB, Air velocity = 0 m/s	—	33.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	32.1	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	30.1	—	°C/W
Thermal resistance, TQFP100 Package	$THETA_{JA\_TQFP100}$	4-Layer PCB, Air velocity = 0 m/s	—	44.1	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	37.7	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	35.5	—	°C/W
Thermal resistance, BGA112 Package	$THETA_{JA\_BGA112}$	4-Layer PCB, Air velocity = 0 m/s	—	42.0	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	37.0	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	35.3	—	°C/W
Thermal resistance, BGA120 Package	$THETA_{JA\_BGA120}$	4-Layer PCB, Air velocity = 0 m/s	—	47.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	41.8	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	39.6	—	°C/W
Thermal resistance, BGA152 Package	$THETA_{JA\_BGA152}$	4-Layer PCB, Air velocity = 0 m/s	—	35.7	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	31.0	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	29.5	—	°C/W
Thermal resistance, BGA192 Package	$THETA_{JA\_BGA192}$	4-Layer PCB, Air velocity = 0 m/s	—	47.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	41.8	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	39.6	—	°C/W

4.1.5 5V Regulator

V_{VREGI} = 5 V, V_{VREGO} = 3.3 V, C_{VREGI} = 10 µF, C_{VREGO} = 4.7 µF, unless otherwise specified.

Table 4.5. 5V Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VREGI or VBUS input voltage range	V_{VREGI}	Regulating output	2.7	—	5.5	V
		Bypass mode enabled	2.7	—	3.8	V
VREGO output voltage	V_{VREGO}	Regulating output, 3.3 V setting	3.1	3.3	3.5	V
		EM4S open-loop output, I_{OUT} < 100 µA	1.8	—	3.8	V
Voltage output step size	V_{VREGO_SS}		—	0.1	—	V
Resistance in Bypass Mode	R_{BYP}	Bypass mode enabled	—	1.2	TBD	Ω
Output current	I_{OUT}	EM0 or EM1, V_{VREGI} > V_{VREGO} + 0.6 V	—	—	200	mA
		EM0 or EM1, V_{VREGI} > V_{VREGO} + 0.3 V	—	—	100	mA
		EM2, EM3, or EM4H, V_{VREGI} > V_{VREGO} + 0.6 V	—	—	2	mA
		EM2, EM3, or EM4H, V_{VREGI} > V_{VREGO} + 0.3 V	—	—	0.5	mA
		EM4S	—	—	20	µA
Load regulation	LR_{VREGO}	EM0 or EM1	—	0.10	—	mV/mA
		EM2, EM3, or EM4H	—	2.5	—	mV/mA
DC power supply rejection	PSR_{DC}		—	40	—	dB
VREGI or VBUS bypass capacitance	C_{VREGI}		—	10	—	µF
VREGO bypass capacitance	C_{VREGO}		1	4.7	10	µF
Supply current consumption	I_{VREGI}	EM0 or EM1, No load	—	29	—	µA
		EM2, EM3, or EM4H, No load	—	270	—	nA
		EM4S, No load	—	70	—	nA
VREGI and VBUS detection high threshold	V_{DET_H}		TBD	1.18	—	V
VREGI and VBUS detection low threshold	V_{DET_L}		—	1.12	TBD	V
Current monitor transfer ratio	$IMON_{XF}$	Translation of current through VREGO path to voltage at ADC input	—	0.35	—	mA/mV

4.1.10.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Table 4.16. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{AUXHFRCO\_ACC}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	$t_{AUXHFRCO}$	$f_{AUXHFRCO} \geq 19$ MHz	—	400	—	ns
		$4 < f_{AUXHFRCO} < 19$ MHz	—	1.4	—	µs
		$f_{AUXHFRCO} \leq 4$ MHz	—	2.5	—	µs
Current consumption on all supplies	$I_{AUXHFRCO}$	$f_{AUXHFRCO} = 50$ MHz	—	289	TBD	µA
		$f_{AUXHFRCO} = 48$ MHz	—	276	TBD	µA
		$f_{AUXHFRCO} = 38$ MHz	—	227	TBD	µA
		$f_{AUXHFRCO} = 32$ MHz	—	186	TBD	µA
		$f_{AUXHFRCO} = 26$ MHz	—	158	TBD	µA
		$f_{AUXHFRCO} = 19$ MHz	—	126	TBD	µA
		$f_{AUXHFRCO} = 16$ MHz	—	114	TBD	µA
		$f_{AUXHFRCO} = 13$ MHz	—	88	TBD	µA
		$f_{AUXHFRCO} = 7$ MHz	—	59	TBD	µA
		$f_{AUXHFRCO} = 4$ MHz	—	33	TBD	µA
		$f_{AUXHFRCO} = 2$ MHz	—	28	TBD	µA
		$f_{AUXHFRCO} = 1$ MHz	—	26	TBD	µA
Coarse trim step size (% of period)	$SS_{AUXHFRCO\_COARSE}$		—	0.8	—	%
Fine trim step size (% of period)	$SS_{AUXHFRCO\_FINE}$		—	0.1	—	%
Period jitter	$PJ_{AUXHFRCO}$		—	0.2	—	% RMS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	—	1.8	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	4.5	—	ns
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1]	—	2.2	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	7.4	—	ns

Note:
1. In GPIO_Pn_CTRL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	$SNDR_{DAC}$	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz	$SNDR_{DAC\_BAND}$	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity[3]	DNL_{DAC}		TBD	—	TBD	LSB
Intergral non-linearity	INL_{DAC}		TBD	—	TBD	LSB
Offset error[5]	V_{OFFSET}	T = 25 °C	TBD	—	TBD	mV
		Across operating temperature range	TBD	—	TBD	mV
Gain error[5]	V_{GAIN}	T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	TBD	—	TBD	%
		Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	TBD	—	TBD	%
External load capactiance, OUTSCALE=0	C_{LOAD}		—	—	75	pF

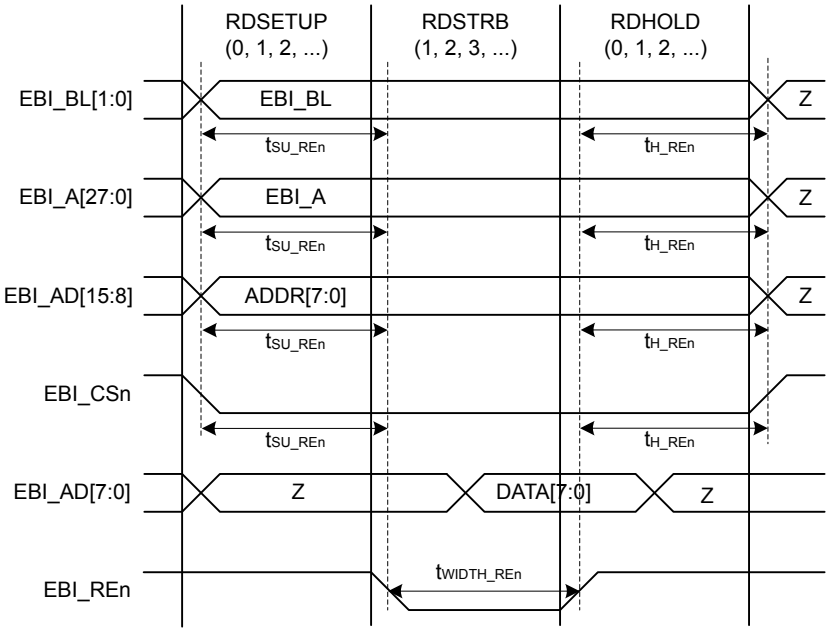

Figure 4.5. EBI Read Enable Output Timing Diagram

QSPI SDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 34, RX DLL = 59, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.55. QSPI SDR Mode Timing (Locations 1, 2)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full SCLK period	T		$(1/F_{SCLK})$ * 0.95	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 2.1	ns
Output hold	t_{OH}		T/2 - 42.3	—	—	ns
Input setup	t_{SU}		48.2 - T/2	—	—	ns
Input hold	t_H		T/2 - 5.1	—	—	ns

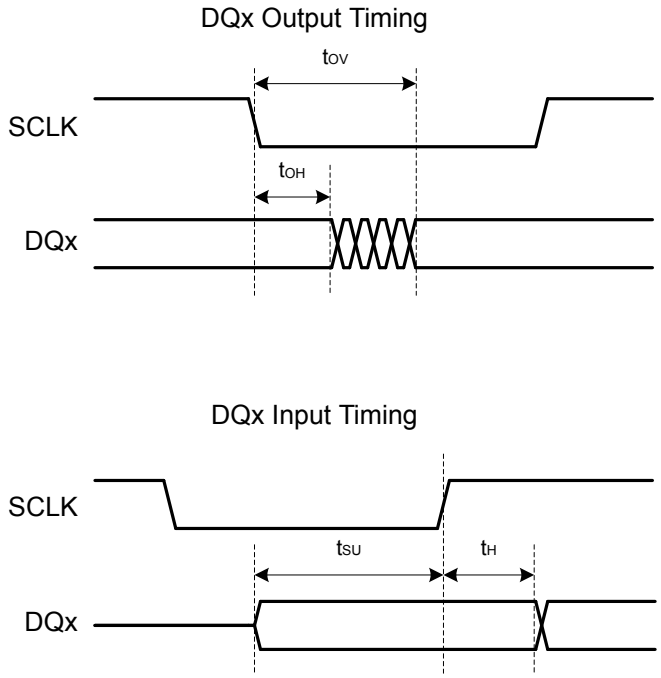

Figure 4.21. QSPI SDR Timing Diagrams

QSPI SDR Flash Timing Example

This example uses timing values for location 0 (SDR mode) to demonstrate the calculation of allowable flash timing using the QSPI in SDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 19 MHz:
- The resulting minimum period, T(min) = $(1/F_{SCLK})$ * 0.95 = 50.0 ns.
- Flash will see a minimum setup time of T/2 – t_{OV} = T/2 – (T/2 – 2.4) = 2.4 ns.
- Flash will see a minimum hold time of T/2 + t_{OH} = T/2 + (T/2 – 32.9) = T – 32.9 = 50.0 – 32.9 = 17.1 ns.
- Flash can have a maximum output valid time of T/2 – t_{SU} = T/2 – (36.2 – T/2) = T – 36.2 = 50.0 – 36.2 = 13.8 ns.
- Flash can have a minimum output hold time of t_H – T/2 = (T/2 – 3.3) – T/2 = - 3.3 ns.

QSPI DDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 53, RX DLL = 88, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.57. QSPI DDR Mode Timing (Locations 1, 2)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Half SCLK period	T/2	HFXO	(1/F_{SCLK}) * 0.4 - 0.4	—	—	ns
		HFRCO, AUXHFRCO, USHFRCO	(1/F_{SCLK}) * 0.44	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 6.6	ns
Output hold	t_{OH}		T/2 - 52.2	—	—	ns
Input setup	t_{SU}		44.8	—	—	ns
Input hold	t_H		-2.4	—	—	ns

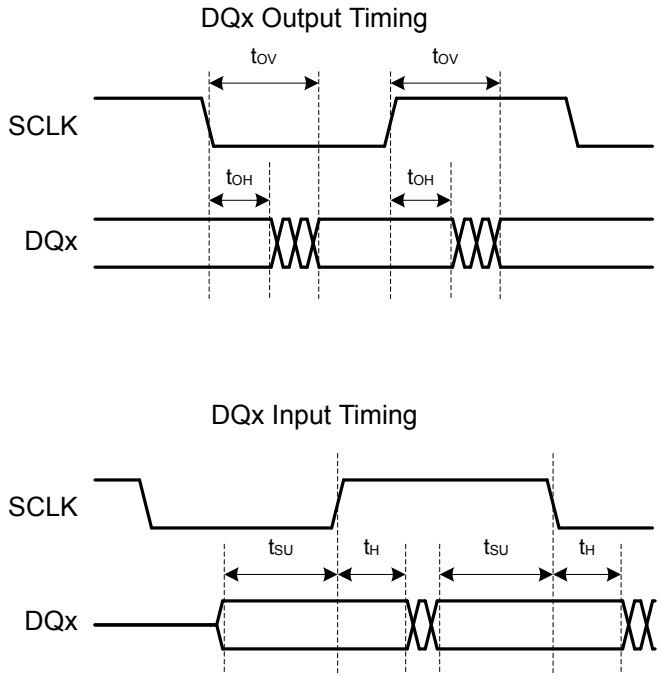

Figure 4.22. QSPI DDR Timing Diagrams

QSPI DDR Flash Timing Example

This example uses timing values for location 0 (DDR mode) to demonstrate the calculation of allowable flash timing using the QSPI in DDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 8 MHz from the HFXO clock source:
- The resulting minimum half-period, T/2(min) = (1/F_{SCLK}) * 0.4 - 0.4 = 49.6 ns.
- Flash will see a minimum setup time of T/2 – t_{OV} = T/2 – (T/2 – 5.0) = 5.0 ns.
- Flash will see a minimum hold time of t_{OH} = T/2 – 39.4 = 49.6 – 39.4 = 10.2 ns.
- Flash can have a maximum output valid time of T/2 – t_{SU} = T/2 – 33.1 = 49.6 – 33.1 = 16.5 ns.
- Flash can have a minimum output hold time of t_H = - 0.9 ns.

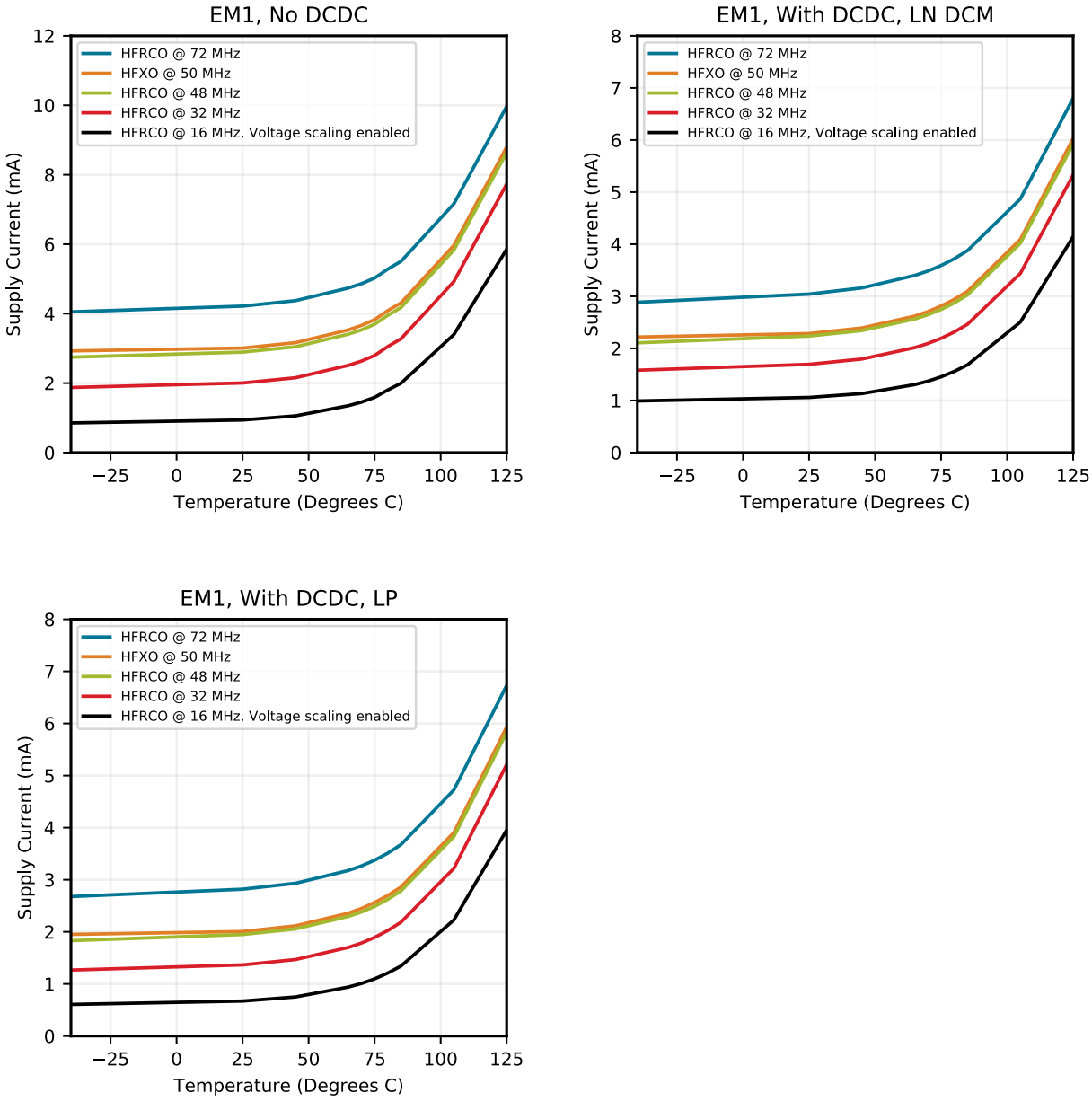

Figure 4.25. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 4.7 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

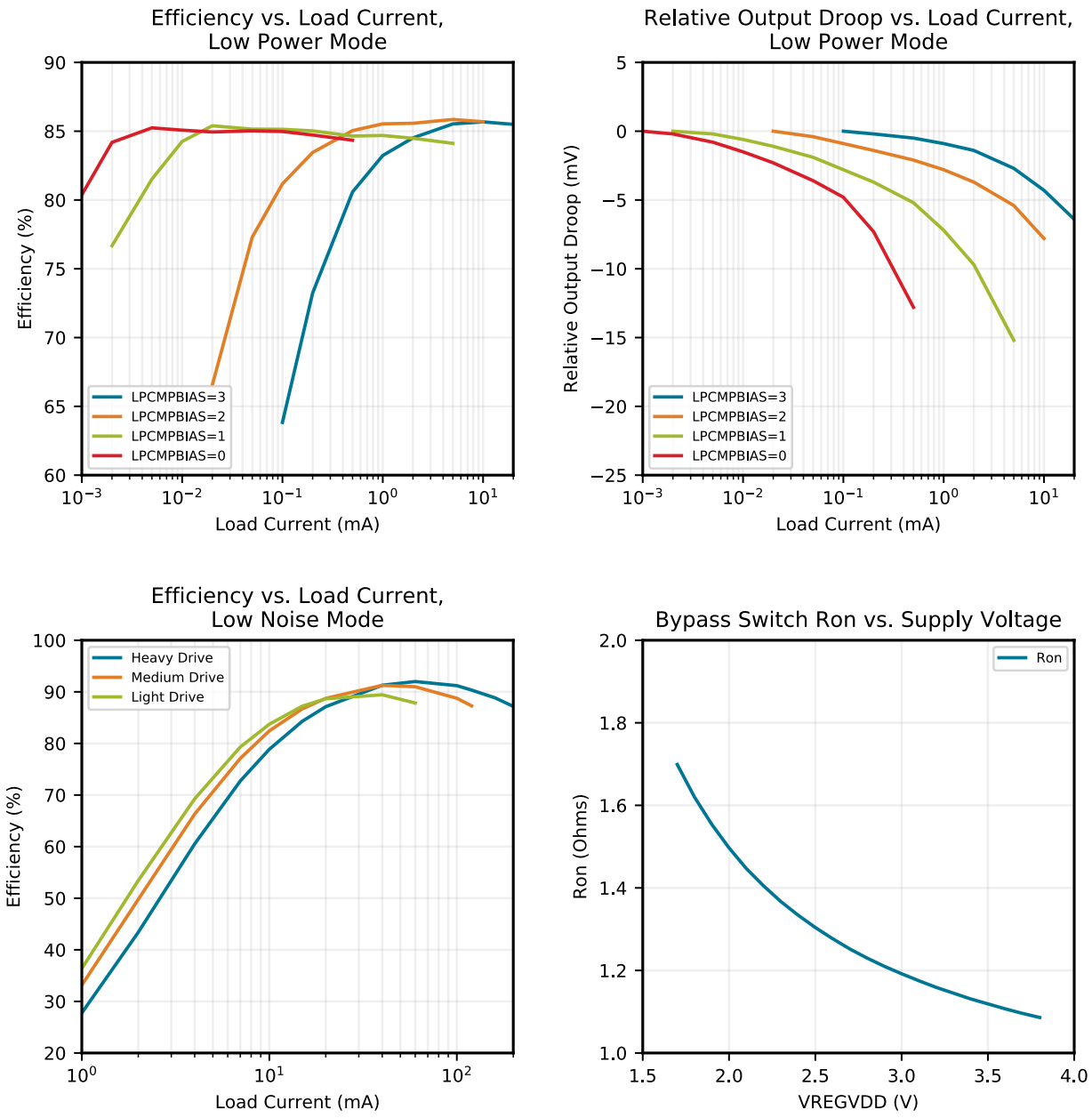

Figure 4.29. DC-DC Converter Typical Performance Characteristics

5.8 EFM32GG11B8xx in QFP100 Device Pinout

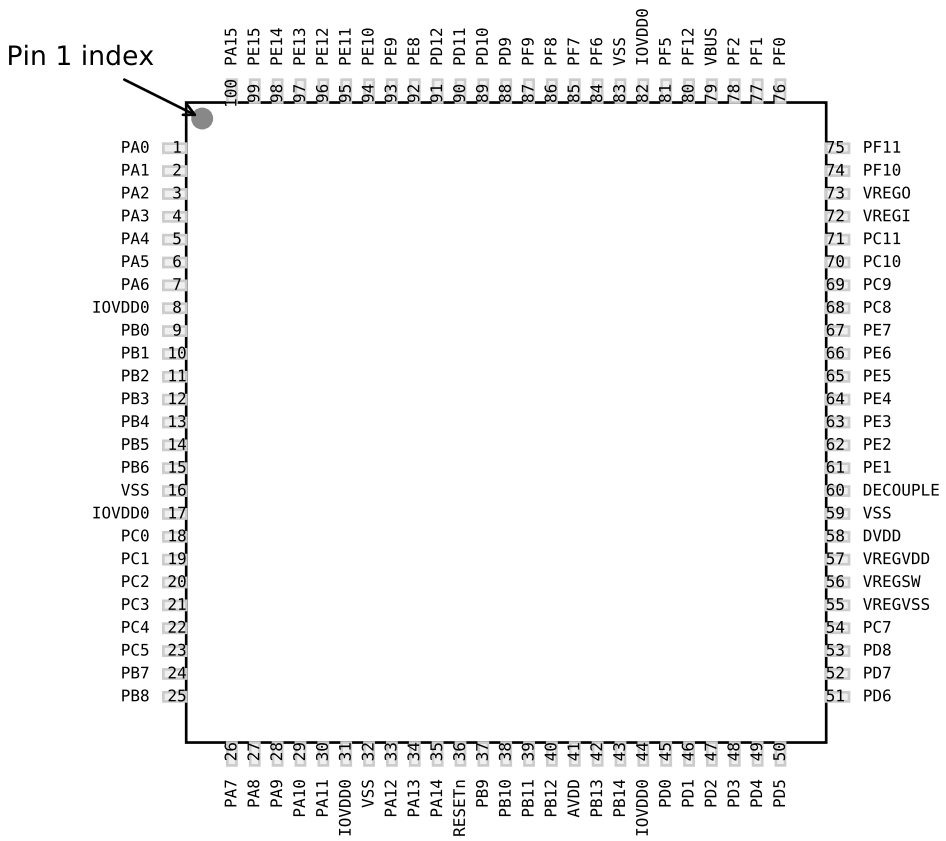

Figure 5.8. EFM32GG11B8xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.8. EFM32GG11B8xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF2	78	GPIO	NC	79	No Connect.
PF12	80	GPIO	PF5	81	GPIO
PF6	84	GPIO	PF7	85	GPIO
PF8	86	GPIO	PF9	87	GPIO
PD9	88	GPIO	PD10	89	GPIO
PD11	90	GPIO	PD12	91	GPIO
PE8	92	GPIO	PE9	93	GPIO
PE10	94	GPIO	PE11	95	GPIO
PE12	96	GPIO	PE13	97	GPIO
PE14	98	GPIO	PE15	99	GPIO
PA15	100	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.12 EFM32GG11B8xx in QFP64 Device Pinout

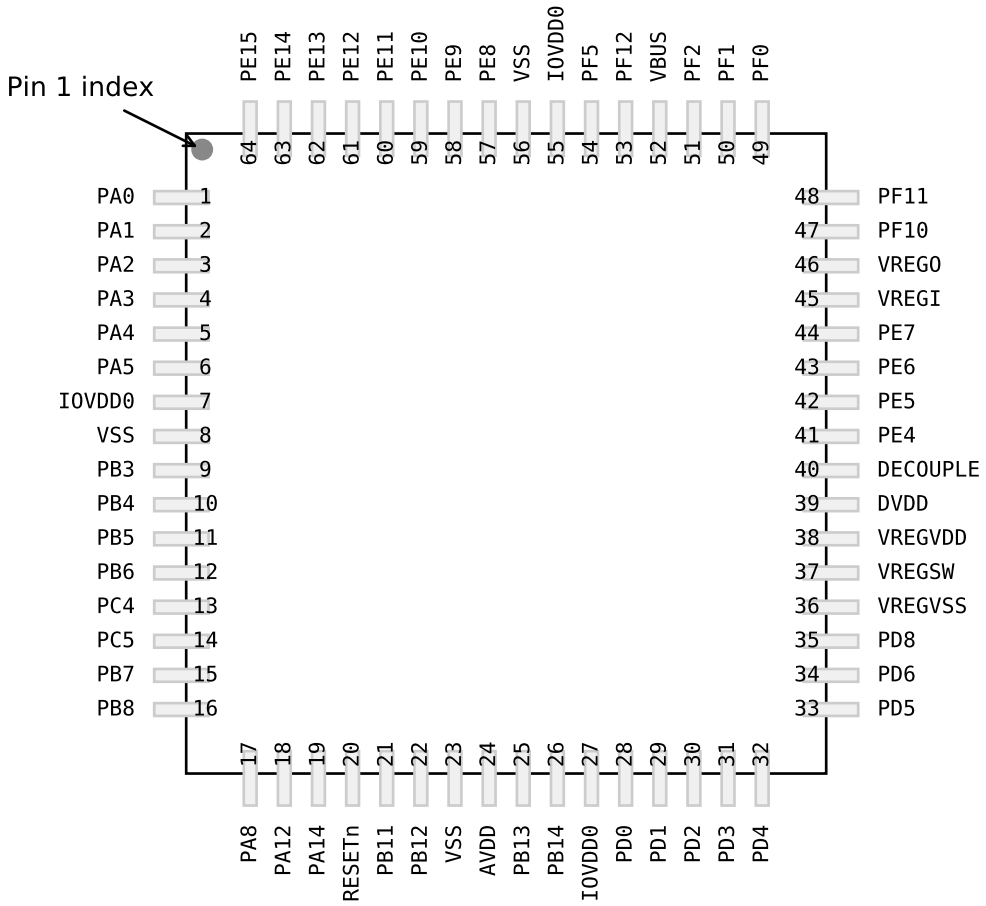

Figure 5.12. EFM32GG11B8xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.12. EFM32GG11B8xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

5.20 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 5.21 Alternate Functionality Overview for a list of GPIO locations available for each function.

Table 5.20. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PA15	BUSAY BUSBX LCD_SEG12	EBI_AD08 #0	TIM3_CC2 #0	ETH_MIIRXCLK #0 ETH_MDIO #3 US2_CLK #3	PRS_CH15 #0
PE15	BUSCY BUSDX LCD_SEG11	EBI_AD07 #0	TIM2_CDTI2 #2 TIM3_CC1 #0	ETH_RMIITXD0 #0 ETH_MIIRXD3 #0 SDIO_CMD #1 US0_RTS #0 QSPI0_DQS #1 LEU0_RX #2	PRS_CH14 #2 ETM_TD3 #4
PE14	BUSDY BUSCX LCD_SEG10	EBI_AD06 #0	TIM2_CDTI1 #2 TIM3_CC0 #0	ETH_RMIITXD1 #0 ETH_MIIRXD2 #0 SDIO_CLK #1 US0_CTS #0 QSPI0_SCLK #1 LEU0_TX #2	PRS_CH13 #2 ETM_TD2 #4
PE13	BUSCY BUSDX LCD_SEG9	EBI_AD05 #0	TIM1_CC3 #1 TIM2_CC2 #3 LE-TIM0_OUT1 #4	SDIO_CLK #0 ETH_MIIRXD1 #0 US0_TX #3 US0_CS #0 U1_RX #4 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 ETM_TD1 #4 GPIO_EM4WU5
PE12	BUSDY BUSCX LCD_SEG8	EBI_AD04 #0	TIM1_CC2 #1 TIM2_CC1 #3 WTIM0_CDTI2 #0 LETIM0_OUT0 #4	SDIO_CMD #0 ETH_MIIRXD0 #0 US0_RX #3 US0_CLK #0 U1_TX #4 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_ALTEX6 PRS_CH1 #3 ETM_TD0 #4
PE11	BUSCY BUSDX LCD_SEG7	EBI_AD03 #0 EBI_CS3 #4	TIM1_CC1 #1 TIM4_CC2 #7 WTIM0_CDTI1 #0	SDIO_DAT0 #0 QSPI0_DQ7 #0 ETH_MIIRXDV #0 US0_RX #0	LES_ALTEX5 PRS_CH3 #2 ETM_TCLK #4
PE10	BUSDY BUSCX LCD_SEG6	EBI_AD02 #0 EBI_CS2 #4	TIM1_CC0 #1 TIM4_CC1 #7 WTIM0_CDTI0 #0	SDIO_DAT1 #0 QSPI0_DQ6 #0 ETH_MIIRXER #0 US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE9	BUSCY BUSDX LCD_SEG5	EBI_AD01 #0 EBI_CS1 #4	TIM4_CC0 #7 PCNT2_S1IN #1	SDIO_DAT2 #0 QSPI0_DQ5 #0 US5_RX #0	PRS_CH8 #2
PE8	BUSDY BUSCX LCD_SEG4	EBI_AD00 #0 EBI_CS0 #4	TIM2_CDTI0 #2 TIM4_CC2 #6 PCNT2_S0IN #1	SDIO_DAT3 #0 QSPI0_DQ4 #0 US5_TX #0 I2C2_SDA #0	PRS_CH3 #1
PI9		EBI_A14 #2	TIM1_CC3 #7 TIM4_CC1 #3	US4_CS #3	
PI6		EBI_A11 #2	TIM1_CC0 #7 TIM4_CC1 #2 WTIM3_CC0 #5	US4_TX #3	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD4	BUSADC0Y BUSADC0X OPA2_P	EBI_A08 #1 EBI_A17 #3	TIM6_CC0 #7 WTIM0_CDTI0 #4 WTIM1_CC2 #1 WTIM2_CC1 #5	CAN1_TX #2 US1_CTS #1 US3_CLK #2 LEU0_TX #0 I2C1_SDA #3	CMU_CLKI0 #0 PRS_CH10 #2 ETM_TD2 #0 ETM_TD2 #2
PC0	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSACMP0Y BUSACMP0X	EBI_AD07 #1 EBI_CS0 #2 EBI_REn #3 EBI_A23 #0	TIM0_CC1 #3 TIM2_CC1 #4 PCNT0_S0IN #2	ETH_MDIO #2 CAN0_RX #0 US0_TX #5 US1_TX #0 US1_CS #4 US2_RTS #0 US3_CS #3 I2C0_SDA #4	LES_CH0 PRS_CH2 #0
PC1	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSACMP0Y BUSACMP0X	EBI_AD08 #1 EBI_CS1 #2 EBI_BL0 #3 EBI_A24 #0	TIM0_CC2 #3 TIM2_CC2 #4 WTIM0_CC0 #7 PCNT0_S1IN #2	ETH_MDC #2 CAN0_TX #0 US0_RX #5 US1_TX #4 US1_RX #0 US2_CTS #0 US3_RTS #1 I2C0_SCL #4	LES_CH1 PRS_CH3 #0
PC2	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSACMP0Y BUSACMP0X	EBI_AD09 #1 EBI_CS2 #2 EBI_NANDWEn #3 EBI_A25 #0	TIM0_CDTI0 #3 TIM2_CC0 #5 WTIM0_CC1 #7 LETIM1_OUT0 #3	ETH_TSUEXTCLK #2 CAN1_RX #0 US1_RX #4 US2_TX #0	LES_CH2 PRS_CH10 #1
PA8	BUSBY BUSAX LCD_SEG36	EBI_AD14 #1 EBI_A02 #3 EBI_DCLK #0	TIM2_CC0 #0 TIM0_CC0 #6 LETIM0_OUT0 #6 PCNT1_S1IN #4	US2_RX #2 US4_RTS #0	PRS_CH8 #0
PA11	BUSAY BUSBX LCD_SEG39	EBI_CS1 #1 EBI_A05 #3 EBI_HSNC #0	WTIM2_CC2 #0 LETIM1_OUT0 #1	US2_CTS #2	PRS_CH11 #0
PA13	BUSAY BUSBX	EBI_WEn #1 EBI_NANDWEn #2 EBI_A01 #0 EBI_A07 #3	TIM0_CC2 #7 TIM2_CC1 #1 WTIM0_CDTI1 #2 WTIM2_CC1 #1 LETIM1_OUT1 #1 PCNT1_S1IN #5	CAN1_TX #5 US0_CS #5 US2_TX #3	PRS_CH13 #0
PB9	BUSAY BUSBX	EBI_ALE #1 EBI_NANDREn #2 EBI_A00 #1 EBI_A03 #0 EBI_A09 #3	WTIM2_CC0 #2 LETIM0_OUT0 #7	SDIO_WP #3 CAN0_RX #3 US1_CTS #0 U1_TX #2	PRS_CH13 #1 ACMP1_O #5
PB12	BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT	EBI_A03 #1 EBI_A12 #3 EBI_CSTFT #2	TIM1_CC3 #3 WTIM2_CC0 #3 LETIM0_OUT1 #1 PCNT0_S0IN #7 PCNT1_S1IN #6	US2_CTS #1 US5_RTS #0 U1_RTS #2 I2C1_SCL #1	PRS_CH16 #1
PH2	BUSADC1Y BUSADC1X	EBI_VSNC #2	TIM6_CC0 #3	US1_CTS #6	
PH5	BUSADC1Y BUSADC1X	EBI_A17 #2	TIM6_CDTI0 #3 WTIM2_CC1 #6	US4_RX #4	
PH8	BUSACMP3Y BUSACMP3X	EBI_A20 #2	TIM6_CC0 #4 WTIM1_CC0 #6 WTIM2_CC1 #7	US4_CTS #4	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PF6		LCD segment line 24.
LCD_SEG25	0: PF7		LCD segment line 25.
LCD_SEG26	0: PF8		LCD segment line 26.
LCD_SEG27	0: PF9		LCD segment line 27.
LCD_SEG28	0: PD9		LCD segment line 28.
LCD_SEG29	0: PD10		LCD segment line 29.
LCD_SEG30	0: PD11		LCD segment line 30.
LCD_SEG31	0: PD12		LCD segment line 31.
LCD_SEG32	0: PB0		LCD segment line 32.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM4_CDTI2	0: PD3		Timer 4 Complimentary Dead Time Insertion channel 2.
TIM5_CC0	0: PE4 1: PE7 2: PH13 3: PI0	4: PC8 5: PC11 6: PC14 7: PF12	Timer 5 Capture Compare input / output channel 0.
TIM5_CC1	0: PE5 1: PH11 2: PH14 3: PI1	4: PC9 5: PC12 6: PF10 7: PF13	Timer 5 Capture Compare input / output channel 1.
TIM5_CC2	0: PE6 1: PH12 2: PH15 3: PI2	4: PC10 5: PC13 6: PF11 7: PF14	Timer 5 Capture Compare input / output channel 2.
TIM6_CC0	0: PG0 1: PG6 2: PG12 3: PH2	4: PH8 5: PB13 6: PD1 7: PD4	Timer 6 Capture Compare input / output channel 0.
TIM6_CC1	0: PG1 1: PG7 2: PG13 3: PH3	4: PH9 5: PB14 6: PD2 7: PD5	Timer 6 Capture Compare input / output channel 1.
TIM6_CC2	0: PG2 1: PG8 2: PG14 3: PH4	4: PH10 5: PD0 6: PD3 7: PD6	Timer 6 Capture Compare input / output channel 2.
TIM6_CDTI0	0: PG3 1: PG9 2: PE4 3: PH5		Timer 6 Complimentary Dead Time Insertion channel 0.
TIM6_CDTI1	0: PG4 1: PG10 2: PE5 3: PH6		Timer 6 Complimentary Dead Time Insertion channel 1.
TIM6_CDTI2	0: PG5 1: PG11 2: PE6 3: PH7		Timer 6 Complimentary Dead Time Insertion channel 2.
U0_CTS	0: PF8 1: PE2 2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.
U0_RTS	0: PF9 1: PE3 2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	0: PF7 1: PE1 2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.

8. BGA120 Package Specifications

8.1 BGA120 Package Dimensions

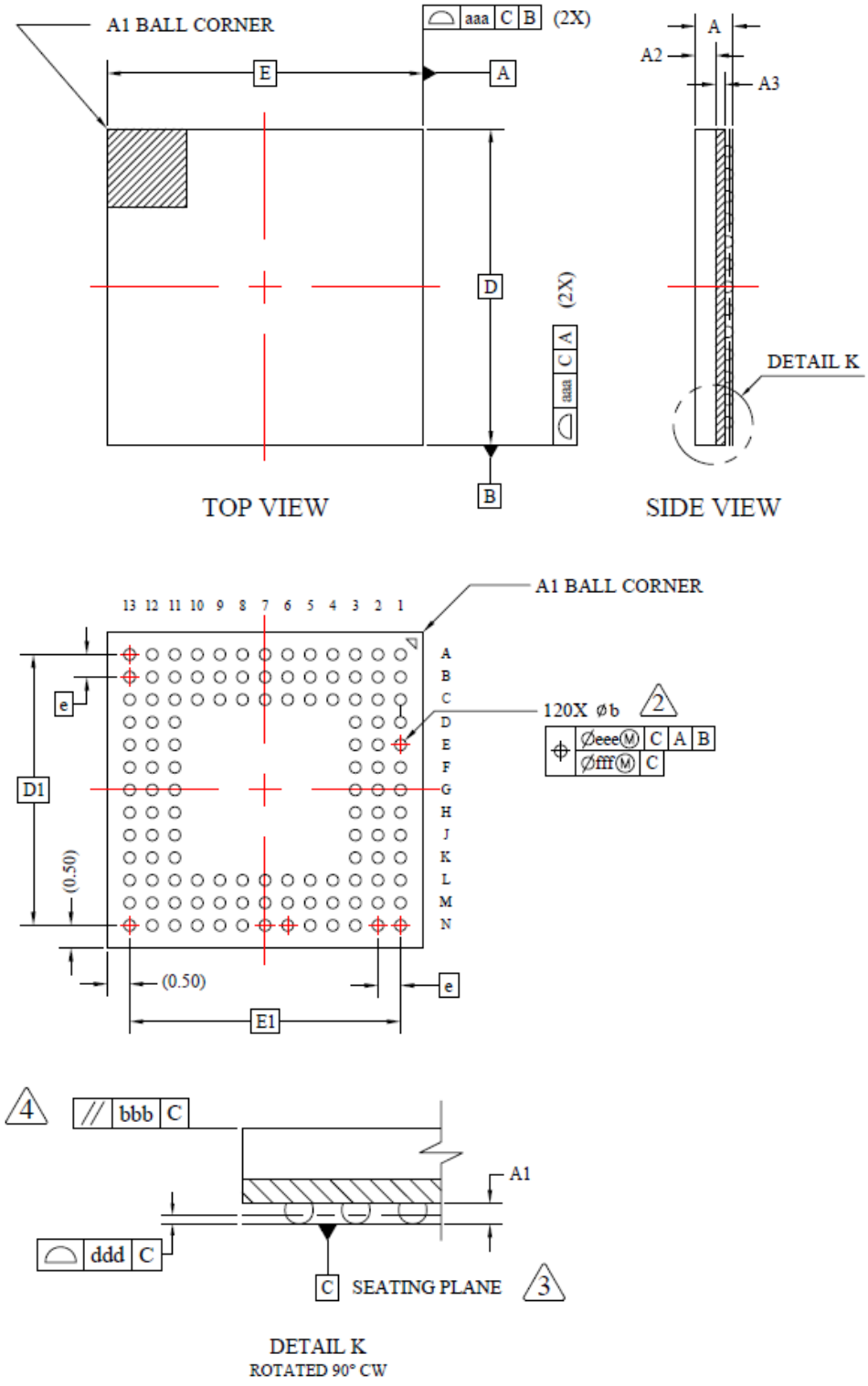

Figure 8.1. BGA120 Package Drawing

9.2 BGA112 PCB Land Pattern

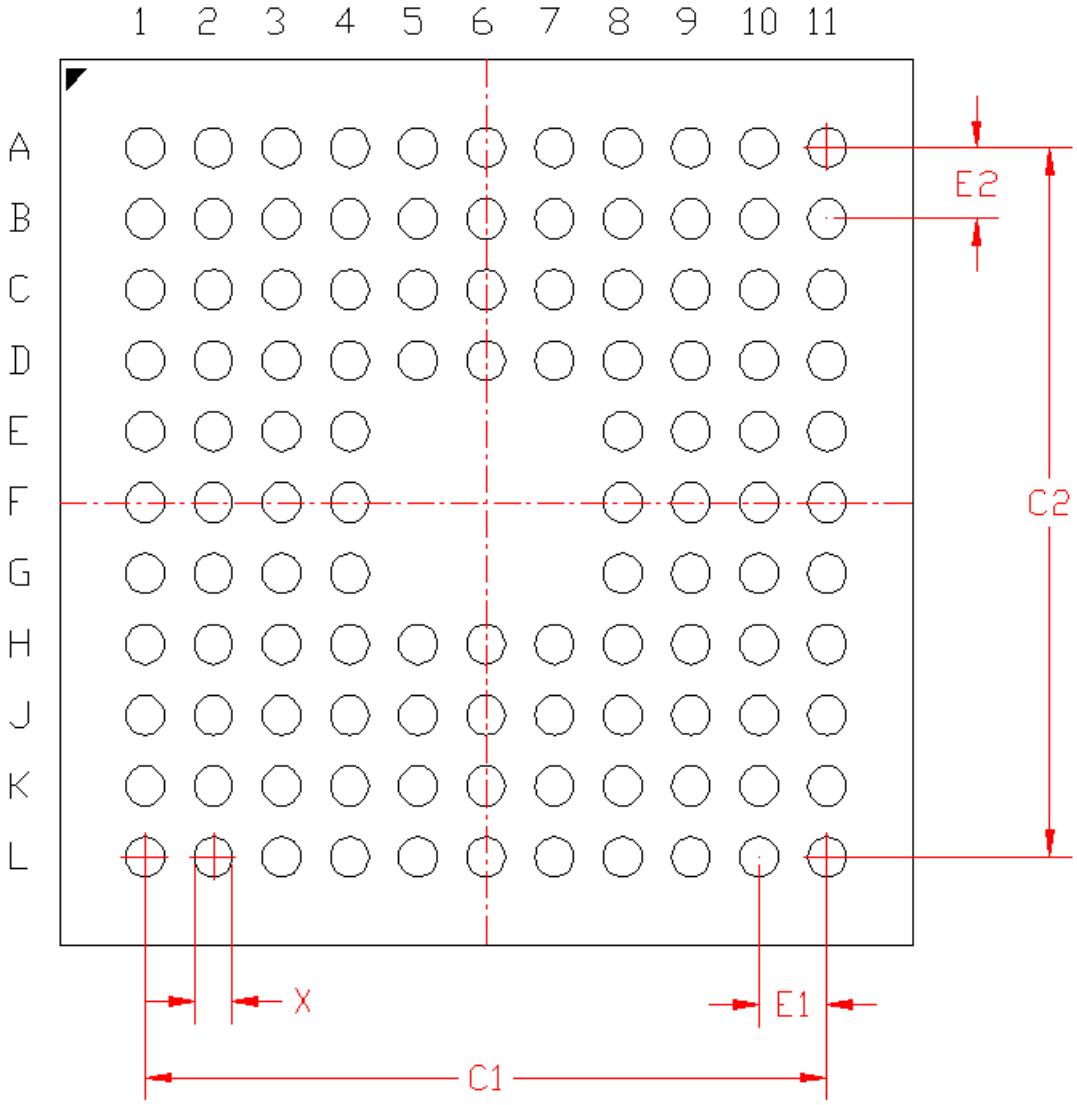

Figure 9.2. BGA112 PCB Land Pattern Drawing