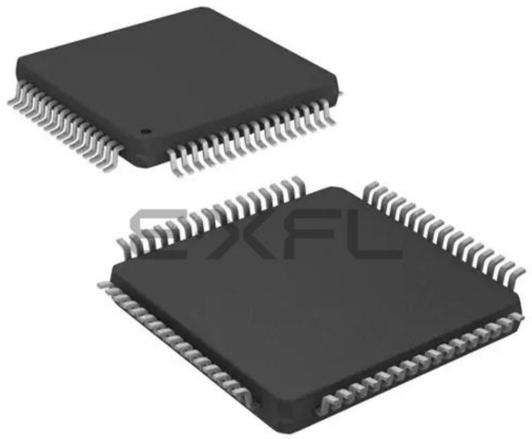

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b510f2048gq64-a

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3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

4.1.9 Brown Out Detector (BOD)

Table 4.11. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	1.62	V
		DVDD falling (EM0/EM1)	1.35	—	—	V
		DVDD falling (EM2/EM3)	TBD	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	18	—	mV
DVDD BOD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/μs rate	—	2.4	—	μs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.8	V
		AVDD falling (EM0/EM1)	1.62	—	—	V
		AVDD falling (EM2/EM3)	TBD	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	20	—	mV
AVDD BOD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/μs rate	—	2.4	—	μs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/μs rate	—	300	—	μs

4.1.10.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.14. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF[2] = 1	TBD	32.768	TBD	kHz
		ENVREF[2] = 1, T > 85 °C	TBD	32.768	TBD	kHz
		ENVREF[2] = 0	TBD	32.768	TBD	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	370	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	520	—	nA

Note:

1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. In CMU_LFRCOCTRL register.

4.1.10.6 USB High-Frequency RC Oscillator (USHFRCO)

Table 4.17. USB High-Frequency RC Oscillator (USHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{USHFRCO\_ACC}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
		USB clock recovery enabled, Active connection as device, FINETUNINGEN[1] = 1	-0.25	—	0.25	%
Start-up time	$t_{USHFRCO}$		—	300	—	ns
Current consumption on all supplies	$I_{USHFRCO}$	$f_{USHFRCO}$ = 48 MHz, FINETUNINGEN[1] = 1	—	340	TBD	µA
		$f_{USHFRCO}$ = 50 MHz, FINETUNINGEN[1] = 0	—	342	TBD	µA
		$f_{USHFRCO}$ = 48 MHz, FINETUNINGEN[1] = 0	—	292	TBD	µA
		$f_{USHFRCO}$ = 32 MHz, FINETUNINGEN[1] = 0	—	223	TBD	µA
		$f_{USHFRCO}$ = 16 MHz, FINETUNINGEN[1] = 0	—	132	TBD	µA
Period jitter	$PJ_{USHFRCO}$		—	0.2	—	% RMS

Note:
1. In the CMU_USHFRCOCTRL register.

4.1.10.7 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.18. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		TBD	1	TBD	kHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:
1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
3. ± 100 mV differential drive.
4. In ACMPn_CTRL register.
5. In ACMPn_HYSTERESIS registers.
6. In ACMPn_INPUTSEL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current, continuous conversions, WARMUP-MODE=KEEPCSENWARM	I_{CSEN_ACTIVE}	SAR or Delta Modulation conversions of 33 pF capacitor, CS0CG=0 (Gain = 10x), always on	—	90.5	—	μA
HFPERCLK supply current	$I_{CSEN\_HFPERCLK}$	Current contribution from HFPERCLK when clock to CSEN block is enabled.	—	2.25	—	μA/MHz

Note:

1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

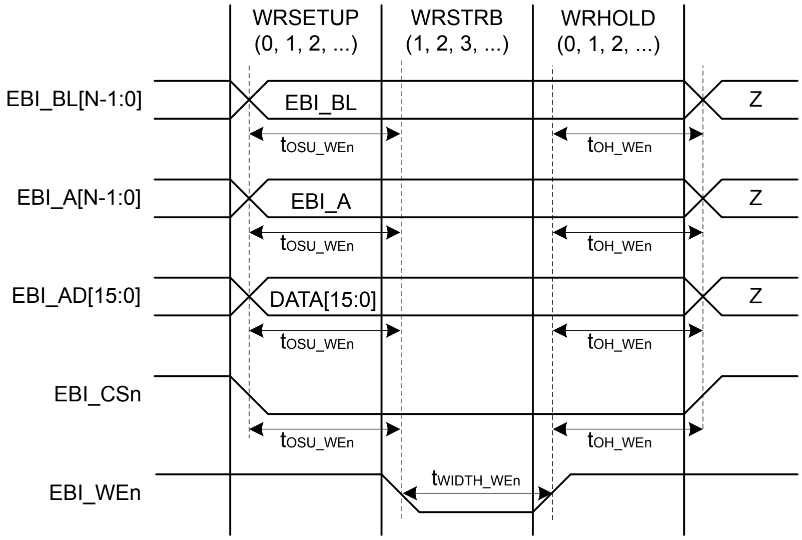

Figure 4.3. EBI Write Enable Output Timing Diagram

SDIO DDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 30 pF on all pins.

Table 4.49. SDIO DS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.69	6.52	—	ns
Clock fall time	t_F		1.42	4.96	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		1.8	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		0.8	—	—	ns
Input setup time, DAT[0:3] valid to SD_CLK	t_{ISU2X}		6	—	—	ns
Input hold time, SD_CLK to DAT[0:3] change	t_{IH2X}		1.5	—	—	ns
Output delay time, SD_CLK to DAT[0:3] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:3] change	t_{OH2X}		0.8	—	—	ns

SDIO MMC SDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.50. SDIO MMC SDR Mode Timing (Location 0, 1.8V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	25	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.96	8.27	—	ns
Clock fall time	t_F		1.67	6.90	—	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:7] change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	t_{OH}		3	—	—	ns

5.5 EFM32GG11B4xx in BGA120 Device Pinout

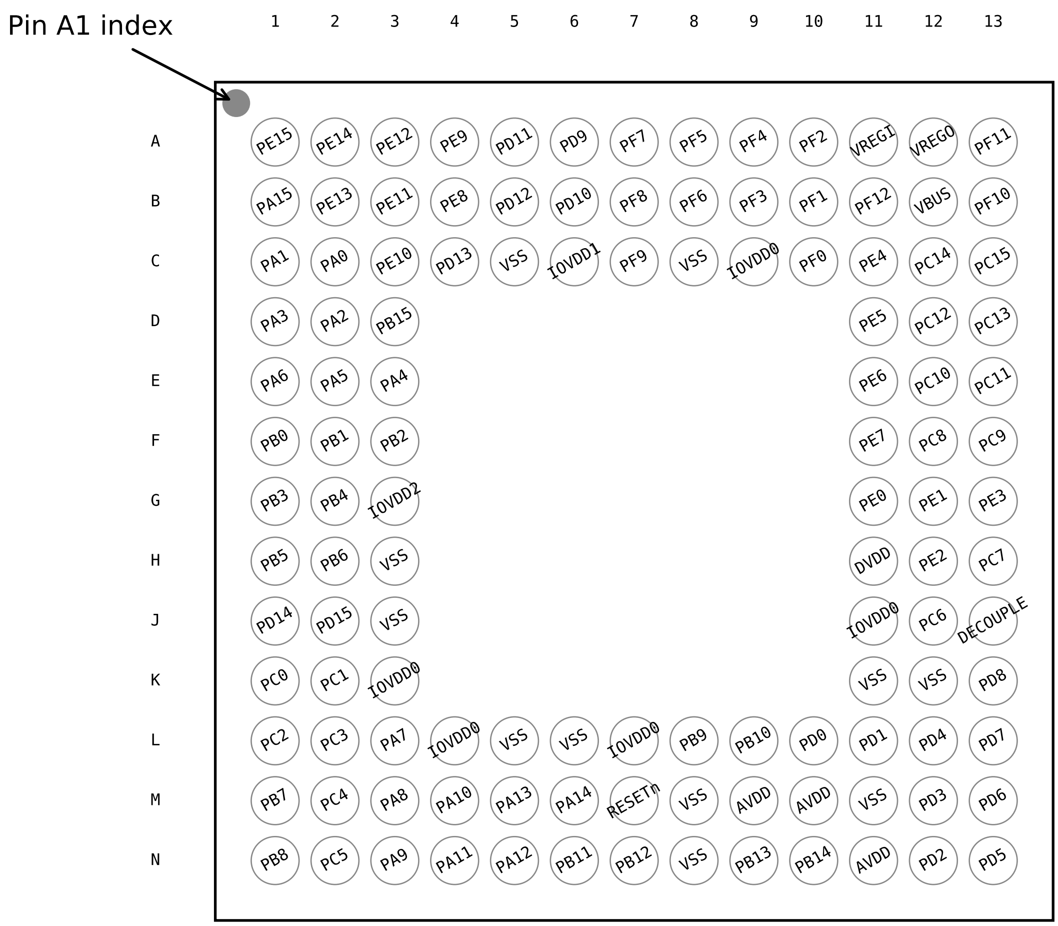

Figure 5.5. EFM32GG11B4xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.5. EFM32GG11B4xx in BGA120 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF4	A9	GPIO	PF2	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF2	78	GPIO	VBUS	79	USB VBUS signal and auxiliary input to 5 V regulator.
PF12	80	GPIO	PF5	81	GPIO
PF6	84	GPIO	PF7	85	GPIO
PF8	86	GPIO	PF9	87	GPIO
PD9	88	GPIO	PD10	89	GPIO
PD11	90	GPIO	PD12	91	GPIO
PE8	92	GPIO	PE9	93	GPIO
PE10	94	GPIO	PE11	95	GPIO
PE12	96	GPIO	PE13	97	GPIO
PE14	98	GPIO	PE15	99	GPIO
PA15	100	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA12	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	PB12	22	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD7	35	GPIO	PD8	36	GPIO
PC7	37	GPIO	VREGVSS	38	Voltage regulator VSS
VREGSW	39	DCDC regulator switching node	VREGVDD	40	Voltage regulator VDD input
DVDD	41	Digital power supply.	DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	43	GPIO	PE5	44	GPIO
PE6	45	GPIO	PE7	46	GPIO
PC12	47	GPIO (5V)	PC13	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	PF3	52	GPIO
PF4	53	GPIO	PF5	54	GPIO
PE8	57	GPIO	PE9	58	GPIO
PE10	59	GPIO	PE11	60	GPIO
PE12	61	GPIO	PE13	62	GPIO
PE14	63	GPIO	PE15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM2_CC1	0: PA9 1: PA13 2: PC9 3: PE12	4: PC0 5: PC3 6: PG9 7: PG6	Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	0: PA10 1: PA14 2: PC10 3: PE13	4: PC1 5: PC4 6: PG10 7: PG7	Timer 2 Capture Compare input / output channel 2.
TIM2_CDTI0	0: PB0 1: PD13 2: PE8 3: PG0		Timer 2 Complimentary Dead Time Insertion channel 0.
TIM2_CDTI1	0: PB1 1: PD14 2: PE14 3: PG1		Timer 2 Complimentary Dead Time Insertion channel 1.
TIM2_CDTI2	0: PB2 1: PD15 2: PE15 3: PG2		Timer 2 Complimentary Dead Time Insertion channel 2.
TIM3_CC0	0: PE14 1: PE0 2: PE3 3: PE5	4: PA0 5: PA3 6: PA6 7: PD15	Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	0: PE15 1: PE1 2: PE4 3: PE6	4: PA1 5: PA4 6: PD13 7: PB15	Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	0: PA15 1: PE2 2: PE5 3: PE7	4: PA2 5: PA5 6: PD14 7: PB0	Timer 3 Capture Compare input / output channel 2.
TIM4_CC0	0: PF3 1: PF13 2: PF5 3: PI8	4: PF6 5: PF9 6: PD11 7: PE9	Timer 4 Capture Compare input / output channel 0.
TIM4_CC1	0: PF4 1: PF14 2: PI6 3: PI9	4: PF7 5: PD9 6: PD12 7: PE10	Timer 4 Capture Compare input / output channel 1.
TIM4_CC2	0: PF12 1: PF15 2: PI7 3: PI10	4: PF8 5: PD10 6: PE8 7: PE11	Timer 4 Capture Compare input / output channel 2.
TIM4_CDTI0	0: PD0		Timer 4 Complimentary Dead Time Insertion channel 0.
TIM4_CDTI1	0: PD1		Timer 4 Complimentary Dead Time Insertion channel 1.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US3_RTS	0: PA5 1: PC1 2: PA14 3: PC15	4: PG5 5: PG11	USART3 Request To Send hardware flow control output.
US3_RX	0: PA1 1: PE7 2: PB7 3: PG7	4: PG1 5: PI13	USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PA0 1: PE6 2: PB3 3: PG6	4: PG0 5: PI12	USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI).
US4_CLK	0: PC4 1: PD11 2: PI2 3: PI8	4: PH6	USART4 clock input / output.
US4_CS	0: PC5 1: PD12 2: PI3 3: PI9	4: PH7	USART4 chip select input / output.
US4_CTS	0: PA7 1: PD13 2: PI4 3: PI10	4: PH8	USART4 Clear To Send hardware flow control input.
US4_RTS	0: PA8 1: PD14 2: PI5 3: PI11	4: PH9	USART4 Request To Send hardware flow control output.
US4_RX	0: PB8 1: PD10 2: PI1 3: PI7	4: PH5	USART4 Asynchronous Receive. USART4 Synchronous mode Master Input / Slave Output (MISO).
US4_TX	0: PB7 1: PD9 2: PI0 3: PI6	4: PH4	USART4 Asynchronous Transmit. Also used as receive input in half duplex communication. USART4 Synchronous mode Master Output / Slave Input (MOSI).
US5_CLK	0: PB11 1: PD13 2: PF13 3: PH12		USART5 clock input / output.
US5_CS	0: PB13 1: PD14 2: PF12 3: PH13		USART5 chip select input / output.
US5_CTS	0: PB14 1: PD15 2: PF11 3: PH14		USART5 Clear To Send hardware flow control input.
US5_RTS	0: PB12 1: PB15 2: PF10 3: PH15		USART5 Request To Send hardware flow control output.

Table 5.24. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP1X																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT0Y	BUSACMP1Y																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA3_OUT																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
OPA3_P																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
VDAC0_OUT0 / OPA0_OUT																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 6.2. BGA192 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.20	
C1		6.00	
C2		6.00	
E1		0.4	
E2		0.4	

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.2 BGA112 PCB Land Pattern

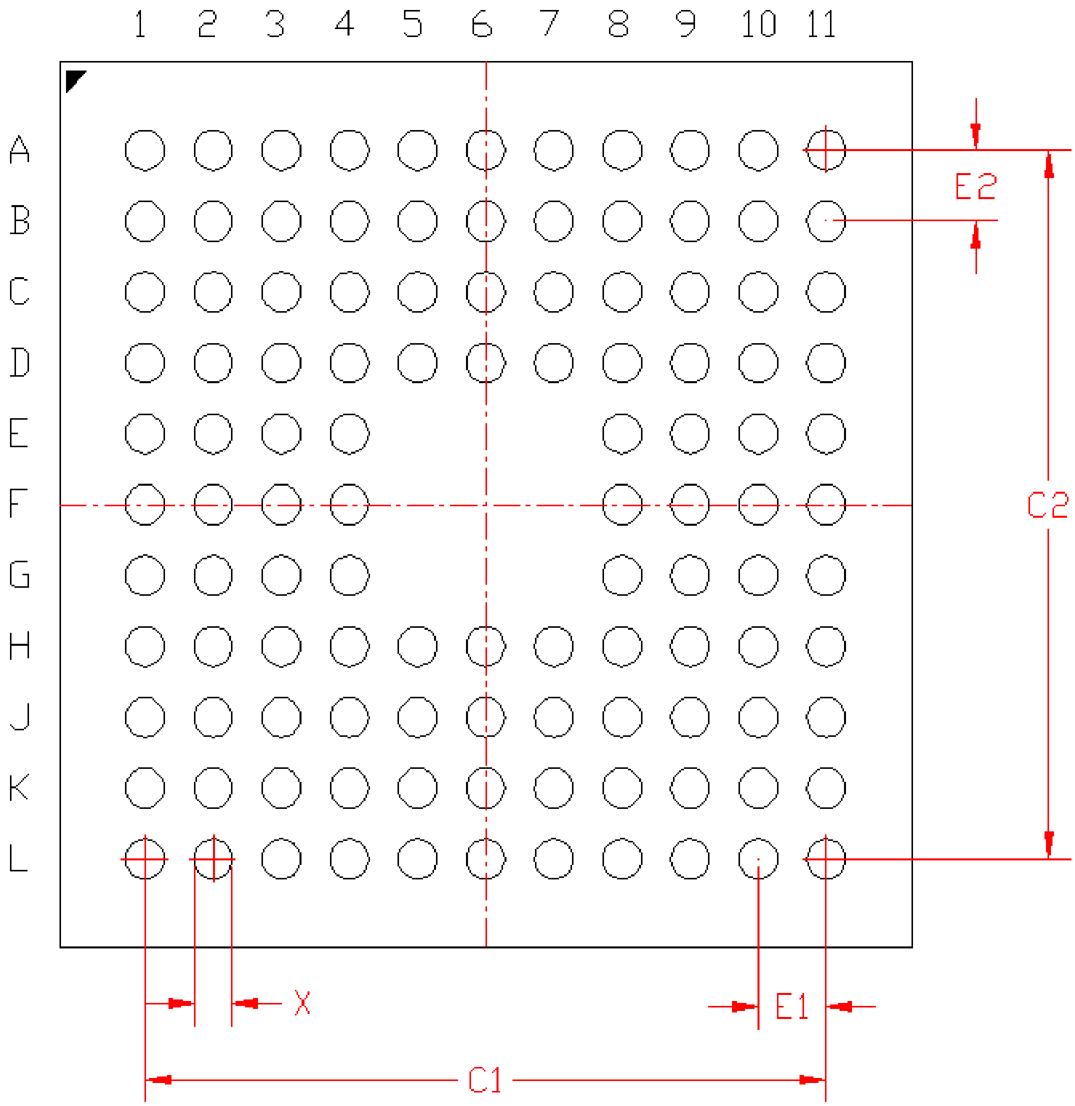

Figure 9.2. BGA112 PCB Land Pattern Drawing

Table 11.2. TQFP64 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11.3 TQFP64 Package Marking

Figure 11.3. TQFP64 Package Marking

The package marking consists of:
- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.