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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b510f2048gq64-br

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	USB	Ethernet	QSPI	SDIO	LCD	GPIO	Package	Temp Range
EFM32GG11B820F2048GL192-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85°C
EFM32GG11B840F1024GL192-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85°C
EFM32GG11B820F2048GL152-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +85°C
EFM32GG11B820F2048IL152-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +125°C
EFM32GG11B840F1024GL152-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +85°C
EFM32GG11B840F1024IL152-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +125°C
EFM32GG11B820F2048GL120-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +85°C
EFM32GG11B820F2048IL120-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +125°C
EFM32GG11B840F1024GL120-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +85°C
EFM32GG11B840F1024IL120-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +125°C
EFM32GG11B820F2048GQ100-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85°C
EFM32GG11B820F2048IQ100-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +125°C
EFM32GG11B840F1024GQ100-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85°C
EFM32GG11B840F1024IQ100-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +125°C
EFM32GG11B820F2048GQ64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +85°C
EFM32GG11B820F2048GM64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +85°C
EFM32GG11B820F2048IQ64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +125°C
EFM32GG11B820F2048IM64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +125°C
EFM32GG11B840F1024GQ64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +85°C
EFM32GG11B840F1024GM64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +85°C
EFM32GG11B840F1024IQ64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +125°C
EFM32GG11B840F1024IM64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +125°C
EFM32GG11B520F2048GL120-A	2048	512	Yes	No	No	No	No	Yes	95	BGA120	-40 to +85°C
EFM32GG11B510F2048GL120-A	2048	384	Yes	No	No	No	No	Yes	95	BGA120	-40 to +85°C
EFM32GG11B520F2048IL120-A	2048	512	Yes	No	No	No	No	Yes	95	BGA120	-40 to +125°C
EFM32GG11B510F2048IL120-A	2048	384	Yes	No	No	No	No	Yes	95	BGA120	-40 to +125°C
EFM32GG11B520F2048GQ100-A	2048	512	Yes	No	No	No	No	Yes	83	QFP100	-40 to +85°C
EFM32GG11B510F2048GQ100-A	2048	384	Yes	No	No	No	No	Yes	83	QFP100	-40 to +85°C
EFM32GG11B520F2048IQ100-A	2048	512	Yes	No	No	No	No	Yes	83	QFP100	-40 to +125°C
EFM32GG11B510F2048IQ100-A	2048	384	Yes	No	No	No	No	Yes	83	QFP100	-40 to +125°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	μs
Settling time, (output settled within 1% of steady state value),	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	μs
		Step value is changed	—	1	—	μs
Current consumption ²	I_{IDAC}	EM0 or EM1 Source mode, excluding output current, Across operating temperature range	—	11	TBD	μA
		EM0 or EM1 Sink mode, excluding output current, Across operating temperature range	—	13	TBD	μA
		EM2 or EM3 Source mode, excluding output current, T = 25 °C	—	0.05	—	μA
		EM2 or EM3 Sink mode, excluding output current, T = 25 °C	—	0.07	—	μA
		EM2 or EM3 Source mode, excluding output current, T $\geq$ 85 °C	—	11	—	μA
		EM2 or EM3 Sink mode, excluding output current, T $\geq$ 85 °C	—	13	—	μA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$	—	0.11	—	%
		RANGESEL1=1, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 100 \text{ mV})$	—	0.06	—	%
		RANGESEL1=2, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 150 \text{ mV})$	—	0.04	—	%
		RANGESEL1=3, output voltage = $\min(V_{IOVDD}, V_{AVDD}^2 - 250 \text{ mV})$	—	0.03	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.29	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.27	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.12	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.03	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

SPI Slave Timing

Table 4.35. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 3 2}	t_{SCLK}		$6 * t_{\text{HFERCLK}}$	—	—	ns
SCLK high time ^{1 3 2}	$t_{\text{SCLK_HI}}$		$2.5 * t_{\text{HFERCLK}}$	—	—	ns
SCLK low time ^{1 3 2}	$t_{\text{SCLK_LO}}$		$2.5 * t_{\text{HFERCLK}}$	—	—	ns
CS active to MISO ^{1 3}	$t_{\text{CS_ACT_MI}}$		24	—	69	ns
CS disable to MISO ^{1 3}	$t_{\text{CS_DIS_MI}}$		19	—	175	ns
MOSI setup time ^{1 3}	$t_{\text{SU_MO}}$		7	—	—	ns
MOSI hold time ^{1 3 2}	$t_{\text{H_MO}}$		6	—	—	ns
SCLK to MISO ^{1 3 2}	$t_{\text{SCLK_MI}}$		$16 + 1.5 * t_{\text{HFERCLK}}$	—	$43 + 2.5 * t_{\text{HFERCLK}}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. t_{HFERCLK} is one period of the selected HFERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

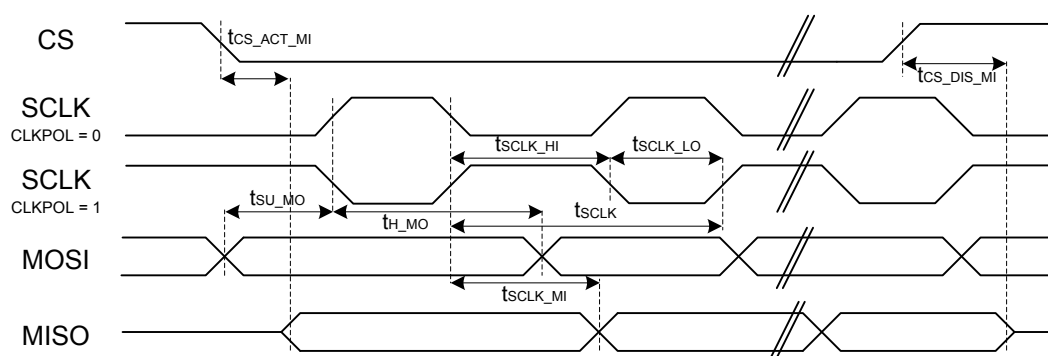


Figure 4.2. SPI Slave Timing Diagram

SDIO DDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 30 pF on all pins.

Table 4.49. SDIO DS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F _{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t _{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t _{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t _R		1.69	6.52	—	ns
Clock fall time	t _F		1.42	4.96	—	ns
Input setup time, CMD valid to SD_CLK	t _{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD change	t _{IH}		1.8	—	—	ns
Output delay time, SD_CLK to CMD valid	t _{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t _{OH}		0.8	—	—	ns
Input setup time, DAT[0:3] valid to SD_CLK	t _{ISU2X}		6	—	—	ns
Input hold time, SD_CLK to DAT[0:3] change	t _{IH2X}		1.5	—	—	ns
Output delay time, SD_CLK to DAT[0:3] valid	t _{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:3] change	t _{OH2X}		0.8	—	—	ns

QSPI SDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 34, RX DLL = 59, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.55. QSPI SDR Mode Timing (Locations 1, 2)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full SCLK period	T		$(1/F_{SCLK}) * 0.95$	—	—	ns
Output valid	t_{OV}		—	—	$T/2 - 2.1$	ns
Output hold	t_{OH}		$T/2 - 42.3$	—	—	ns
Input setup	t_{SU}		$48.2 - T/2$	—	—	ns
Input hold	t_H		$T/2 - 5.1$	—	—	ns

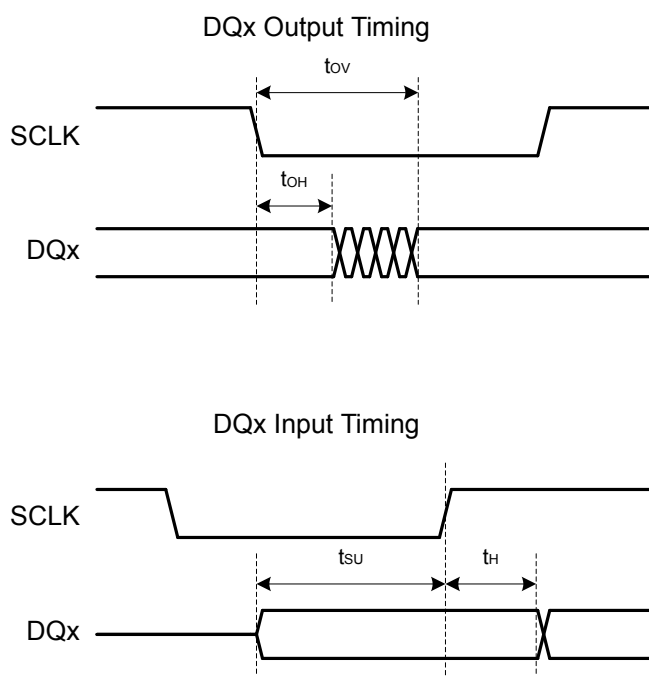


Figure 4.21. QSPI SDR Timing Diagrams

QSPI SDR Flash Timing Example

This example uses timing values for location 0 (SDR mode) to demonstrate the calculation of allowable flash timing using the QSPI in SDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 19 MHz:
- The resulting minimum period, $T(\min) = (1/F_{SCLK}) * 0.95 = 50.0$ ns.
- Flash will see a minimum setup time of $T/2 - t_{OV} = T/2 - (T/2 - 2.4) = 2.4$ ns.
- Flash will see a minimum hold time of $T/2 + t_{OH} = T/2 + (T/2 - 32.9) = T - 32.9 = 50.0 - 32.9 = 17.1$ ns.
- Flash can have a maximum output valid time of $T/2 - t_{SU} = T/2 - (36.2 - T/2) = T - 36.2 = 50.0 - 36.2 = 13.8$ ns.
- Flash can have a minimum output hold time of $t_H - T/2 = (T/2 - 3.3) - T/2 = -3.3$ ns.

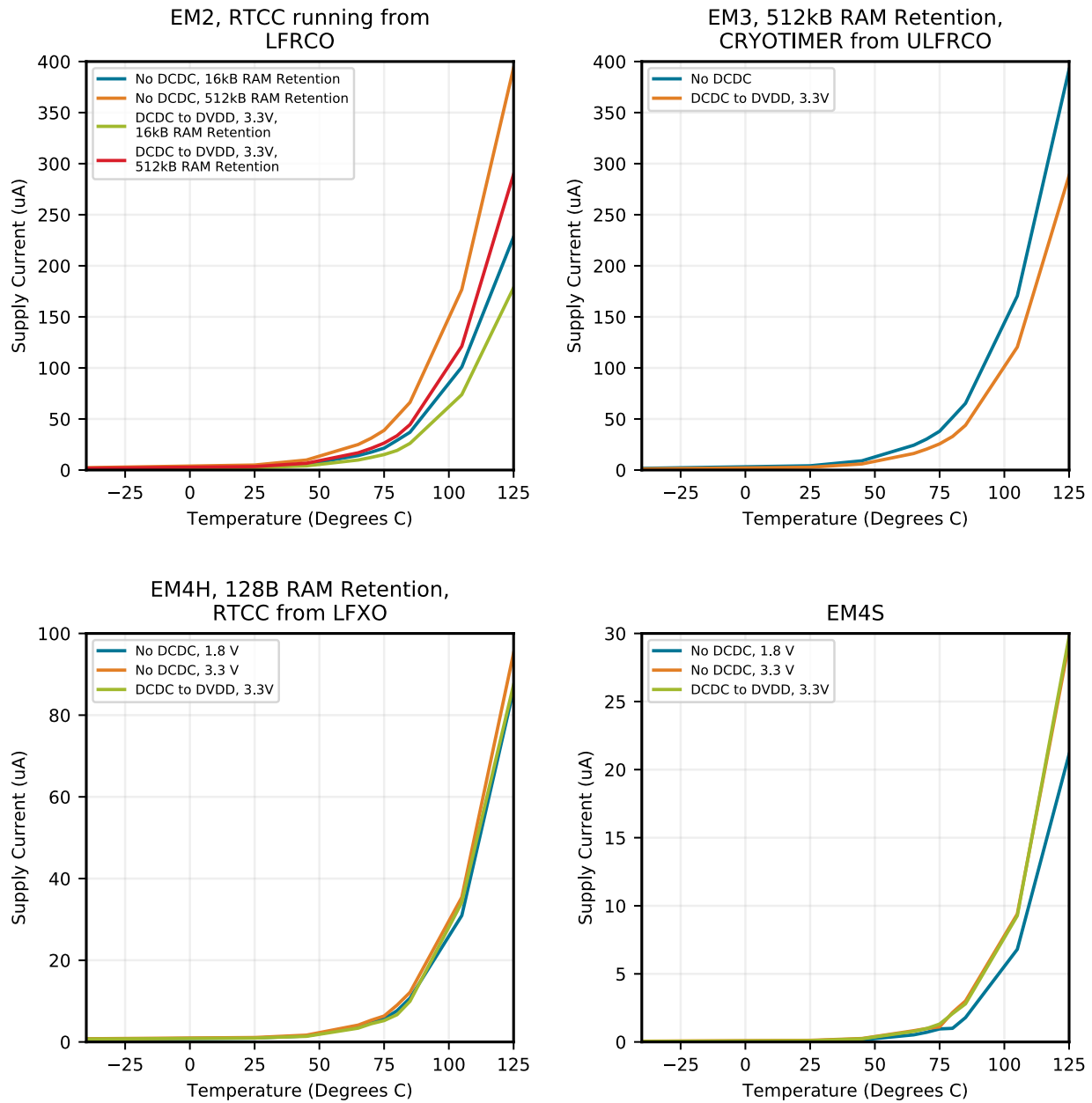


Figure 4.26. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VBUS	A13	USB VBUS signal and auxiliary input to 5 V regulator.	PF11	A14	GPIO (5V)
PF10	A15	GPIO (5V)	PF0	A16	GPIO (5V)
PA0	B1	GPIO	PD11	B2	GPIO
PD10	B3	GPIO	PD9	B4	GPIO
PF9	B5	GPIO	PF8	B6	GPIO
PF7	B7	GPIO	PF6	B8	GPIO
PI11	B9	GPIO (5V)	PI8	B10	GPIO (5V)
PF5	B11	GPIO	PF13	B12	GPIO (5V)
PF3	B13	GPIO	PF2	B14	GPIO
PF1	B15	GPIO (5V)	VREGO	B16	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PA1	C1	GPIO	PD12	C2	GPIO
PD14	C3	GPIO (5V)	PD13	C4	GPIO (5V)
PI15	C5	GPIO (5V)	PI14	C6	GPIO (5V)
PI13	C7	GPIO (5V)	PI12	C8	GPIO (5V)
PI10	C9	GPIO (5V)	PI7	C10	GPIO (5V)
PF15	C11	GPIO (5V)	PF12	C12	GPIO
PF4	C13	GPIO	PC15	C14	GPIO (5V)
PC14	C15	GPIO (5V)	VREGI	C16	Input to 5 V regulator.
PA2	D1	GPIO	PG0	D2	GPIO (5V)
PD15	D3	GPIO (5V)	PC13	D14	GPIO (5V)
PC12	D15	GPIO (5V)	PC11	D16	GPIO (5V)
PA3	E1	GPIO	PG2	E2	GPIO (5V)
PG1	E3	GPIO (5V)	PC10	E14	GPIO (5V)
PC9	E15	GPIO (5V)	PC8	E16	GPIO (5V)
PA4	F1	GPIO	PG4	F2	GPIO (5V)
PG3	F3	GPIO (5V)	IOVDD2	F6 G6	Digital IO power supply 2.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE8	B4	GPIO	PD11	B5	GPIO
PF8	B6	GPIO	PF6	B7	GPIO
PF3	B8	GPIO	PE5	B9	GPIO
PC12	B10	GPIO (5V)	PC13	B11	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
PD12	C5	GPIO	PF9	C6	GPIO
VSS	C7 D4 F9 G3 G9 H6 K4 K7 K10 L7	Ground	PF2	C8	GPIO
PE6	C9	GPIO	PC10	C10	GPIO (5V)
PC11	C11	GPIO (5V)	PA3	D1	GPIO
PA2	D2	GPIO	PB15	D3	GPIO (5V)
IOVDD1	D5	Digital IO power supply 1.	PD9	D6	GPIO
IOVDD0	D7 G8 H7 L4	Digital IO power supply 0.	PF1	D8	GPIO (5V)
PE7	D9	GPIO	PC8	D10	GPIO (5V)
PC9	D11	GPIO (5V)	PA6	E1	GPIO
PA5	E2	GPIO	PA4	E3	GPIO
PB0	E4	GPIO	PF0	E8	GPIO (5V)
PE0	E9	GPIO (5V)	PE1	E10	GPIO (5V)
PE3	E11	GPIO	PB1	F1	GPIO
PB2	F2	GPIO	PB3	F3	GPIO
PB4	F4	GPIO	DVDD	F8	Digital power supply.
PE2	F10	GPIO	DECOUPLE	F11	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PB5	G1	GPIO	PB6	G2	GPIO
IOVDD2	G4	Digital IO power supply 2.	PC6	G10	GPIO
PC7	G11	GPIO	PC0	H1	GPIO (5V)
PC2	H2	GPIO (5V)	PD14	H3	GPIO (5V)
PA7	H4	GPIO	PA8	H5	GPIO
PD8	H8	GPIO	PD5	H9	GPIO
PD6	H10	GPIO	PD7	H11	GPIO

5.20 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to [5.21 Alternate Functionality Overview](#) for a list of GPIO locations available for each function.

Table 5.20. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PA15	BUSAY BUSBX LCD_SEG12	EBI_AD08 #0	TIM3_CC2 #0	ETH_MIIRXCLK #0 ETH_MDIO #3 US2_CLK #3	PRS_CH15 #0
PE15	BUSCY BUSDX LCD_SEG11	EBI_AD07 #0	TIM2_CDTI2 #2 TIM3_CC1 #0	ETH_RMIITXD0 #0 ETH_MIIRXD3 #0 SDIO_CMD #1 US0_RTS #0 QSPI0_DQS #1 LEU0_RX #2	PRS_CH14 #2 ETM_TD3 #4
PE14	BUSDY BUSCX LCD_SEG10	EBI_AD06 #0	TIM2_CDTI1 #2 TIM3_CC0 #0	ETH_RMIITXD1 #0 ETH_MIIRXD2 #0 SDIO_CLK #1 US0_CTS #0 QSPI0_SCLK #1 LEU0_TX #2	PRS_CH13 #2 ETM_TD2 #4
PE13	BUSCY BUSDX LCD_SEG9	EBI_AD05 #0	TIM1_CC3 #1 TIM2_CC2 #3 LE- TIM0_OUT1 #4	SDIO_CLK #0 ETH_MIIRXD1 #0 US0_TX #3 US0_CS #0 U1_RX #4 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 ETM_TD1 #4 GPIO_EM4WU5
PE12	BUSDY BUSCX LCD_SEG8	EBI_AD04 #0	TIM1_CC2 #1 TIM2_CC1 #3 WTIM0_CDTI2 #0 LETIM0_OUT0 #4	SDIO_CMD #0 ETH_MIIRXD0 #0 US0_RX #3 US0_CLK #0 U1_TX #4 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_ALTEX6 PRS_CH1 #3 ETM_TD0 #4
PE11	BUSCY BUSDX LCD_SEG7	EBI_AD03 #0 EBI_CS3 #4	TIM1_CC1 #1 TIM4_CC2 #7 WTIM0_CDTI1 #0	SDIO_DAT0 #0 QSPI0_DQ7 #0 ETH_MIIRXDV #0 US0_RX #0	LES_ALTEX5 PRS_CH3 #2 ETM_TCLK #4
PE10	BUSDY BUSCX LCD_SEG6	EBI_AD02 #0 EBI_CS2 #4	TIM1_CC0 #1 TIM4_CC1 #7 WTIM0_CDTI0 #0	SDIO_DAT1 #0 QSPI0_DQ6 #0 ETH_MIIRXER #0 US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE9	BUSCY BUSDX LCD_SEG5	EBI_AD01 #0 EBI_CS1 #4	TIM4_CC0 #7 PCNT2_S1IN #1	SDIO_DAT2 #0 QSPI0_DQ5 #0 US5_RX #0	PRS_CH8 #2
PE8	BUSDY BUSCX LCD_SEG4	EBI_AD00 #0 EBI_CS0 #4	TIM2_CDTI0 #2 TIM4_CC2 #6 PCNT2_S0IN #1	SDIO_DAT3 #0 QSPI0_DQ4 #0 US5_TX #0 I2C2_SDA #0	PRS_CH3 #1
PI9		EBI_A14 #2	TIM1_CC3 #7 TIM4_CC1 #3	US4_CS #3	
PI6		EBI_A11 #2	TIM1_CC0 #7 TIM4_CC1 #2 WTIM3_CC0 #5	US4_TX #3	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF7	BUSCY BUSDX LCD_SEG25	EBI_BL1 #0 EBI_BL1 #4 EBI_BL1 #5 EBI_DCLK #1	TIM0_CC1 #1 TIM4_CC1 #4	ETH_RMIITXD0 #1 US2_RX #4 QSPI0_CS0 #0 ETH_MIIIRXER #2 US1_RX #3 U0_RX #0	PRS_CH23 #2
PF6	BUSDY BUSCX LCD_SEG24	EBI_BL0 #0 EBI_BL0 #4 EBI_BL0 #5 EBI_CSTFT #1	TIM0_CC0 #1 TIM4_CC0 #4 WTIM3_CC2 #5	ETH_RMIITXD1 #1 US2_TX #4 QSPI0_SCLK #0 US1_TX #3 U0_TX #0	PRS_CH22 #2
PI11				US4_RTS #3	
PI8		EBI_A13 #2	TIM1_CC2 #7 TIM4_CC0 #3	US4_CLK #3	
PF5	BUSCY BUSDX LCD_SEG3	EBI_REn #0 EBI_REn #5 EBI_A27 #1	TIM0_CDTI2 #2 TIM1_CC3 #6 TIM4_CC0 #2	US2_CS #5 I2C2_SCL #0 USB_VBUSEN	PRS_CH2 #1 DBG_TDI
PF13	BUSCY BUSDX		TIM1_CC0 #6 TIM4_CC0 #1 TIM5_CC1 #7 WTIM3_CC0 #7	US5_CLK #2 I2C2_SDA #4	
PF3	BUSCY BUSDX LCD_SEG1	EBI_ALE #0	TIM4_CC0 #0 TIM0_CDTI0 #2 TIM1_CC1 #5	CAN1_TX #1 US1_CTS #2 I2C2_SCL #5	CMU_CLK1 #4 PRS_CH0 #1 ETM_TD3 #1
PF2	BUSDY BUSCX LCD_SEG0	EBI_ARDY #0 EBI_A26 #1	TIM0_CC2 #4 TIM1_CC0 #5 TIM2_CC0 #3	US2_CLK #5 CAN0_TX #1 US1_TX #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO DBG_SWO #0 GPIO_EM4WU4
PF1	BUSCY BUSDX	EBI_A25 #1	TIM0_CC1 #4 WTIM0_CC2 #4 LE- TIM0_OUT1 #2	US2_RX #5 CAN1_RX #1 US1_CS #2 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PA1	BUSAY USBX LCD_SEG14	EBI_AD10 #0 EBI_DCLK #3	TIM0_CC0 #7 TIM0_CC1 #0 TIM3_CC1 #4 PCNT0_S1IN #4	ETH_RMIIRXD1 #0 ETH_MIIITXD3 #0 SDIO_DAT1 #1 US3_RX #0 QSPI0_CS1 #1 I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
PD12	LCD_SEG31	EBI_CS3 #0	TIM4_CC1 #6	ETH_RMIIRXER #1 SDIO_DAT4 #0 QSPI0_DQ3 #0 ETH_MIIIRXCLK #2 US4_CS #1	
PD14		EBI_NANDWEn #1	TIM2_CDTI1 #1 TIM3_CC2 #6 WTIM0_CC2 #1	ETH_MDC #1 CAN0_RX #5 US4_RTS #1 US5_CS #1 I2C0_SDA #3	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PB0	BUSBY BUSAX LCD_SEG32	EBI_AD00 #1 EBI_CS0 #3 EBI_A16 #0	TIM2_CDTI0 #0 TIM1_CC0 #2 TIM3_CC2 #7 WTIM0_CC0 #5 PCNT0_S0IN #5 PCNT1_S1IN #2	LEU1_TX #3	PRS_CH4 #1 ACMP0_O #5
PE0	BUSDY BUSCX	EBI_A00 #2 EBI_A07 #0	TIM3_CC0 #1 WTIM1_CC1 #3 PCNT0_S0IN #1	CAN0_RX #6 U0_TX #1 I2C1_SDA #2	PRS_CH22 #1 ACMP2_O #1
PC7	BUSACMP0Y BU- SACMP0X OPA3_N	EBI_A06 #0 EBI_A13 #1 EBI_A21 #3	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 LEU1_RX #0 I2C0_SCL #2	LES_CH7 PRS_CH15 #1 ETM_TD0 #2
PB1	BUSAY BUSBX LCD_SEG33	EBI_AD01 #1 EBI_CS1 #3 EBI_A17 #0	TIM2_CDTI1 #0 TIM1_CC1 #2 WTIM0_CC1 #5 LE- TIM1_OUT1 #5 PCNT0_S1IN #5	ETH_MIICRS #0 US5_RX #2 LEU1_RX #3	PRS_CH5 #1
PB2	BUSBY BUSAX LCD_SEG34	EBI_AD02 #1 EBI_CS2 #3 EBI_A18 #0	TIM2_CDTI2 #0 TIM1_CC2 #2 WTIM0_CC2 #5 LE- TIM1_OUT0 #5	ETH_MIICOL #0 US1_CS #6	PRS_CH18 #0 ACMP0_O #6
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	EBI_AD03 #1 EBI_CS3 #3 EBI_A19 #0	TIM1_CC3 #2 WTIM0_CC0 #6 PCNT1_S0IN #1	ETH_MIICRS #2 ETH_MDIO #0 SDIO_DAT6 #1 US2_TX #1 US3_TX #2 QSPI0_DQ4 #1	PRS_CH19 #0 ACMP0_O #7
PC6	BUSACMP0Y BU- SACMP0X OPA3_P	EBI_A05 #0	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 LEU1_TX #0 I2C0_SDA #2	LES_CH6 PRS_CH14 #1 ETM_TCLK #2
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	EBI_AD04 #1 EBI_ARDY #3 EBI_A20 #0	WTIM0_CC1 #6 PCNT1_S1IN #1	ETH_MIICOL #2 ETH_MDC #0 SDIO_DAT7 #1 US2_RX #1 QSPI0_DQ5 #1 LEU1_TX #4	PRS_CH20 #0
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	EBI_AD05 #1 EBI_ALE #3 EBI_A21 #0	WTIM0_CC2 #6 LE- TIM1_OUT0 #4 PCNT0_S0IN #6	ETH_TSUEXTCLK #0 US0_RTS #4 US2_CLK #1 QSPI0_DQ6 #1 LEU1_RX #4	PRS_CH21 #0
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	EBI_AD06 #1 EBI_WEn #3 EBI_A22 #0	TIM0_CC0 #3 TIM2_CC0 #4 WTIM3_CC0 #6 LE- TIM1_OUT1 #4 PCNT0_S1IN #6	ETH_TSUTMRTOG #0 US0_CTS #4 US2_CS #1 QSPI0_DQ7 #1	PRS_CH12 #1
PD5	BUSADC0Y BU- SADC0X OPA2_OUT	EBI_A09 #1 EBI_A18 #3	TIM6_CC1 #7 WTIM0_CDTI1 #4 WTIM1_CC3 #1 WTIM2_CC2 #5	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3	PRS_CH11 #2 ETM_TD3 #0 ETM_TD3 #2

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PB13	BUSAY BUSBX HFX TAL_P		TIM6_CC0 #5 WTIM1_CC0 #0 PCNT2_S0IN #2	US0_CLK #4 US1_CTS #5 US5_CS #0 LEU0_TX #1	CMU_CLKI0 #3 PRS_CH7 #0
PB14	BUSBY BUSAX HFX TAL_N		TIM6_CC1 #5 WTIM1_CC1 #0 PCNT2_S1IN #2	US0_CS #4 US1_RTS #5 US5_CTS #0 LEU0_RX #1	PRS_CH6 #1
PD1	VDAC0_OUT1ALT / OPA1_OUTALT #4 BUSADC0Y BU- SADC0X OPA3_OUT	EBI_A05 #1 EBI_A14 #3	TIM4_CDTI1 TIM0_CC0 #2 TIM6_CC0 #6 WTIM1_CC3 #0 PCNT2_S1IN #0	CAN0_TX #2 US1_RX #1	DBG_SWO #2
PD6	BUSADC0Y BU- SADC0X ADC0_EXTP VDAC0_EXT ADC1_EXTP OPA1_P	EBI_A10 #1 EBI_A19 #3	TIM1_CC0 #4 TIM6_CC2 #7 WTIM0_CDTI2 #4 WTIM1_CC0 #2 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US0_RTS #5 US1_RX #2 US2_CTS #5 US3_CTS #2 U0_RTS #5 I2C0_SDA #1	CMU_CLK2 #2 LES_ALTEX0 PRS_CH5 #2 ACMP0_O #2 ETM_TD0 #0

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG33	0: PB1		LCD segment line 33.
LCD_SEG34	0: PB2		LCD segment line 34.
LCD_SEG35	0: PA7		LCD segment line 35.
LCD_SEG36	0: PA8		LCD segment line 36.
LCD_SEG37	0: PA9		LCD segment line 37.
LCD_SEG38	0: PA10		LCD segment line 38.
LCD_SEG39	0: PA11		LCD segment line 39.
LES_ALTEX0	0: PD6		LESENSE alternate excite output 0.
LES_ALTEX1	0: PD7		LESENSE alternate excite output 1.
LES_ALTEX2	0: PA3		LESENSE alternate excite output 2.
LES_ALTEX3	0: PA4		LESENSE alternate excite output 3.
LES_ALTEX4	0: PA5		LESENSE alternate excite output 4.
LES_ALTEX5	0: PE11		LESENSE alternate excite output 5.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.
LES_CH0	0: PC0		LESENSE channel 0.
LES_CH1	0: PC1		LESENSE channel 1.
LES_CH2	0: PC2		LESENSE channel 2.
LES_CH3	0: PC3		LESENSE channel 3.
LES_CH4	0: PC4		LESENSE channel 4.
LES_CH5	0: PC5		LESENSE channel 5.
LES_CH6	0: PC6		LESENSE channel 6.
LES_CH7	0: PC7		LESENSE channel 7.
LES_CH8	0: PC8		LESENSE channel 8.
LES_CH9	0: PC9		LESENSE channel 9.
LES_CH10	0: PC10		LESENSE channel 10.

Table 5.24. ACMP1 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP1Y	BUSACMP1X	Bus
PF14	PF15	PF15	PF14	PB14	PB15	PB15	PB14			CH31
	PF13	PF13			PB13	PB13				CH30
PF12			PF12	PB12			PB12			CH29
	PF11	PF11			PB11	PB11				CH28
PF10			PF10	PB10			PB10			CH27
	PF9	PF9			PB9	PB9				CH26
PF8			PF8							CH25
	PF7	PF7								CH24
PF6			PF6	PB6			PB6			CH23
	PF5	PF5			PB5	PB5				CH22
PF4			PF4	PB4			PB4			CH21
	PF3	PF3			PB3	PB3				CH20
PF2			PF2	PB2			PB2			CH19
	PF1	PF1			PB1	PB1				CH18
PF0			PF0	PB0			PB0			CH17
	PE15	PE15			PA15	PA15				CH16
PE14			PE14	PA14			PA14			CH15
	PE13	PE13			PA13	PA13				CH14
PE12			PE12	PA12			PA12			CH13
	PE11	PE11			PA11	PA11				CH12
PE10			PE10	PA10			PA10			CH11
	PE9	PE9			PA9	PA9				CH10
PE8			PE8	PA8			PA8			CH9
	PE7	PE7			PA7	PA7				CH8
PE6			PE6	PA6			PA6	PC15	PC15	CH7
	PE5	PE5			PA5	PA5		PC14	PC14	CH6
PE4			PE4	PA4			PA4	PC13	PC13	CH5
					PA3	PA3		PC12	PC12	CH4
				PA2			PA2	PC11	PC11	CH3
	PE1	PE1			PA1	PA1		PC10	PC10	CH2
PE0			PE0	PA0			PA0	PC9	PC9	CH1
								PC8	PC8	CH0

Table 5.26. ACMP3 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP3Y	BUSACMP3X	Bus
PF14	PF15	PF15	PF14	PB14	PB15	PB15	PB14			CH31
	PF13	PF13			PB13	PB13				CH30
PF12			PF12	PB12			PB12			CH29
	PF11	PF11			PB11	PB11				CH28
PF10			PF10	PB10			PB10			CH27
	PF9	PF9			PB9	PB9				CH26
PF8			PF8							CH25
	PF7	PF7								CH24
PF6			PF6	PB6			PB6			CH23
	PF5	PF5			PB5	PB5				CH22
PF4			PF4	PB4			PB4			CH21
	PF3	PF3			PB3	PB3				CH20
PF2			PF2	PB2			PB2			CH19
	PF1	PF1			PB1	PB1				CH18
PF0			PF0	PB0			PB0			CH17
	PE15	PE15			PA15	PA15				CH16
PE14			PE14	PA14			PA14			CH15
	PE13	PE13			PA13	PA13				CH14
PE12			PE12	PA12			PA12			CH13
	PE11	PE11			PA11	PA11				CH12
PE10			PE10	PA10			PA10			CH11
	PE9	PE9			PA9	PA9				CH10
PE8			PE8	PA8			PA8			CH9
	PE7	PE7			PA7	PA7				CH8
PE6			PE6	PA6			PA6	PH15	PH15	CH7
	PE5	PE5			PA5	PA5		PH14	PH14	CH6
PE4			PE4	PA4			PA4	PH13	PH13	CH5
					PA3	PA3		PH12	PH12	CH4
				PA2			PA2	PH11	PH11	CH3
	PE1	PE1			PA1	PA1		PH10	PH10	CH2
PE0			PE0	PA0			PA0	PH9	PH9	CH1
								PH8	PH8	CH0

Table 8.1. BGA120 Package Dimensions

Dimension	Min	Typ	Max
A	0.78	0.84	0.90
A1	0.13	0.18	0.23
A3	0.17	0.21	0.25
A2	0.45 REF		
D	7.00 BSC		
e	0.50 BSC		
E	7.00 BSC		
D1	6.00 BSC		
E1	6.00 BSC		
b	0.20	0.25	0.30
aaa	0.10		
bbb	0.10		
ddd	0.08		
eee	0.15		
fff	0.05		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 9.2. BGA112 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.45	
C1		8.00	
C2		8.00	
E1		0.8	
E2		0.8	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10.2 TQFP100 PCB Land Pattern

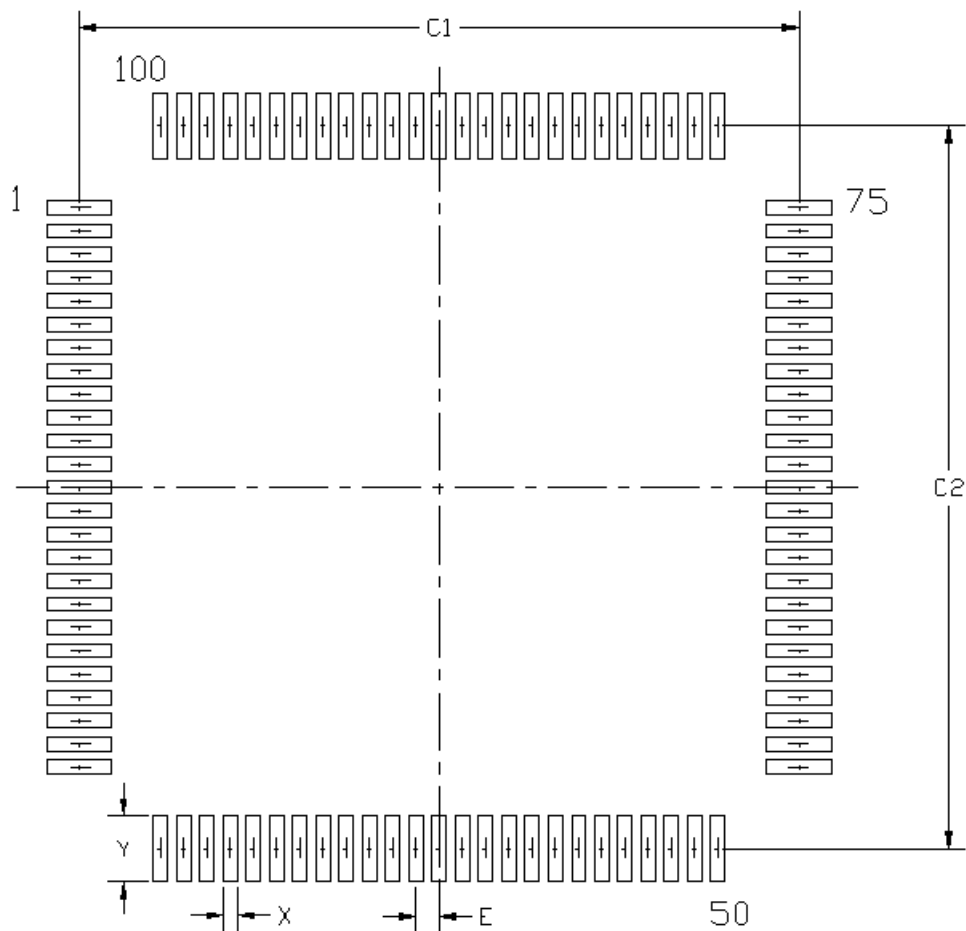


Figure 10.2. TQFP100 PCB Land Pattern Drawing

12. QFN64 Package Specifications

12.1 QFN64 Package Dimensions

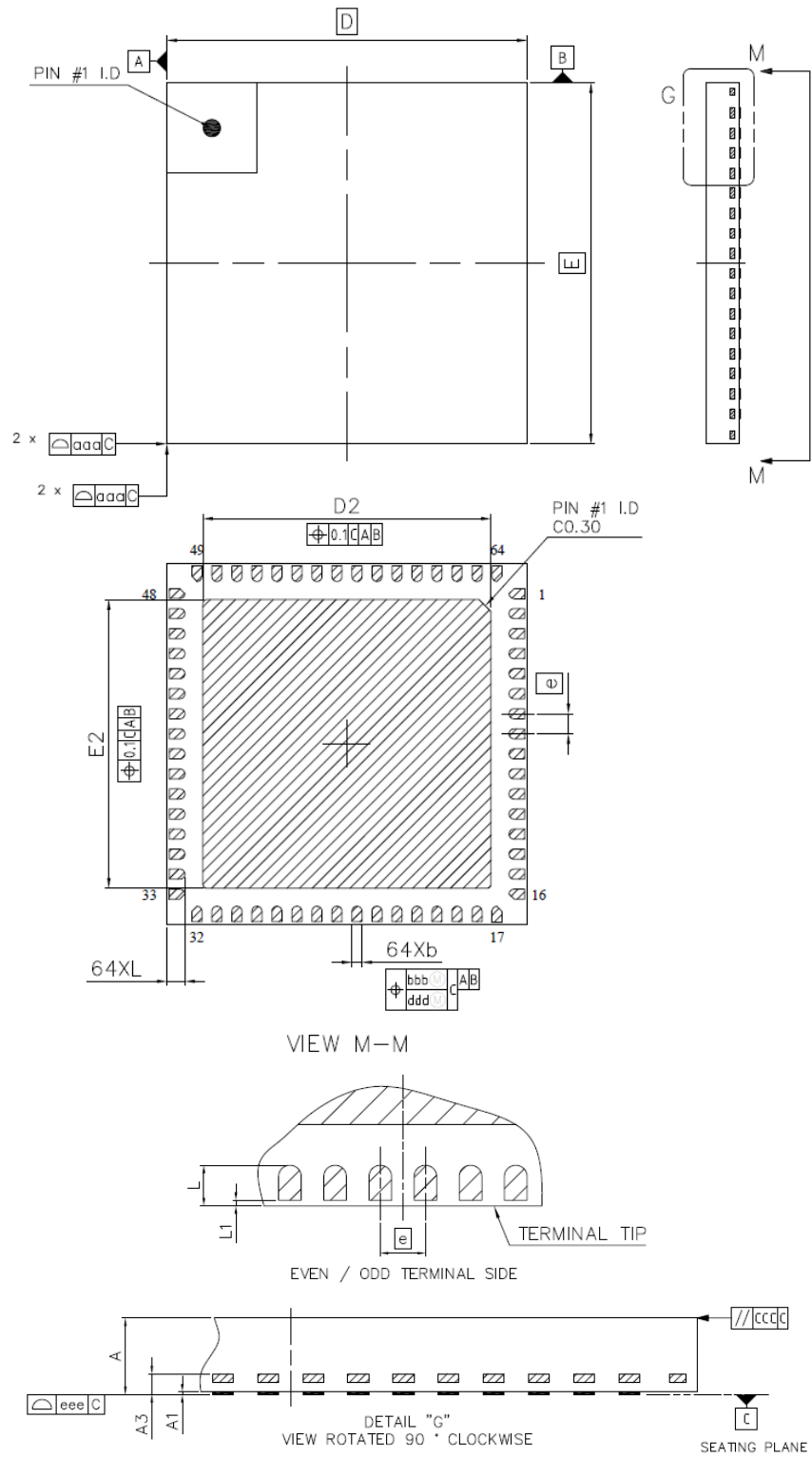


Figure 12.1. QFN64 Package Drawing