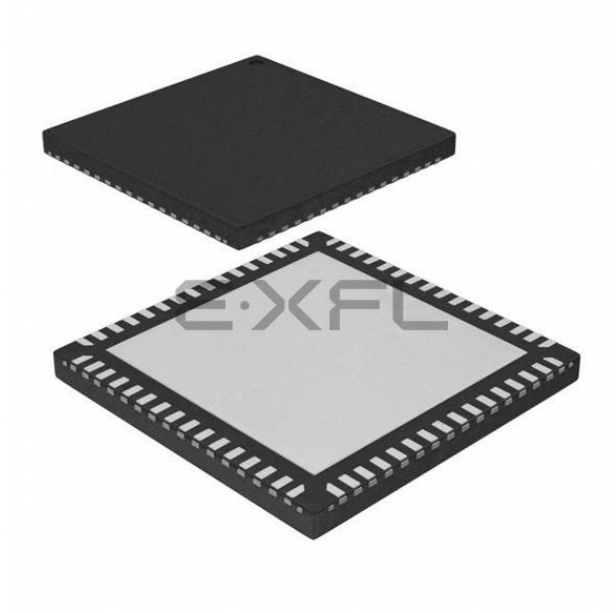

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b510f2048im64-a

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.10.4 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the [**Documentation**] area.

4.1.5 5V Regulator

V_{VREGI} = 5 V, V_{VREGO} = 3.3 V, C_{VREGI} = 10 µF, C_{VREGO} = 4.7 µF, unless otherwise specified.

Table 4.5. 5V Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VREGI or VBUS input voltage range	V_{VREGI}	Regulating output	2.7	—	5.5	V
		Bypass mode enabled	2.7	—	3.8	V
VREGO output voltage	V_{VREGO}	Regulating output, 3.3 V setting	3.1	3.3	3.5	V
		EM4S open-loop output, I_{OUT} < 100 µA	1.8	—	3.8	V
Voltage output step size	V_{VREGO_SS}		—	0.1	—	V
Resistance in Bypass Mode	R_{BYP}	Bypass mode enabled	—	1.2	TBD	Ω
Output current	I_{OUT}	EM0 or EM1, V_{VREGI} > V_{VREGO} + 0.6 V	—	—	200	mA
		EM0 or EM1, V_{VREGI} > V_{VREGO} + 0.3 V	—	—	100	mA
		EM2, EM3, or EM4H, V_{VREGI} > V_{VREGO} + 0.6 V	—	—	2	mA
		EM2, EM3, or EM4H, V_{VREGI} > V_{VREGO} + 0.3 V	—	—	0.5	mA
		EM4S	—	—	20	µA
Load regulation	LR_{VREGO}	EM0 or EM1	—	0.10	—	mV/mA
		EM2, EM3, or EM4H	—	2.5	—	mV/mA
DC power supply rejection	PSR_{DC}		—	40	—	dB
VREGI or VBUS bypass capacitance	C_{VREGI}		—	10	—	µF
VREGO bypass capacitance	C_{VREGO}		1	4.7	10	µF
Supply current consumption	I_{VREGI}	EM0 or EM1, No load	—	29	—	µA
		EM2, EM3, or EM4H, No load	—	270	—	nA
		EM4S, No load	—	70	—	nA
VREGI and VBUS detection high threshold	V_{DET_H}		TBD	1.18	—	V
VREGI and VBUS detection low threshold	V_{DET_L}		—	1.12	TBD	V
Current monitor transfer ratio	$IMON_{XF}$	Translation of current through VREGO path to voltage at ADC input	—	0.35	—	mA/mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode[3]	I_{ACTIVE_LPM}	32 MHz HFRCO, CPU running while loop from flash	—	82	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	83	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	88	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	257	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1]	$I_{ACTIVE\_CCM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	117	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1231	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode[3]	$I_{ACTIVE\_LPM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	72	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	219	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{EM1_DCM}	72 MHz HFRCO	—	42	—	µA/MHz
		50 MHz crystal	—	46	—	µA/MHz
		48 MHz HFRCO	—	46	—	µA/MHz
		32 MHz HFRCO	—	53	—	µA/MHz
		26 MHz HFRCO	—	57	—	µA/MHz
		16 MHz HFRCO	—	72	—	µA/MHz
		1 MHz HFRCO	—	663	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode[3]	I_{EM1_LPM}	32 MHz HFRCO	—	42	—	µA/MHz
		26 MHz HFRCO	—	43	—	µA/MHz
		16 MHz HFRCO	—	48	—	µA/MHz
		1 MHz HFRCO	—	219	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2]	$I_{EM1\_DCM\_VS}$	19 MHz HFRCO	—	60	—	µA/MHz
		1 MHz HFRCO	—	637	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode[3]	$I_{EM1\_LPM\_VS}$	19 MHz HFRCO	—	39	—	µA/MHz
		1 MHz HFRCO	—	190	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode[3]	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	2.8	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	3.1	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[5]	—	2.1	—	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.4	—	µA

4.1.9 Brown Out Detector (BOD)

Table 4.11. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	1.62	V
		DVDD falling (EM0/EM1)	1.35	—	—	V
		DVDD falling (EM2/EM3)	TBD	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	18	—	mV
DVDD BOD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	1.8	V
		AVDD falling (EM0/EM1)	1.62	—	—	V
		AVDD falling (EM2/EM3)	TBD	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	20	—	mV
AVDD BOD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	1.7	V
		AVDD falling	1.45	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	—	300	—	µs

4.1.10 Oscillators

4.1.10.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.12. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}		6	—	18	pF
On-chip tuning cap range [2]	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup [3]	I_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2, AGC[4] = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{LFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

4.1.10.6 USB High-Frequency RC Oscillator (USHFRCO)

Table 4.17. USB High-Frequency RC Oscillator (USHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{USHFRCO\_ACC}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
		USB clock recovery enabled, Active connection as device, FINETUNINGEN[1] = 1	-0.25	—	0.25	%
Start-up time	$t_{USHFRCO}$		—	300	—	ns
Current consumption on all supplies	$I_{USHFRCO}$	$f_{USHFRCO}$ = 48 MHz, FINETUNINGEN[1] = 1	—	340	TBD	µA
		$f_{USHFRCO}$ = 50 MHz, FINETUNINGEN[1] = 0	—	342	TBD	µA
		$f_{USHFRCO}$ = 48 MHz, FINETUNINGEN[1] = 0	—	292	TBD	µA
		$f_{USHFRCO}$ = 32 MHz, FINETUNINGEN[1] = 0	—	223	TBD	µA
		$f_{USHFRCO}$ = 16 MHz, FINETUNINGEN[1] = 0	—	132	TBD	µA
Period jitter	$PJ_{USHFRCO}$		—	0.2	—	% RMS

Note:
1. In the CMU_USHFRCOCTRL register.

4.1.10.7 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.18. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		TBD	1	TBD	kHz

EBI TFT Output Timing

All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.39. EBI TFT Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, EBI_DCLK to EBI_AD invalid	t_{OH_DCLK}	IOVDD ≥ 1.62 V	-23 + (TFTHOLD * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-12 + (TFTHOLD * $t_{HFCORECLK}$)	—	—	ns
Output setup time, EBI_AD valid to EBI_DCLK	t_{OSU_DCLK}	IOVDD ≥ 1.62 V	-11 + (TFTSETUP * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-9 + (TFTSETUP * $t_{HFCORECLK}$)	—	—	ns

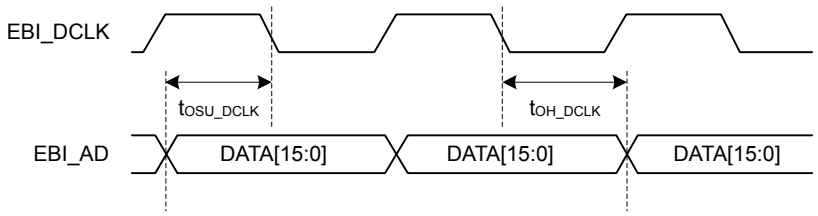

Figure 4.6. EBI TFT Output Timing

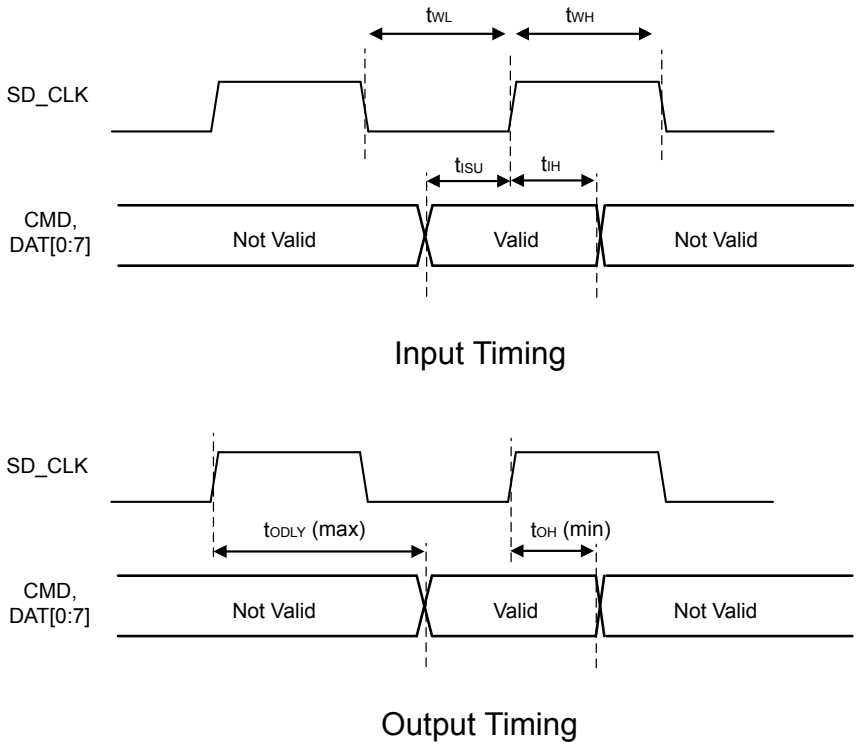

Figure 4.14. SDIO HS Mode Timing

5.2 EFM32GG11B8xx in BGA152 Device Pinout

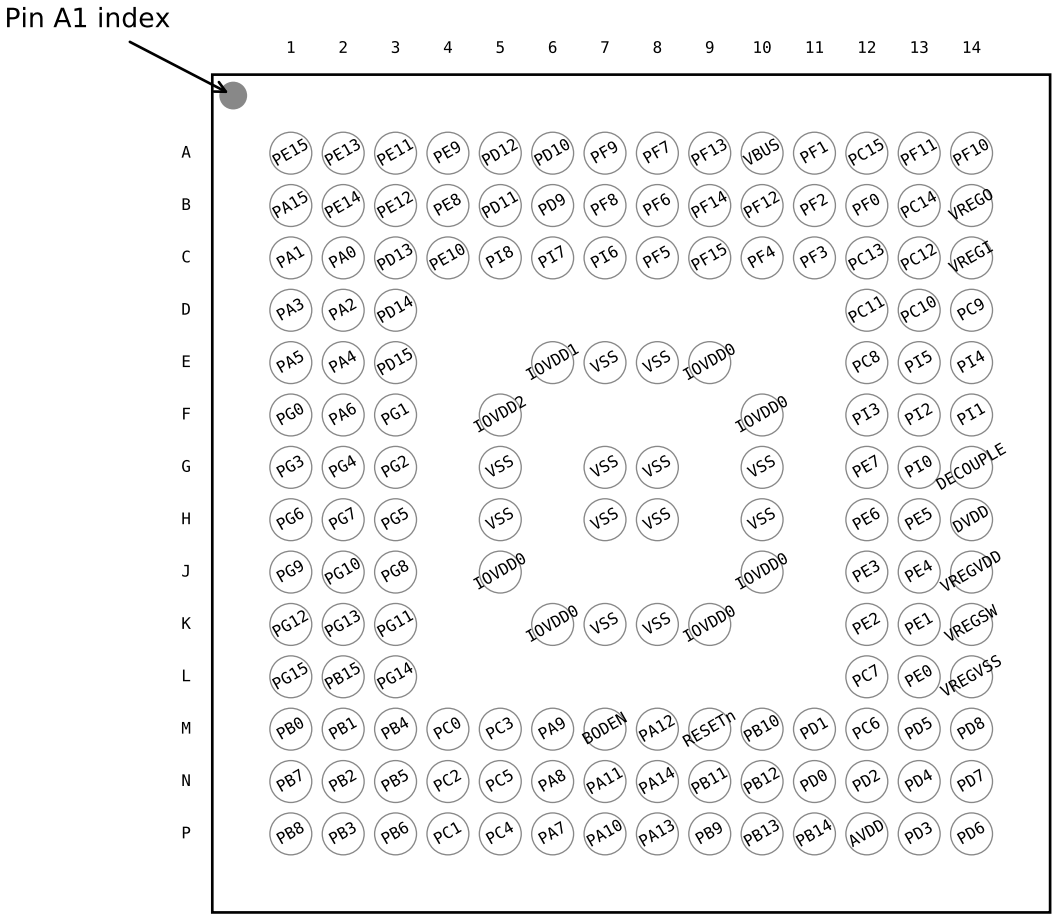

Figure 5.2. EFM32GG11B8xx in BGA152 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.2. EFM32GG11B8xx in BGA152 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE13	A2	GPIO
PE11	A3	GPIO	PE9	A4	GPIO
PD12	A5	GPIO	PD10	A6	GPIO
PF9	A7	GPIO	PF7	A8	GPIO
PF13	A9	GPIO (5V)	VBUS	A10	USB VBUS signal and auxiliary input to 5 V regulator.
PF1	A11	GPIO (5V)	PC15	A12	GPIO (5V)
PF11	A13	GPIO (5V)	PF10	A14	GPIO (5V)

5.3 EFM32GG11B8xx in BGA120 Device Pinout

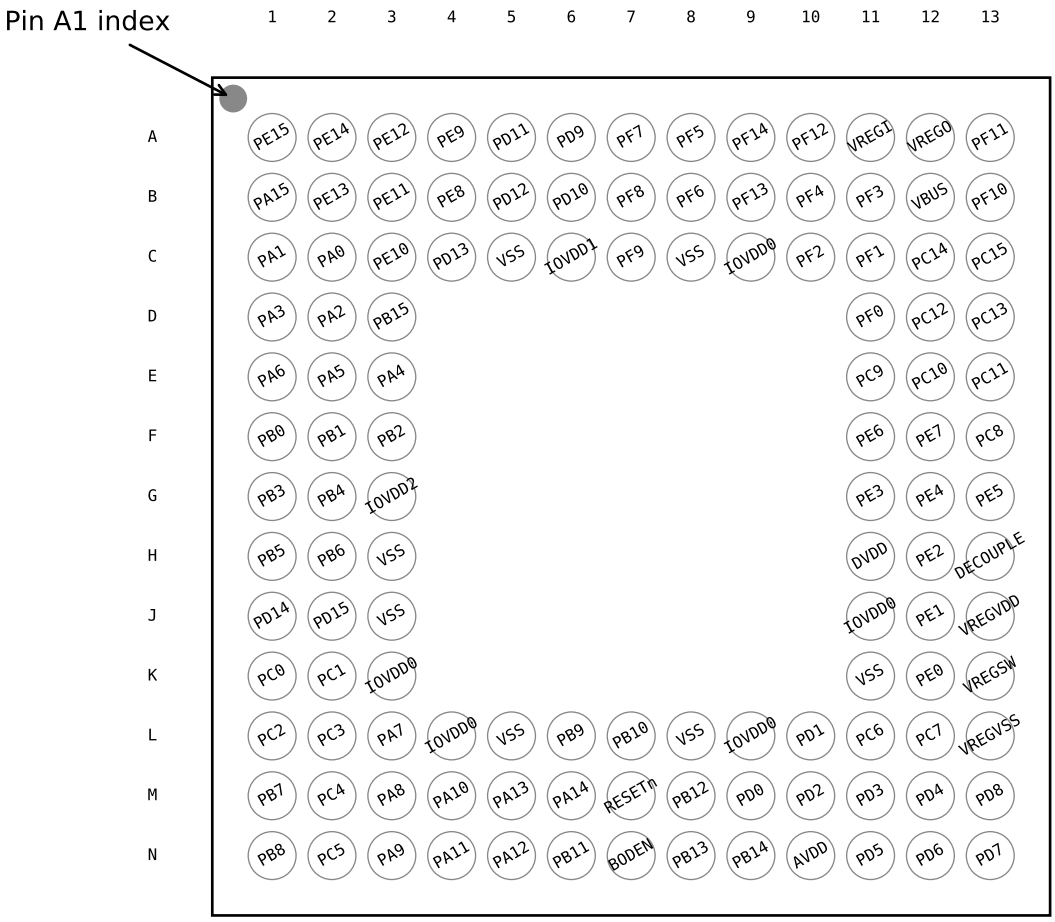

Figure 5.3. EFM32GG11B8xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.3. EFM32GG11B8xx in BGA120 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF14	A9	GPIO (5V)	PF12	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 59 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB9	37	GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	45	GPIO (5V)	PD1	46	GPIO
PD2	47	GPIO (5V)	PD3	48	GPIO
PD4	49	GPIO	PD5	50	GPIO
PD6	51	GPIO	PD7	52	GPIO
PD8	53	GPIO	PC7	54	GPIO
VREGVSS	55	Voltage regulator VSS	VREGSW	56	DCDC regulator switching node
VREGVDD	57	Voltage regulator VDD input	DVDD	58	Digital power supply.
DECOUPLE	60	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE1	61	GPIO (5V)
PE2	62	GPIO	PE3	63	GPIO
PE4	64	GPIO	PE5	65	GPIO
PE6	66	GPIO	PE7	67	GPIO
PC8	68	GPIO (5V)	PC9	69	GPIO (5V)
PC10	70	GPIO (5V)	PC11	71	GPIO (5V)
VREGI	72	Input to 5 V regulator.	VREGO	73	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PF10	74	GPIO (5V)	PF11	75	GPIO (5V)
PF0	76	GPIO (5V)	PF1	77	GPIO (5V)

5.13 EFM32GG11B5xx in QFP64 Device Pinout

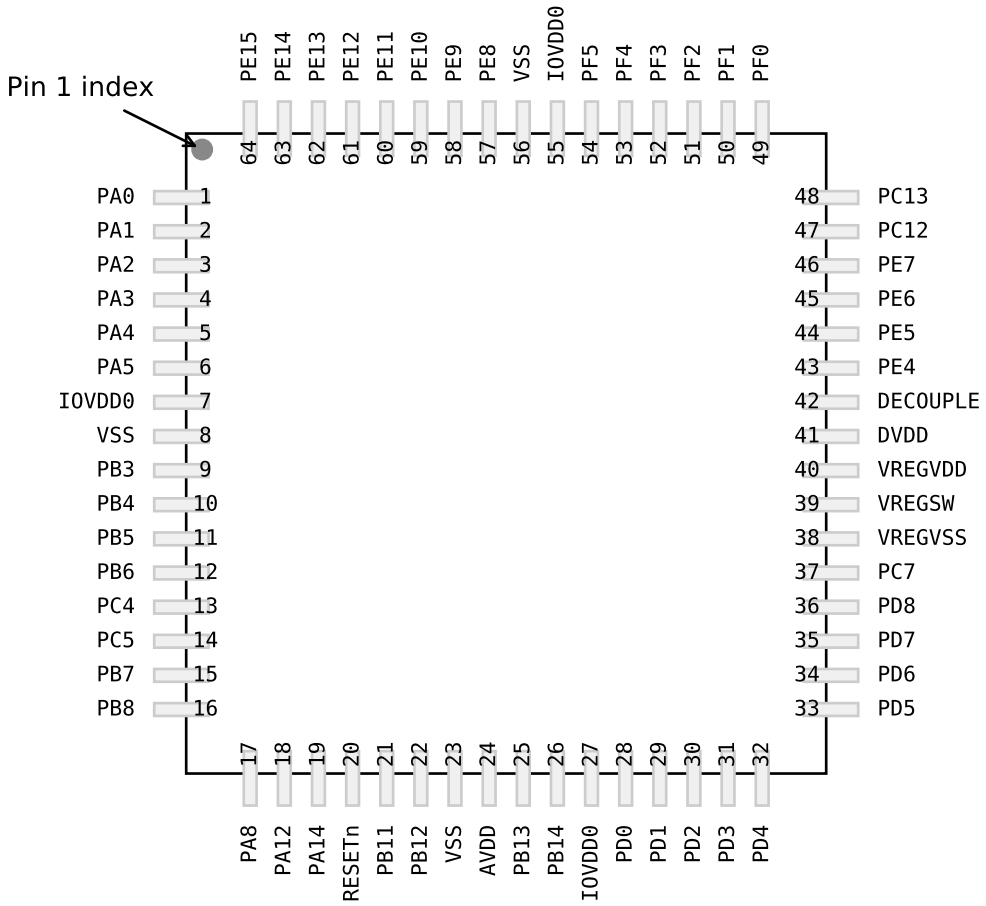

Figure 5.13. EFM32GG11B5xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.13. EFM32GG11B5xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO (5V)
PC9	42	GPIO (5V)	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
BU_STAT	0: PE3		Backup Power Domain status, whether or not the system is in backup mode.
BU_VIN	0: PD8		Battery input for Backup Power Domain.
BU_VOUT	0: PE2		Power output for Backup Power Domain.
CAN0_RX	0: PC0 1: PF0 2: PD0 3: PB9	4: PG8 5: PD14 6: PE0 7: PI12	CAN0 RX.
CAN0_TX	0: PC1 1: PF2 2: PD1 3: PB10	4: PG9 5: PD15 6: PE1 7: PI13	CAN0 TX.
CAN1_RX	0: PC2 1: PF1 2: PD3 3: PC9	4: PC12 5: PA12 6: PG10 7: PI14	CAN1 RX.
CAN1_TX	0: PC3 1: PF3 2: PD4 3: PC10	4: PC11 5: PA13 6: PG11 7: PI15	CAN1 TX.
CMU_CLK0	0: PA2 1: PC12 2: PD7 3: PG2	4: PF2 5: PA12	Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA1 1: PD8 2: PE12 3: PG1	4: PF3 5: PB11	Clock Management Unit, clock output number 1.
CMU_CLK2	0: PA0 1: PA3 2: PD6 3: PG0	4: PA3 5: PD10	Clock Management Unit, clock output number 2.
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	4: PE1 5: PD10 6: PE12 7: PB11	Clock Management Unit, clock input number 0.
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_AD08	0: PA15 1: PC1 2: PG8		External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	0: PA0 1: PC2 2: PG9		External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	0: PA1 1: PC3 2: PG10		External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	0: PA2 1: PC4 2: PG11		External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	0: PA3 1: PC5 2: PG12		External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	0: PA4 1: PA7 2: PG13		External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	0: PA5 1: PA8 2: PG14		External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	0: PA6 1: PA9 2: PG15		External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	0: PF3 1: PB9 2: PC4 3: PB5	4: PC11 5: PC11	External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	0: PF2 1: PD13 2: PB15 3: PB4	4: PC13 5: PF10	External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	0: PF6 1: PF8 2: PB10 3: PC1	4: PF6 5: PF6	External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	0: PF7 1: PF9 2: PB11 3: PC3	4: PF7 5: PF7	External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	0: PD9 1: PA10 2: PC0 3: PB0	4: PE8	External Bus Interface (EBI) Chip Select output 0.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_MIITXD2	0: PA2 1: PG2		Ethernet MII Transmit Data Bit 2.
ETH_MIITXD3	0: PA1 1: PG1		Ethernet MII Transmit Data Bit 3.
ETH_MIITXEN	0: PA5 1: PG5		Ethernet MII Transmit Enable.
ETH_MIITXER	0: PA6 1: PG6		Ethernet MII Transmit Error.
ETH_RMIICRSDV	0: PA4 1: PD11		Ethernet RMII Carrier Sense / Data Valid.
ETH_RMIIREFCLK	0: PA3 1: PD10		Ethernet RMII Reference Clock.
ETH_RMIIRXD0	0: PA2 1: PD9		Ethernet RMII Receive Data Bit 0.
ETH_RMIIRXD1	0: PA1 1: PF9		Ethernet RMII Receive Data Bit 1.
ETH_RMIIRXER	0: PA5 1: PD12		Ethernet RMII Receive Error.
ETH_RMIITXD0	0: PE15 1: PF7		Ethernet RMII Transmit Data Bit 0.
ETH_RMIITXD1	0: PE14 1: PF6		Ethernet RMII Transmit Data Bit 1.
ETH_RMIITXEN	0: PA0 1: PF8		Ethernet RMII Transmit Enable.
ETH_TSUEXTCLK	0: PB5 1: PD15 2: PC2 3: PF8		Ethernet IEEE1588 External Reference Clock.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US3_RTS	0: PA5 1: PC1 2: PA14 3: PC15	4: PG5 5: PG11	USART3 Request To Send hardware flow control output.
US3_RX	0: PA1 1: PE7 2: PB7 3: PG7	4: PG1 5: PI13	USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PA0 1: PE6 2: PB3 3: PG6	4: PG0 5: PI12	USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI).
US4_CLK	0: PC4 1: PD11 2: PI2 3: PI8	4: PH6	USART4 clock input / output.
US4_CS	0: PC5 1: PD12 2: PI3 3: PI9	4: PH7	USART4 chip select input / output.
US4_CTS	0: PA7 1: PD13 2: PI4 3: PI10	4: PH8	USART4 Clear To Send hardware flow control input.
US4_RTS	0: PA8 1: PD14 2: PI5 3: PI11	4: PH9	USART4 Request To Send hardware flow control output.
US4_RX	0: PB8 1: PD10 2: PI1 3: PI7	4: PH5	USART4 Asynchronous Receive. USART4 Synchronous mode Master Input / Slave Output (MISO).
US4_TX	0: PB7 1: PD9 2: PI0 3: PI6	4: PH4	USART4 Asynchronous Transmit. Also used as receive input in half duplex communication. USART4 Synchronous mode Master Output / Slave Input (MOSI).
US5_CLK	0: PB11 1: PD13 2: PF13 3: PH12		USART5 clock input / output.
US5_CS	0: PB13 1: PD14 2: PF12 3: PH13		USART5 chip select input / output.
US5_CTS	0: PB14 1: PD15 2: PF11 3: PH14		USART5 Clear To Send hardware flow control input.
US5_RTS	0: PB12 1: PB15 2: PF10 3: PH15		USART5 Request To Send hardware flow control output.

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
VDAC0_OUT1 / OPA1_OUT																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

9. BGA112 Package Specifications

9.1 BGA112 Package Dimensions

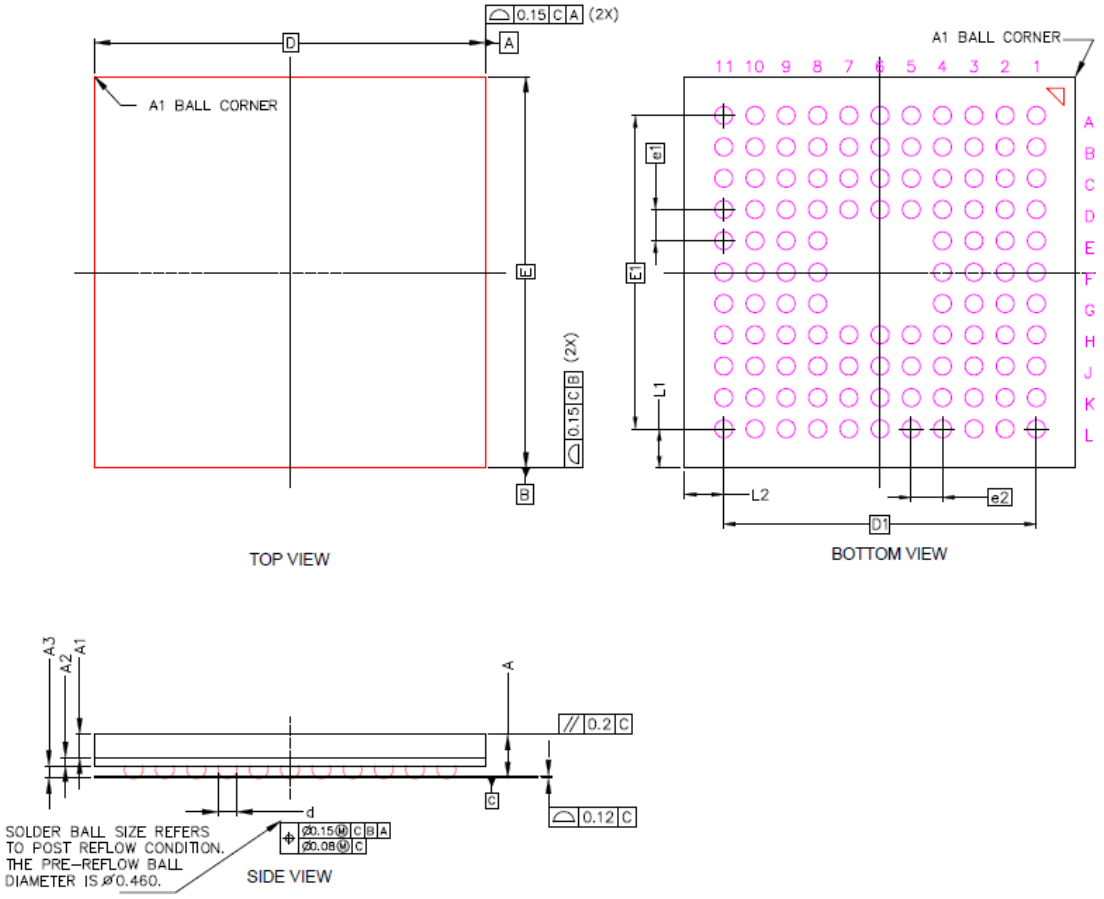

Figure 9.1. BGA112 Package Drawing