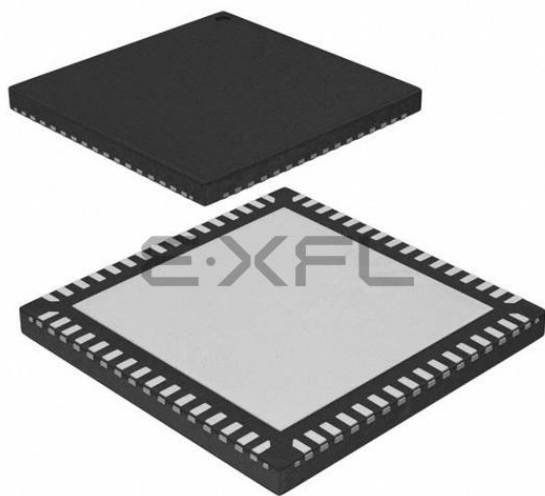




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b510f2048im64-b

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3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Giant Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only privileged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output fall time, From 70% to 30% of V_{IO}	t_{IOF}	$C_L = 50\text{ pF}$, DRIVESTRENGTH ¹ = STRONG, SLEWRATE ¹ = 0x6	—	1.8	—	ns
		$C_L = 50\text{ pF}$, DRIVESTRENGTH ¹ = WEAK, SLEWRATE ¹ = 0x6	—	4.5	—	ns
Output rise time, From 30% to 70% of V_{IO}	t_{IOR}	$C_L = 50\text{ pF}$, DRIVESTRENGTH ¹ = STRONG, SLEWRATE = 0x6 ¹	—	2.2	—	ns
		$C_L = 50\text{ pF}$, DRIVESTRENGTH ¹ = WEAK, SLEWRATE ¹ = 0x6	—	7.4	—	ns

Note:
1. In GPIO_Pn_CTRL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis ($V_{CM} = 1.25\text{ V}$, $BIASPROG^4 = 0x10$, $FULLBIAS^4 = 1$)	$V_{ACMPHYST}$	$HYSTSEL^5 = HYST0$	TBD	0	TBD	mV
		$HYSTSEL^5 = HYST1$	TBD	18	TBD	mV
		$HYSTSEL^5 = HYST2$	TBD	33	TBD	mV
		$HYSTSEL^5 = HYST3$	TBD	46	TBD	mV
		$HYSTSEL^5 = HYST4$	TBD	57	TBD	mV
		$HYSTSEL^5 = HYST5$	TBD	68	TBD	mV
		$HYSTSEL^5 = HYST6$	TBD	79	TBD	mV
		$HYSTSEL^5 = HYST7$	TBD	90	TBD	mV
		$HYSTSEL^5 = HYST8$	TBD	0	TBD	mV
		$HYSTSEL^5 = HYST9$	TBD	-18	TBD	mV
		$HYSTSEL^5 = HYST10$	TBD	-33	TBD	mV
		$HYSTSEL^5 = HYST11$	TBD	-45	TBD	mV
		$HYSTSEL^5 = HYST12$	TBD	-57	TBD	mV
		$HYSTSEL^5 = HYST13$	TBD	-67	TBD	mV
		$HYSTSEL^5 = HYST14$	TBD	-78	TBD	mV
		$HYSTSEL^5 = HYST15$	TBD	-88	TBD	mV
Comparator delay ³	$t_{ACMPDELAY}$	$BIASPROG^4 = 1$, $FULLBIAS^4 = 0$	—	30	—	μs
		$BIASPROG^4 = 0x10$, $FULLBIAS^4 = 0$	—	3.7	—	μs
		$BIASPROG^4 = 0x02$, $FULLBIAS^4 = 1$	—	360	—	ns
		$BIASPROG^4 = 0x20$, $FULLBIAS^4 = 1$	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	$BIASPROG^4 = 0x10$, $FULLBIAS^4 = 1$	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	$CSRESSEL^6 = 0$	—	infinite	—	k Ω
		$CSRESSEL^6 = 1$	—	15	—	k Ω
		$CSRESSEL^6 = 2$	—	27	—	k Ω
		$CSRESSEL^6 = 3$	—	39	—	k Ω
		$CSRESSEL^6 = 4$	—	51	—	k Ω
		$CSRESSEL^6 = 5$	—	100	—	k Ω
		$CSRESSEL^6 = 6$	—	162	—	k Ω
		$CSRESSEL^6 = 7$	—	235	—	k Ω

4.1.21 Pulse Counter (PCNT)

Table 4.29. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.22 Analog Port (APORT)

Table 4.30. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current ^{2 1}	I_{APORT}	Operation in EM0/EM1	—	7	—	μA
		Operation in EM2/EM3	—	915	—	nA

Note:

- Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by multiplying the duty cycle of the requests by the specified continuous current number.
- Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

4.1.23.3 I2C Fast-mode Plus (Fm+)¹

Table 4.33. I2C Fast-mode Plus (Fm+)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f _{SCL}		0	—	1000	kHz
SCL clock low time	t _{LOW}		0.5	—	—	μs
SCL clock high time	t _{HIGH}		0.26	—	—	μs
SDA set-up time	t _{SU_DAT}		50	—	—	ns
SDA hold time	t _{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t _{SU_STA}		0.26	—	—	μs
(Repeated) START condition hold time	t _{HD_STA}		0.26	—	—	μs
STOP condition set-up time	t _{SU_STO}		0.26	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		0.5	—	—	μs

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HPPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

MII Receive Timing

Timing is specified with $3.0\text{ V} \leq \text{IOVDD} \leq 3.8\text{ V}$, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.43. Ethernet MII Receive Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX_CLK frequency	$F_{\text{RX_CLK}}$		—	25	—	MHz
RX_CLK duty cycle	$\text{DC}_{\text{RX_CLK}}$		35	—	65	%
Setup time, RXD[3:0], RX_DV, RX_ER valid to RX_CLK	t_{SU}		6	—	—	ns
Hold time, RX_CLK to RXD[3:0], RX_DV, RX_ER change	t_{HD}		5	—	—	ns

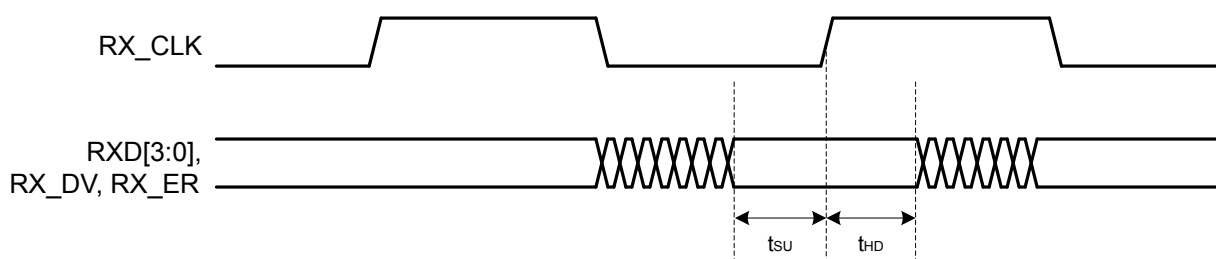


Figure 4.10. Ethernet MII Receive Timing

RMII Transmit Timing

Timing is specified with $3.0\text{ V} \leq \text{IOVDD} \leq 3.8\text{ V}$, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.44. Ethernet RMII Transmit Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REF_CLK frequency	$F_{\text{REF_CLK}}$	Output slew rate set to 7	—	50	—	MHz
REF_CLK duty cycle	$\text{DC}_{\text{REF_CLK}}$		35	—	65	%
Output delay, REF_CLK to TXD[1:0], TX_EN	t_{OUT}		2.3	—	14.1	ns

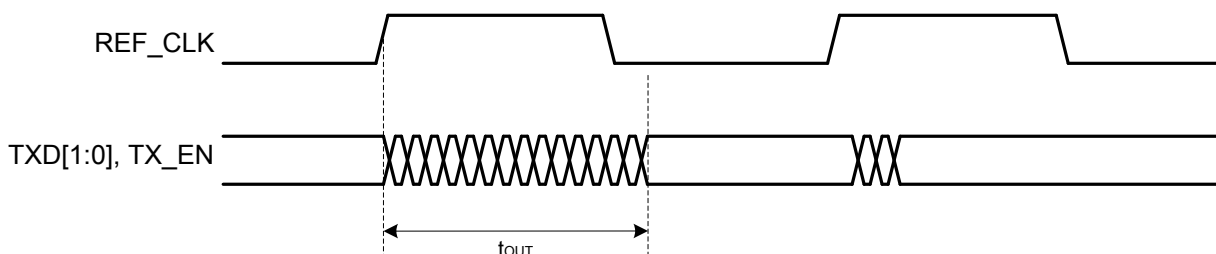


Figure 4.11. Ethernet RMII Transmit Timing

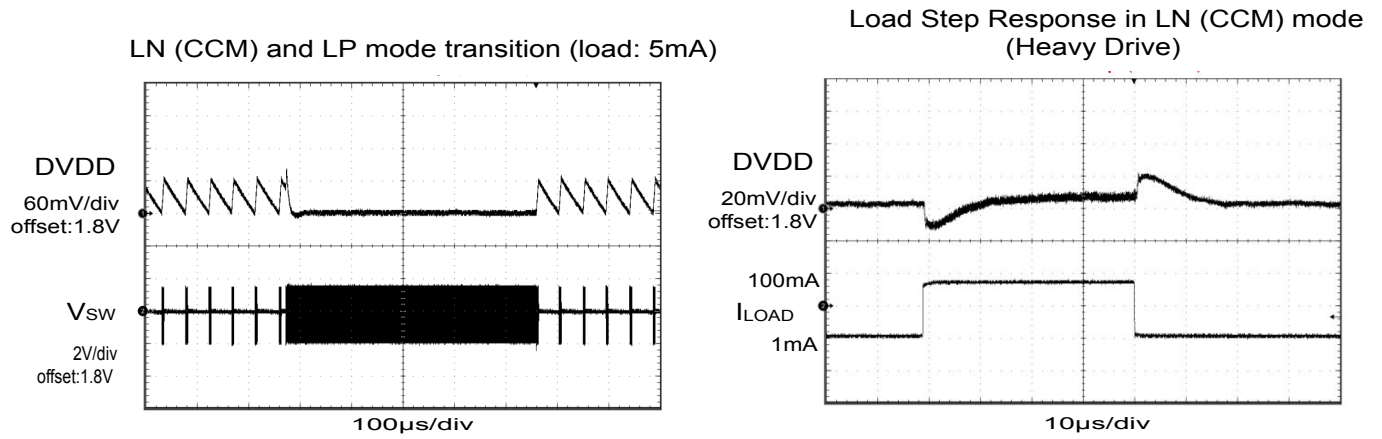


Figure 4.30. DC-DC Converter Transition Waveforms

5.5 EFM32GG11B4xx in BGA120 Device Pinout

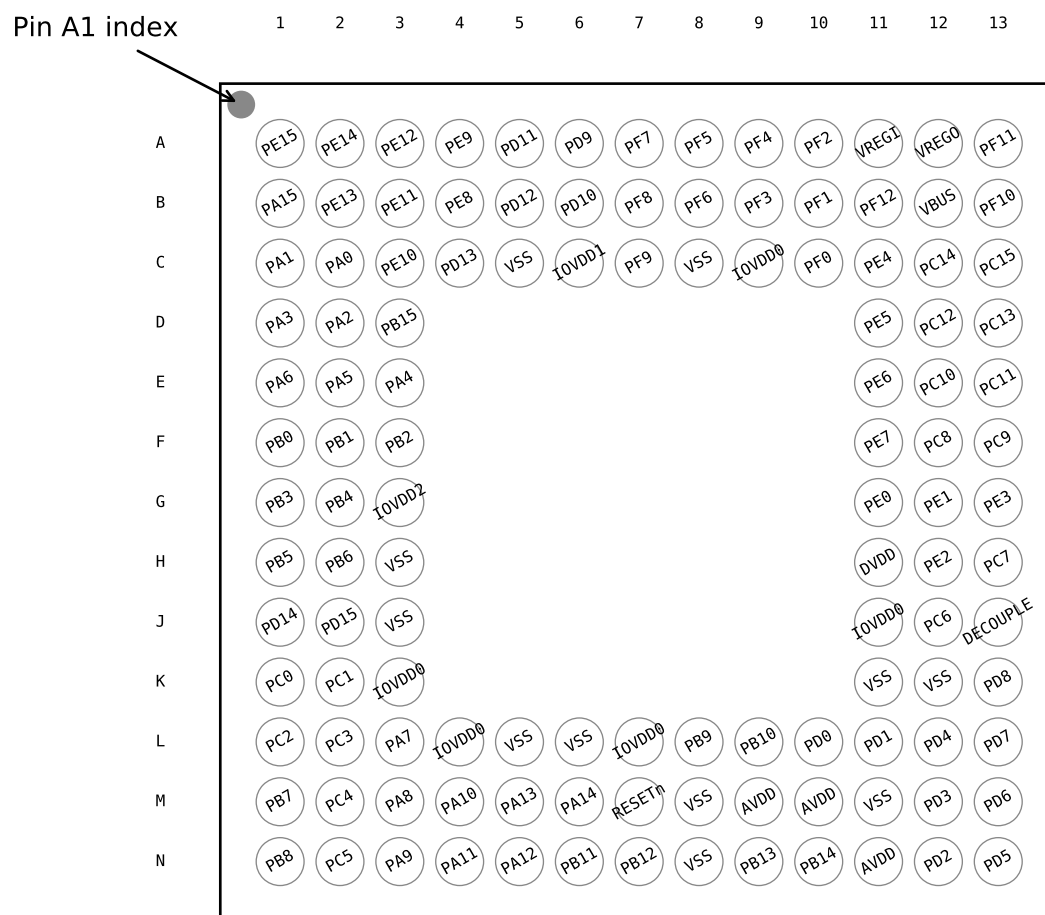


Figure 5.5. EFM32GG11B4xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.5. EFM32GG11B4xx in BGA120 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF4	A9	GPIO	PF2	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF3	B9	GPIO
PF1	B10	GPIO (5V)	PF12	B11	GPIO
VBUS	B12	USB VBUS signal and auxiliary input to 5 V regulator.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 K12 L12 L13 M8 M11 N8	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L14	Digital IO power supply 0.
PF0	C10	GPIO (5V)	PE4	C11	GPIO
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PE5	D11	GPIO
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PE6	E11	GPIO
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE7	F11	GPIO
PC8	F12	GPIO (5V)	PC9	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE0	G11	GPIO (5V)
PE1	G12	GPIO (5V)	PE3	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
PC7	H13	GPIO	PD14	J1	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF1	77	GPIO (5V)	PF2	78	GPIO
VBUS	79	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	80	GPIO
PF5	81	GPIO	PF6	84	GPIO
PF7	85	GPIO	PF8	86	GPIO
PF9	87	GPIO	PD9	88	GPIO
PD10	89	GPIO	PD11	90	GPIO
PD12	91	GPIO	PE8	92	GPIO
PE9	93	GPIO	PE10	94	GPIO
PE11	95	GPIO	PE12	96	GPIO
PE13	97	GPIO	PE14	98	GPIO
PE15	99	GPIO	PA15	100	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.11 EFM32GG11B3xx in QFP100 Device Pinout

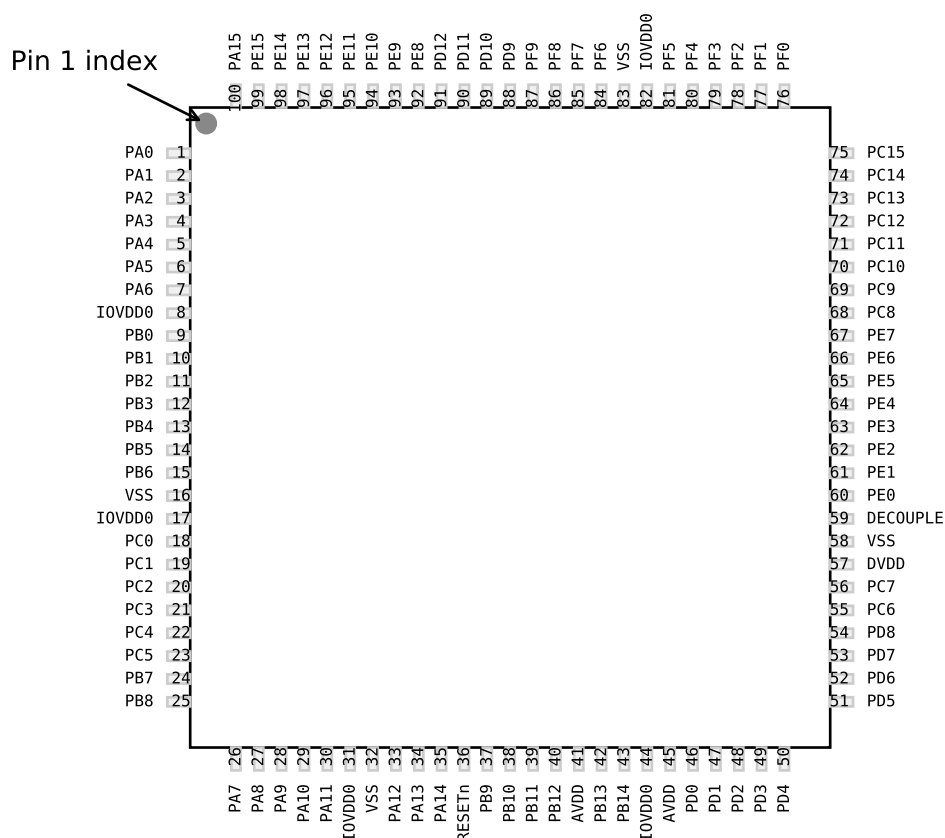


Figure 5.11. EFM32GG11B3xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.11. EFM32GG11B3xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF14	BUSDY BUSCX		TIM1_CC1 #6 TIM4_CC1 #1 TIM5_CC2 #7 WTIM3_CC1 #7	I2C2_SCL #4	
PF11	BUSCY BUSDX	EBI_NANDWE _n #5	TIM5_CC2 #6 WTIM3_CC2 #3 PCNT2_S1IN #3	US5_CTS #2 U1_RX #1 I2C2_SCL #2 USB_DP	
PF10	BUSDY BUSCX	EBI_ARDY #5	TIM5_CC1 #6 WTIM3_CC1 #3 PCNT2_S0IN #3	US5_RTS #2 U1_TX #1 I2C2_SDA #2 USB_DM	
PF0	BUSDY BUSCX	EBI_A24 #1	TIM0_CC0 #4 WTIM0_CC1 #4 LE- TIM0_OUT0 #2	US2_TX #5 CAN0_RX #1 US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	PRS_CH15 #2 ACMP3_O #0 DBG_SWCLKTCK BOOT_TX
PA0	BUSBY BUSAX LCD_SEG13	EBI_AD09 #0 EBI_CSTFT #3	TIM0_CC0 #0 TIM0_CC1 #7 TIM3_CC0 #4 PCNT0_S0IN #4	ETH_RMIITXEN #0 ETH_MII_TXCLK #0 SDIO_DAT0 #1 US1_RX #5 US3_TX #0 QSPI0_CS0 #1 LEU0_RX #4 I2C0_SDA #0	CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
PD11	LCD_SEG30	EBI_CS2 #0 EBI_HSNC #1	TIM4_CC0 #6 WTIM3_CC2 #0	ETH_RMIICRS _{SDV} #1 SDIO_DAT5 #0 QSPI0_DQ2 #0 ETH_MII_RXD3 #2 US4_CLK #1	
PD10	LCD_SEG29	EBI_CS1 #0 EBI_VSNC #1	TIM4_CC2 #5 WTIM3_CC1 #0	ETH_RMIIREFCLK #1 SDIO_DAT6 #0 QSPI0_DQ1 #0 ETH_MII_RXD2 #2 US4_RX #1	CMU_CLK2 #5 CMU_CLKI0 #5
PD9	LCD_SEG28	EBI_CS0 #0 EBI_DTEN #1	TIM4_CC1 #5 WTIM3_CC0 #0	ETH_RMIIRXD0 #1 SDIO_DAT7 #0 QSPI0_DQ0 #0 ETH_MII_RXD1 #2 US4_TX #1	
PF9	BUSCY BUSDX LCD_SEG27	EBI_RE _n #4 EBI_BL1 #1	TIM4_CC0 #5	ETH_RMIIRXD1 #1 US2_CS #4 QSPI0_DQS #0 ETH_MII_RXD0 #2 ETH_TSUTMRTOG #3 SDIO_WP #0 U0_RTS #0 U1_CTS #1	ETM_TD0 #1
PF8	BUSDY BUSCX LCD_SEG26	EBI_WE _n #4 EBI_BL0 #1	TIM0_CC2 #1 TIM4_CC2 #4	ETH_RMIITXEN #1 US2_CLK #4 QSPI0_CS1 #0 ETH_MII_RXDV #2 ETH_TSUEXTCLK #3 SDIO_CD #0 U0_CTS #0 U1_RTS #1	ETM_TCLK #1 GPIO_EM4WU8

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF7	BUSCY BUSDX LCD_SEG25	EBI_BL1 #0 EBI_BL1 #4 EBI_BL1 #5 EBI_DCLK #1	TIM0_CC1 #1 TIM4_CC1 #4	ETH_RMIITXD0 #1 US2_RX #4 QSPI0_CS0 #0 ETH_MIIIRXER #2 US1_RX #3 U0_RX #0	PRS_CH23 #2
PF6	BUSDY BUSCX LCD_SEG24	EBI_BL0 #0 EBI_BL0 #4 EBI_BL0 #5 EBI_CSTFT #1	TIM0_CC0 #1 TIM4_CC0 #4 WTIM3_CC2 #5	ETH_RMIITXD1 #1 US2_TX #4 QSPI0_SCLK #0 US1_TX #3 U0_TX #0	PRS_CH22 #2
PI11				US4_RTS #3	
PI8		EBI_A13 #2	TIM1_CC2 #7 TIM4_CC0 #3	US4_CLK #3	
PF5	BUSCY BUSDX LCD_SEG3	EBI_REn #0 EBI_REn #5 EBI_A27 #1	TIM0_CDTI2 #2 TIM1_CC3 #6 TIM4_CC0 #2	US2_CS #5 I2C2_SCL #0 USB_VBUSEN	PRS_CH2 #1 DBG_TDI
PF13	BUSCY BUSDX		TIM1_CC0 #6 TIM4_CC0 #1 TIM5_CC1 #7 WTIM3_CC0 #7	US5_CLK #2 I2C2_SDA #4	
PF3	BUSCY BUSDX LCD_SEG1	EBI_ALE #0	TIM4_CC0 #0 TIM0_CDTI0 #2 TIM1_CC1 #5	CAN1_TX #1 US1_CTS #2 I2C2_SCL #5	CMU_CLK1 #4 PRS_CH0 #1 ETM_TD3 #1
PF2	BUSDY BUSCX LCD_SEG0	EBI_ARDY #0 EBI_A26 #1	TIM0_CC2 #4 TIM1_CC0 #5 TIM2_CC0 #3	US2_CLK #5 CAN0_TX #1 US1_TX #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO DBG_SWO #0 GPIO_EM4WU4
PF1	BUSCY BUSDX	EBI_A25 #1	TIM0_CC1 #4 WTIM0_CC2 #4 LE- TIM0_OUT1 #2	US2_RX #5 CAN1_RX #1 US1_CS #2 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PA1	BUSAY USBX LCD_SEG14	EBI_AD10 #0 EBI_DCLK #3	TIM0_CC0 #7 TIM0_CC1 #0 TIM3_CC1 #4 PCNT0_S1IN #4	ETH_RMIIRXD1 #0 ETH_MIIITXD3 #0 SDIO_DAT1 #1 US3_RX #0 QSPI0_CS1 #1 I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
PD12	LCD_SEG31	EBI_CS3 #0	TIM4_CC1 #6	ETH_RMIIRXER #1 SDIO_DAT4 #0 QSPI0_DQ3 #0 ETH_MIIIRXCLK #2 US4_CS #1	
PD14		EBI_NANDWEn #1	TIM2_CDTI1 #1 TIM3_CC2 #6 WTIM0_CC2 #1	ETH_MDC #1 CAN0_RX #5 US4_RTS #1 US5_CS #1 I2C0_SDA #3	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_AD08	0: PA15 1: PC1 2: PG8		External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	0: PA0 1: PC2 2: PG9		External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	0: PA1 1: PC3 2: PG10		External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	0: PA2 1: PC4 2: PG11		External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	0: PA3 1: PC5 2: PG12		External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	0: PA4 1: PA7 2: PG13		External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	0: PA5 1: PA8 2: PG14		External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	0: PA6 1: PA9 2: PG15		External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	0: PF3 1: PB9 2: PC4 3: PB5	4: PC11 5: PC11	External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	0: PF2 1: PD13 2: PB15 3: PB4	4: PC13 5: PF10	External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	0: PF6 1: PF8 2: PB10 3: PC1	4: PF6 5: PF6	External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	0: PF7 1: PF9 2: PB11 3: PC3	4: PF7 5: PF7	External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	0: PD9 1: PA10 2: PC0 3: PB0	4: PE8	External Bus Interface (EBI) Chip Select output 0.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_TSUTMR-TOG	0: PB6 1: PB15 2: PC3 3: PF9		Ethernet IEEE1588 Timer Toggle.
ETM_TCLK	0: PD7 1: PF8 2: PC6 3: PA6	4: PE11 5: PG15	Embedded Trace Module ETM clock .
ETM_TD0	0: PD6 1: PF9 2: PC7 3: PA2	4: PE12 5: PG14	Embedded Trace Module ETM data 0.
ETM_TD1	0: PD3 1: PD13 2: PD3 3: PA3	4: PE13 5: PG13	Embedded Trace Module ETM data 1.
ETM_TD2	0: PD4 1: PB15 2: PD4 3: PA4	4: PE14 5: PG12	Embedded Trace Module ETM data 2.
ETM_TD3	0: PD5 1: PF3 2: PD5 3: PA5	4: PE15 5: PG11	Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.
LES_CH0	0: PC0		LESENSE channel 0.
LES_CH1	0: PC1		LESENSE channel 1.
LES_CH2	0: PC2		LESENSE channel 2.
LES_CH3	0: PC3		LESENSE channel 3.
LES_CH4	0: PC4		LESENSE channel 4.
LES_CH5	0: PC5		LESENSE channel 5.
LES_CH6	0: PC6		LESENSE channel 6.
LES_CH7	0: PC7		LESENSE channel 7.
LES_CH8	0: PC8		LESENSE channel 8.
LES_CH9	0: PC9		LESENSE channel 9.
LES_CH10	0: PC10		LESENSE channel 10.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US5_RX	0: PE9 1: PA7 2: PB1 3: PH11		USART5 Asynchronous Receive. USART5 Synchronous mode Master Input / Slave Output (MISO).
US5_TX	0: PE8 1: PA6 2: PF15 3: PH10		USART5 Asynchronous Transmit. Also used as receive input in half duplex communication. USART5 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	0: PF10		USB D- pin.
USB_DP	0: PF11		USB D+ pin.
USB_ID	0: PF12		USB ID pin.
USB_VBUSEN	0: PF5		USB 5 V VBUS enable.
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6 2: PG2 3: PG8	4: PC15 5: PB0 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5 1: PD13 2: PG3 3: PG9	4: PF0 5: PB1 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	
OPA2_OUT																																		
APORT1Y	BUSAY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	
APORT3Y	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	
APORT4Y	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	
APORT1X	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	
APORT2X	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	
APORT3X	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	
APORT4X	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	
APORT1N	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	
APORT2N	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	
APORT3N	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	
APORT4N	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	
APORT1Y	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	BUSAY	
APORT2Y	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	BUSBY	
APORT3Y	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY	BUSCY
APORT4Y	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY
APORT1X	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX	BUSAX
APORT2X	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX	BUSBX
APORT3X	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX	BUSCX
APORT4X	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY
APORT1N	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN	BUSAN
APORT2N	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN	BUSBN
APORT3N	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN	BUSCN
APORT4N	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSD

8. BGA120 Package Specifications

8.1 BGA120 Package Dimensions

