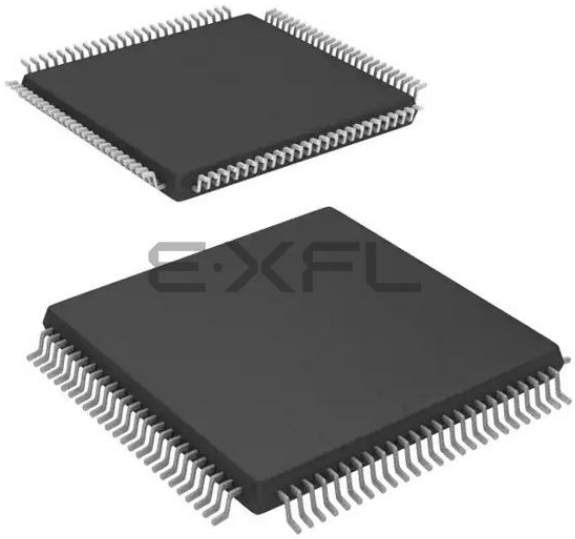
Silicon Labs - EFM32GG11B510F2048IQ100-AR Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b510f2048iq100-ar

1. Feature List

The EFM32GG11 highlighted features are listed below.

- **ARM Cortex-M4 CPU platform**
  - High performance 32-bit processor @ up to 72 MHz
  - DSP instruction support and Floating Point Unit
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 80 µA/MHz in Active Mode (EM0)
  - 2.1 µA EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Up to 2048 kB flash program memory**
  - Dual-bank with read-while-write support
- **Up to 512 kB RAM data memory**
  - 256 kB with ECC (SEC-DED)
- **Octal/Quad-SPI Flash Memory Interface**
  - Supports 3 V and 1.8 V memories
  - 1/2/4/8-bit data bus
  - Quad-SPI Execute In Place (XIP)
- **Communication Interfaces**
  - Low-energy Universal Serial Bus (USB) with Device and Host support
    - Fully USB 2.0 compliant
    - On-chip PHY and embedded 5V to 3.3V regulator
    - Crystal-free Device mode operation
    - Patent-pending Low-Energy Mode (LEM)
  - SD/MMC/SDIO Host Controller
    - SD v3.01, SDIO v3.0 and MMC v4.51
    - 1/4/8-bit bus width
  - 10/100 Ethernet MAC with MII/RMII interface
    - IEEE1588-2008 precision time stamping
    - Energy Efficient Ethernet (802.3az)
  - Up to 2× CAN Bus Controller
    - Version 2.0A and 2.0B up to 1 Mbps
  - 6× Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
    - Triple buffered full/half-duplex operation with flow control
    - Ultra high speed (36 MHz) operation on one instance
  - 2× Universal Asynchronous Receiver/ Transmitter
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 3× I^2C Interface with SMBus support
    - Address recognition in EM3 Stop Mode
- **Up to 144 General Purpose I/O Pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 5 V tolerance on select pins
  - Asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **Up to 24 Channel DMA Controller**
- **Up to 24 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **External Bus Interface for up to 4x256 MB of external memory mapped space**
  - TFT Controller with Direct Drive
  - Per-pixel alpha-blending engine
- **Hardware Cryptography**
  - AES 128/256-bit keys
  - ECC B/K163, B/K233, P192, P224, P256
  - SHA-1 and SHA-2 (SHA-224 and SHA-256)
  - True Random Number Generator (TRNG)
- **Hardware CRC engine**
  - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
  - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8×36 segments**
  - Voltage boost, contrast and autonomous animation
  - Patented low-energy LCD driver
- **Backup Power Domain**
  - RTCC and retention registers in a separate power domain, available down to energy mode EM4H
  - Operation from backup battery when main power absent/ insufficient
- **Ultra Low-Power Precision Analog Peripherals**
  - 2× 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
    - On-chip temperature sensor
  - 2× 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
  - Digital to Analog Current Converter (IDAC)
  - Up to 4× Analog Comparator (ACMP)
  - Up to 4× Operational Amplifier (OPAMP)
  - Robust current-based capacitive sensing with up to 64 inputs and wake-on-touch (CSEN)
  - Up to 108 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
  - Supply Voltage Monitor

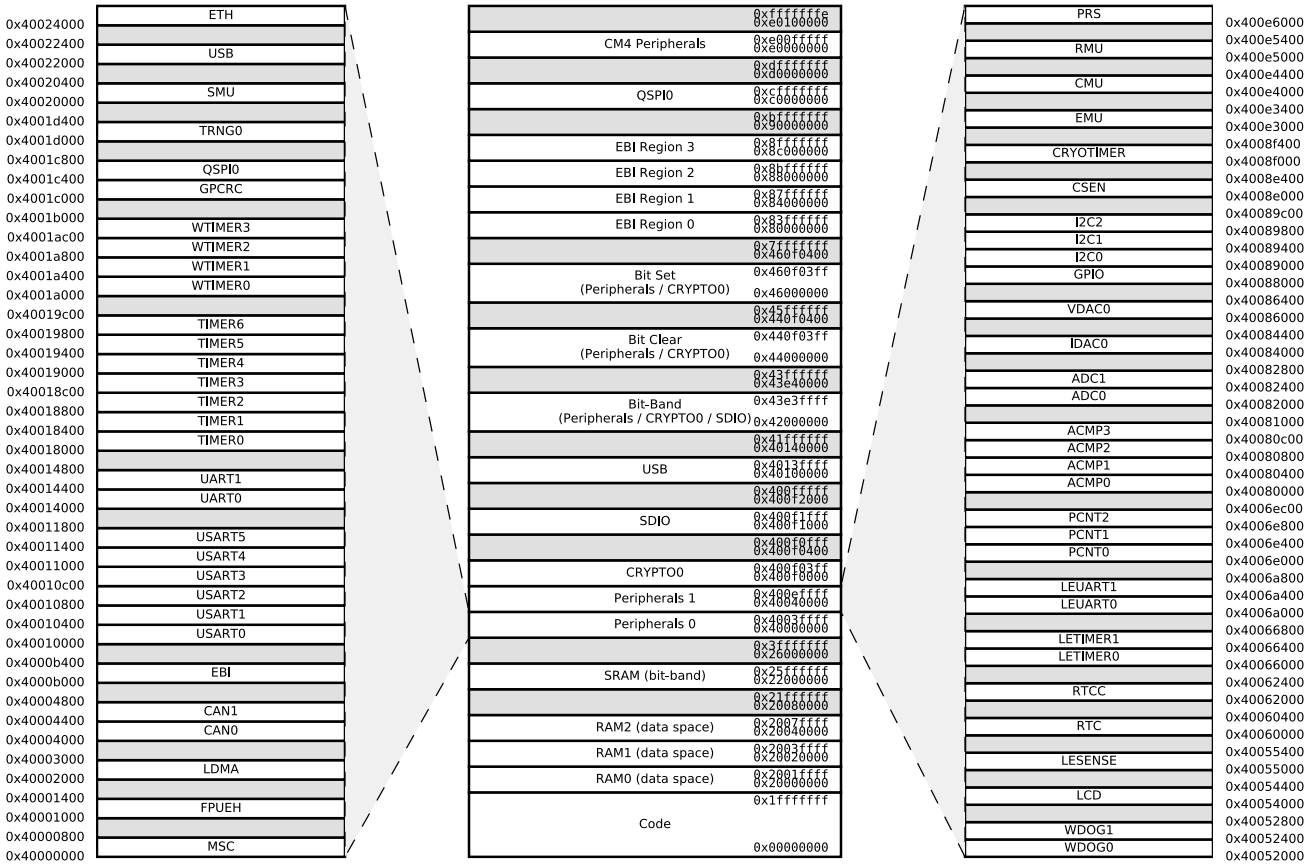

Figure 3.3. EFM32GG11 Memory Map — Peripherals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency limits	f_{HFRCO_BAND}	FREQRANGE = 0, FINETUNINGEN = 0	1	—	10	MHz
		FREQRANGE = 3, FINETUNINGEN = 0	2	—	17	MHz
		FREQRANGE = 6, FINETUNINGEN = 0	4	—	30	MHz
		FREQRANGE = 7, FINETUNINGEN = 0	5	—	34	MHz
		FREQRANGE = 8, FINETUNINGEN = 0	7	—	42	MHz
		FREQRANGE = 10, FINETUNINGEN = 0	12	—	58	MHz
		FREQRANGE = 11, FINETUNINGEN = 0	15	—	68	MHz
		FREQRANGE = 12, FINETUNINGEN = 0	18	—	83	MHz
		FREQRANGE = 13, FINETUNINGEN = 0	24	—	100	MHz
		FREQRANGE = 14, FINETUNINGEN = 0	28	—	119	MHz
		FREQRANGE = 15, FINETUNINGEN = 0	33	—	138	MHz
		FREQRANGE = 16, FINETUNINGEN = 0	43	—	163	MHz

Note:

1. Maximum DPLL lock time ~= 6 x (M+1) x t_{REF}, where t_{REF} is the reference clock period.

4.1.12 General-Purpose I/O (GPIO)

Table 4.20. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	IOVDD*0.3	V
Input high voltage	V_{IH}	GPIO pins	IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C	—	—	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T > 85 °C	—	—	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	TBD	µA
I/O pin pull-up/pull-down resistor	R_{PUD}		TBD	40	TBD	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		15	25	35	ns

4.1.16 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.24. Digital to Analog Converter (VDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage	V_{DACOUT}	Single-Ended	0	—	V_{VREF}	V
		Differential[2]	$-V_{VREF}$	—	V_{VREF}	V
Current consumption including references (2 channels)[1]	I_{DAC}	500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4	—	402	—	µA
		44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4	—	88	—	µA
		200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, BGRREQTIME = 1, EM2REFENTIME = 9, REFSEL = 4, SETTLETIME = 0x0A, WARMUPTIME = 0x02	—	2	—	µA
Current from HFPERCLK[4]	I_{DAC_CLK}		—	5.25	—	µA/MHz
Sample rate	SR_{DAC}		—	—	500	ksps
DAC clock frequency	f_{DAC}		—	—	1	MHz
Conversion time	$t_{DACCONV}$	f_{DAC} = 1MHz	2	—	—	µs
Settling time	$t_{DACSETTLE}$	50% fs step settling to 5 LSB	—	2.5	—	µs
Startup time	$t_{DACSTARTUP}$	Enable to 90% fs output, settling to 10 LSB	—	—	12	µs
Output impedance	R_{OUT}	DRIVESTRENGTH = 2, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -8 mA < I_{OUT} < 8 mA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -400 µA < I_{OUT} < 400 µA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 2, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -2 mA < I_{OUT} < 2 mA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -100 µA < I_{OUT} < 100 µA, Full supply range	—	2	—	Ω
Power supply rejection ratio[6]	PSRR	Vout = 50% fs. DC	—	65.5	—	dB

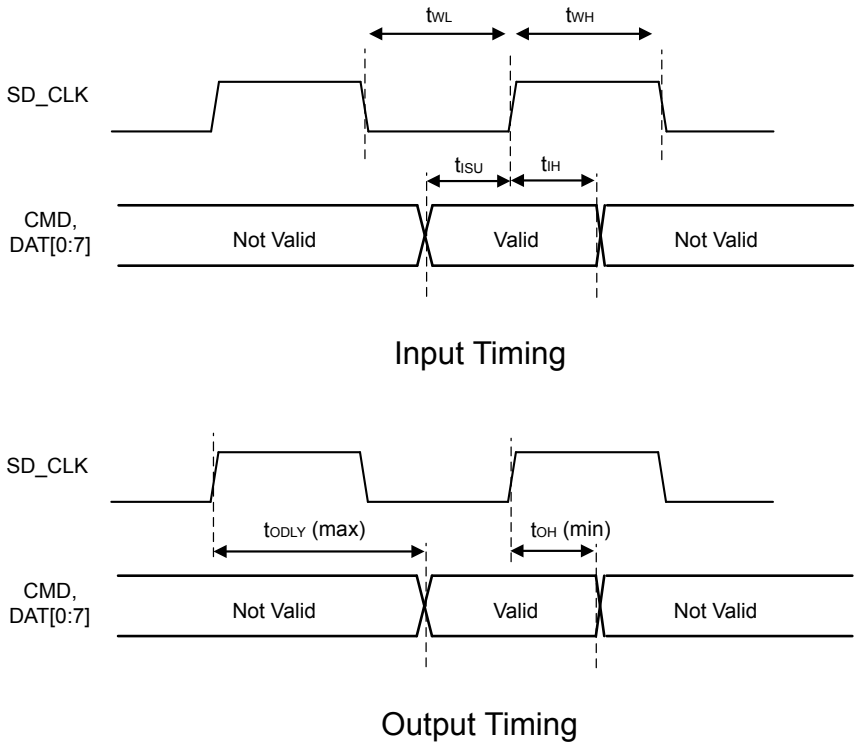

Figure 4.17. SDIO MMC SDR Mode Timing

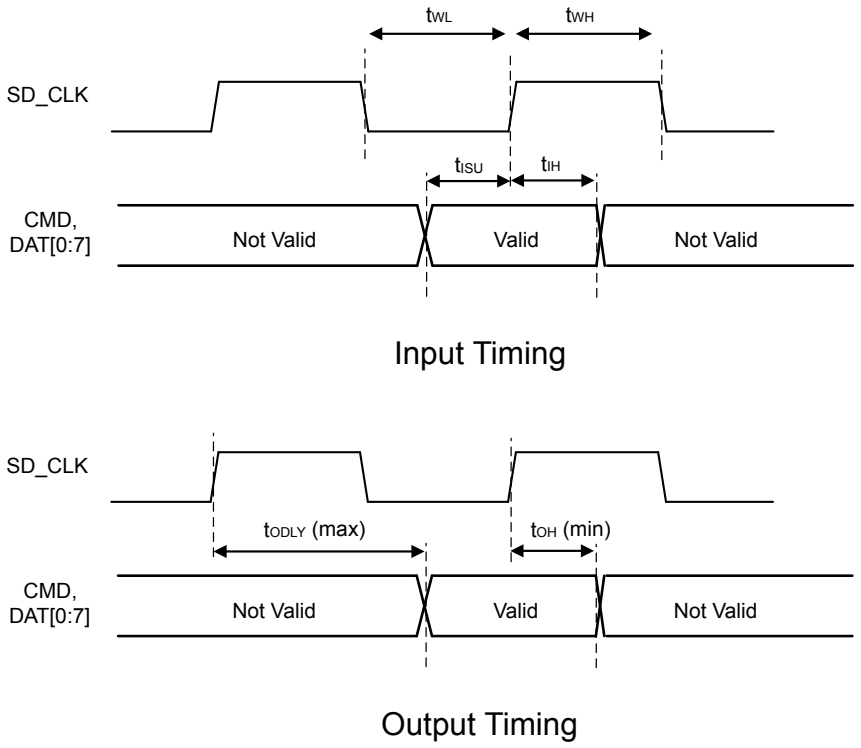

Figure 4.18. SDIO MMC SDR Mode Timing

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	M2	GPIO	PB3	M3	GPIO
PC6	M14	GPIO	VREGVSS	M15 N16	Voltage regulator VSS
VREGSW	M16	DCDC regulator switching node	PB4	N1	GPIO
PB5	N2	GPIO	PB6	N3	GPIO
PD5	N14	GPIO	PD4	N15	GPIO
PC0	P1	GPIO (5V)	PC1	P2	GPIO (5V)
PC2	P3	GPIO (5V)	PA8	P4	GPIO
PA11	P5	GPIO	PA13	P6	GPIO (5V)
PB9	P7	GPIO (5V)	PB12	P8	GPIO
PH2	P9	GPIO (5V)	PH5	P10	GPIO
PH8	P11	GPIO (5V)	PH11	P12	GPIO (5V)
PH13	P13	GPIO (5V)	PD0	P14	GPIO (5V)
PD3	P15	GPIO	PD8	P16	GPIO
PB7	R1	GPIO	PC3	R2	GPIO (5V)
PC5	R3	GPIO	PA9	R4	GPIO
BODEN	R5	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	RESETn	R6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB10	R7	GPIO (5V)	PH0	R8	GPIO (5V)
PH3	R9	GPIO (5V)	PH6	R10	GPIO
PH9	R11	GPIO (5V)	PH12	R12	GPIO (5V)
PH14	R13	GPIO (5V)	PH15	R14	GPIO (5V)
PD2	R15	GPIO (5V)	PD7	R16	GPIO
PB8	T1	GPIO	PC4	T2	GPIO
PA7	T3	GPIO	PA10	T4	GPIO
PA12	T5	GPIO (5V)	PA14	T6	GPIO
PB11	T7	GPIO	PH1	T8	GPIO (5V)
PH4	T9	GPIO	PH7	T10	GPIO (5V)
PH10	T11	GPIO (5V)	PB13	T12	GPIO
PB14	T13	GPIO	AVDD	T14	Analog power supply.
PD1	T15	GPIO	PD6	T16	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PG6	H1	GPIO (5V)	PG7	H2	GPIO (5V)
PG5	H3	GPIO (5V)	PE6	H12	GPIO
PE5	H13	GPIO	DVDD	H14	Digital power supply.
PG9	J1	GPIO (5V)	PG10	J2	GPIO (5V)
PG8	J3	GPIO (5V)	PE3	J12	GPIO
PE4	J13	GPIO	VREGVDD	J14	Voltage regulator VDD input
PG12	K1	GPIO	PG13	K2	GPIO
PG11	K3	GPIO (5V)	PE2	K12	GPIO
PE1	K13	GPIO (5V)	VREGSW	K14	DCDC regulator switching node
PG15	L1	GPIO (5V)	PB15	L2	GPIO (5V)
PG14	L3	GPIO	PC7	L12	GPIO
PE0	L13	GPIO (5V)	VREGVSS	L14	Voltage regulator VSS
PB0	M1	GPIO	PB1	M2	GPIO
PB4	M3	GPIO	PC0	M4	GPIO (5V)
PC3	M5	GPIO (5V)	PA9	M6	GPIO
BODEN	M7	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	PA12	M8	GPIO (5V)
RESETn	M9	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB10	M10	GPIO (5V)
PD1	M11	GPIO	PC6	M12	GPIO
PD5	M13	GPIO	PD8	M14	GPIO
PB7	N1	GPIO	PB2	N2	GPIO
PB5	N3	GPIO	PC2	N4	GPIO (5V)
PC5	N5	GPIO	PA8	N6	GPIO
PA11	N7	GPIO	PA14	N8	GPIO
PB11	N9	GPIO	PB12	N10	GPIO
PD0	N11	GPIO (5V)	PD2	N12	GPIO (5V)
PD4	N13	GPIO	PD7	N14	GPIO
PB8	P1	GPIO	PB3	P2	GPIO
PB6	P3	GPIO	PC1	P4	GPIO (5V)
PC4	P5	GPIO	PA7	P6	GPIO
PA10	P7	GPIO	PA13	P8	GPIO (5V)
PB9	P9	GPIO (5V)	PB13	P10	GPIO
PB14	P11	GPIO	AVDD	P12	Analog power supply.
PD3	P13	GPIO	PD6	P14	GPIO

5.9 EFM32GG11B5xx in QFP100 Device Pinout

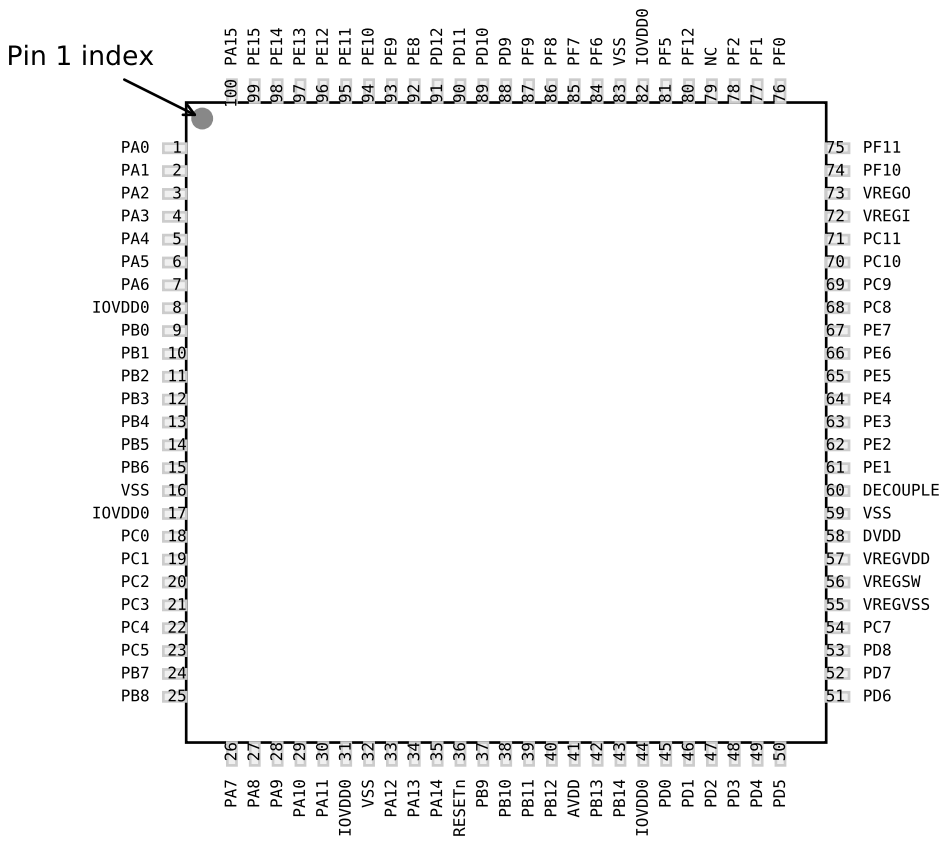

Figure 5.9. EFM32GG11B5xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.9. EFM32GG11B5xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 59 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB9	37	GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	45	GPIO (5V)	PD1	46	GPIO
PD2	47	GPIO (5V)	PD3	48	GPIO
PD4	49	GPIO	PD5	50	GPIO
PD6	51	GPIO	PD7	52	GPIO
PD8	53	GPIO	PC7	54	GPIO
VREGVSS	55	Voltage regulator VSS	VREGSW	56	DCDC regulator switching node
VREGVDD	57	Voltage regulator VDD input	DVDD	58	Digital power supply.
DECOUPLE	60	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE1	61	GPIO (5V)
PE2	62	GPIO	PE3	63	GPIO
PE4	64	GPIO	PE5	65	GPIO
PE6	66	GPIO	PE7	67	GPIO
PC8	68	GPIO (5V)	PC9	69	GPIO (5V)
PC10	70	GPIO (5V)	PC11	71	GPIO (5V)
VREGI	72	Input to 5 V regulator.	VREGO	73	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PF10	74	GPIO (5V)	PF11	75	GPIO (5V)
PF0	76	GPIO (5V)	PF1	77	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF1	77	GPIO (5V)	PF2	78	GPIO
VBUS	79	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	80	GPIO
PF5	81	GPIO	PF6	84	GPIO
PF7	85	GPIO	PF8	86	GPIO
PF9	87	GPIO	PD9	88	GPIO
PD10	89	GPIO	PD11	90	GPIO
PD12	91	GPIO	PE8	92	GPIO
PE9	93	GPIO	PE10	94	GPIO
PE11	95	GPIO	PE12	96	GPIO
PE13	97	GPIO	PE14	98	GPIO
PE15	99	GPIO	PA15	100	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A10	0: PE3 1: PD6 2: PC10 3: PB10		External Bus Interface (EBI) address output pin 10.
EBI_A11	0: PE4 1: PD7 2: PI6 3: PB11		External Bus Interface (EBI) address output pin 11.
EBI_A12	0: PE5 1: PD8 2: PI7 3: PB12		External Bus Interface (EBI) address output pin 12.
EBI_A13	0: PE6 1: PC7 2: PI8 3: PD0		External Bus Interface (EBI) address output pin 13.
EBI_A14	0: PE7 1: PE2 2: PI9 3: PD1		External Bus Interface (EBI) address output pin 14.
EBI_A15	0: PC8 1: PE3 2: PI10 3: PD2		External Bus Interface (EBI) address output pin 15.
EBI_A16	0: PB0 1: PE4 2: PH4 3: PD3		External Bus Interface (EBI) address output pin 16.
EBI_A17	0: PB1 1: PE5 2: PH5 3: PD4		External Bus Interface (EBI) address output pin 17.
EBI_A18	0: PB2 1: PE6 2: PH6 3: PD5		External Bus Interface (EBI) address output pin 18.
EBI_A19	0: PB3 1: PE7 2: PH7 3: PD6		External Bus Interface (EBI) address output pin 19.
EBI_A20	0: PB4 1: PC8 2: PH8 3: PD7		External Bus Interface (EBI) address output pin 20.
EBI_A21	0: PB5 1: PC9 2: PH9 3: PC7		External Bus Interface (EBI) address output pin 21.
EBI_A22	0: PB6 1: PC10 2: PH10 3: PE4		External Bus Interface (EBI) address output pin 22.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_TSUTMR-TOG	0: PB6 1: PB15 2: PC3 3: PF9		Ethernet IEEE1588 Timer Toggle.
ETM_TCLK	0: PD7 1: PF8 2: PC6 3: PA6	4: PE11 5: PG15	Embedded Trace Module ETM clock .
ETM_TD0	0: PD6 1: PF9 2: PC7 3: PA2	4: PE12 5: PG14	Embedded Trace Module ETM data 0.
ETM_TD1	0: PD3 1: PD13 2: PD3 3: PA3	4: PE13 5: PG13	Embedded Trace Module ETM data 1.
ETM_TD2	0: PD4 1: PB15 2: PD4 3: PA4	4: PE14 5: PG12	Embedded Trace Module ETM data 2.
ETM_TD3	0: PD5 1: PF3 2: PD5 3: PA5	4: PE15 5: PG11	Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.
OPA2_OUT	0: PD5		Operational Amplifier 2 output.
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.
OPA3_N	0: PC7		Operational Amplifier 3 external negative input.
OPA3_OUT	0: PD1		Operational Amplifier 3 output.
OPA3_P	0: PC6		Operational Amplifier 3 external positive input.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM2_CC1	0: PA9 1: PA13 2: PC9 3: PE12	4: PC0 5: PC3 6: PG9 7: PG6	Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	0: PA10 1: PA14 2: PC10 3: PE13	4: PC1 5: PC4 6: PG10 7: PG7	Timer 2 Capture Compare input / output channel 2.
TIM2_CDTI0	0: PB0 1: PD13 2: PE8 3: PG0		Timer 2 Complimentary Dead Time Insertion channel 0.
TIM2_CDTI1	0: PB1 1: PD14 2: PE14 3: PG1		Timer 2 Complimentary Dead Time Insertion channel 1.
TIM2_CDTI2	0: PB2 1: PD15 2: PE15 3: PG2		Timer 2 Complimentary Dead Time Insertion channel 2.
TIM3_CC0	0: PE14 1: PE0 2: PE3 3: PE5	4: PA0 5: PA3 6: PA6 7: PD15	Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	0: PE15 1: PE1 2: PE4 3: PE6	4: PA1 5: PA4 6: PD13 7: PB15	Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	0: PA15 1: PE2 2: PE5 3: PE7	4: PA2 5: PA5 6: PD14 7: PB0	Timer 3 Capture Compare input / output channel 2.
TIM4_CC0	0: PF3 1: PF13 2: PF5 3: PI8	4: PF6 5: PF9 6: PD11 7: PE9	Timer 4 Capture Compare input / output channel 0.
TIM4_CC1	0: PF4 1: PF14 2: PI6 3: PI9	4: PF7 5: PD9 6: PD12 7: PE10	Timer 4 Capture Compare input / output channel 1.
TIM4_CC2	0: PF12 1: PF15 2: PI7 3: PI10	4: PF8 5: PD10 6: PE8 7: PE11	Timer 4 Capture Compare input / output channel 2.
TIM4_CDTI0	0: PD0		Timer 4 Complimentary Dead Time Insertion channel 0.
TIM4_CDTI1	0: PD1		Timer 4 Complimentary Dead Time Insertion channel 1.

Table 5.26. ACMP3 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP3X																									PH15	PH14	PH13	PH12	PH11	PH10	PH9	PH8
APORT0Y	BUSACMP3Y																									PH15	PH14	PH13	PH12	PH11	PH10	PH9	PH8
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA1_N																																	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
OPA1_P																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
OPA2_N																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 6.2. BGA192 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.20	
C1		6.00	
C2		6.00	
E1		0.4	
E2		0.4	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10.2 TQFP100 PCB Land Pattern

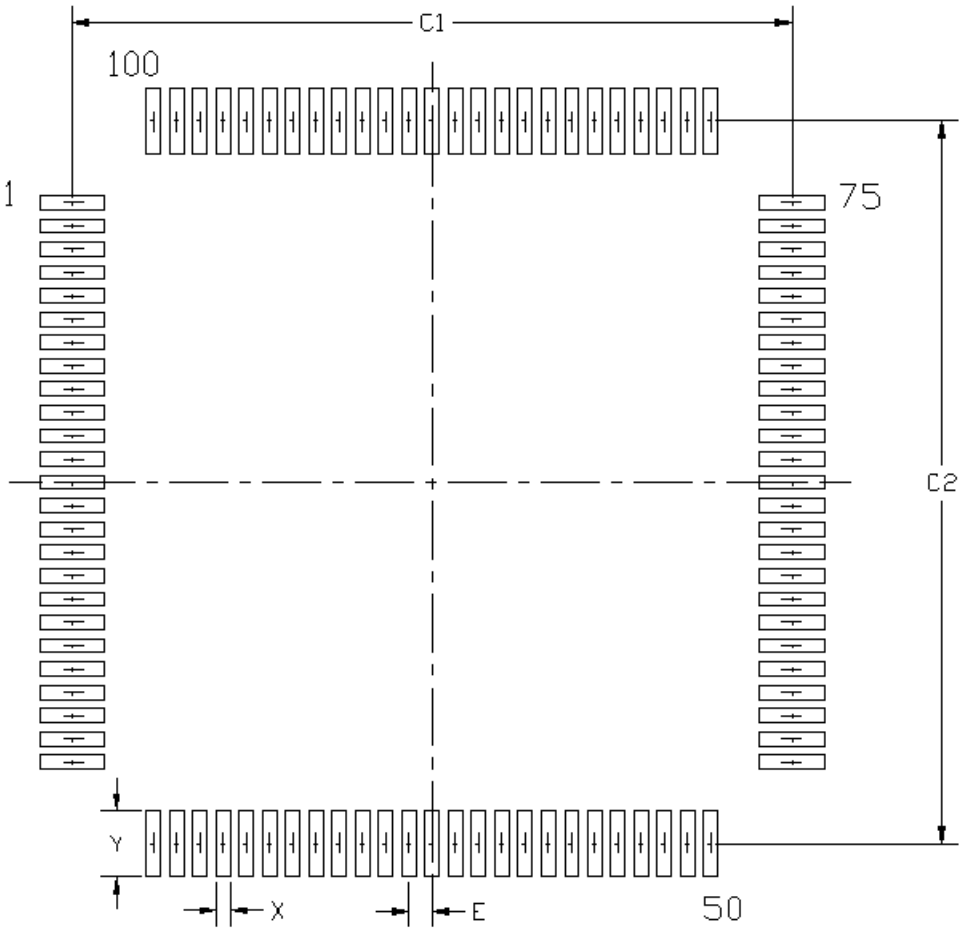

Figure 10.2. TQFP100 PCB Land Pattern Drawing