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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b510f2048iq64-br

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD $\leq$ AVDD
- IOVDD $\leq$ AVDD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4H mode, with voltage scaling enabled	I _{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.94	—	μA
		128 byte RAM retention, CRYO-TIMER running from ULFRCO	—	0.62	—	μA
		128 byte RAM retention, no RTCC	—	0.62	—	μA
Current consumption in EM4S mode	I _{EM4S}	No RAM retention, no RTCC	—	0.13	—	μA
Current consumption of peripheral power domain 1, with voltage scaling enabled, DCDC in LP mode ³	I _{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled ⁴	—	0.68	—	μA
Current consumption of peripheral power domain 2, with voltage scaling enabled, DCDC in LP mode ³	I _{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled ⁴	—	0.28	—	μA

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See [3.2.4 EM2 and EM3 Power Domains](#) for a list of the peripherals in each power domain.
5. CMU_LFRCCOCTRL_ENVREF = 1, CMU_LFRCCOCTRL_VREFUPDATE = 1

SPI Slave Timing

Table 4.35. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 3 2}	t_{SCLK}		6 * t_{HFERCLK}	—	—	ns
SCLK high time ^{1 3 2}	$t_{\text{SCLK_HI}}$		2.5 * t_{HFERCLK}	—	—	ns
SCLK low time ^{1 3 2}	$t_{\text{SCLK_LO}}$		2.5 * t_{HFERCLK}	—	—	ns
CS active to MISO ^{1 3}	$t_{\text{CS_ACT_MI}}$		24	—	69	ns
CS disable to MISO ^{1 3}	$t_{\text{CS_DIS_MI}}$		19	—	175	ns
MOSI setup time ^{1 3}	$t_{\text{SU_MO}}$		7	—	—	ns
MOSI hold time ^{1 3 2}	$t_{\text{H_MO}}$		6	—	—	ns
SCLK to MISO ^{1 3 2}	$t_{\text{SCLK_MI}}$		16 + 1.5 * t_{HFERCLK}	—	43 + 2.5 * t_{HFERCLK}	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. t_{HFERCLK} is one period of the selected HFERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

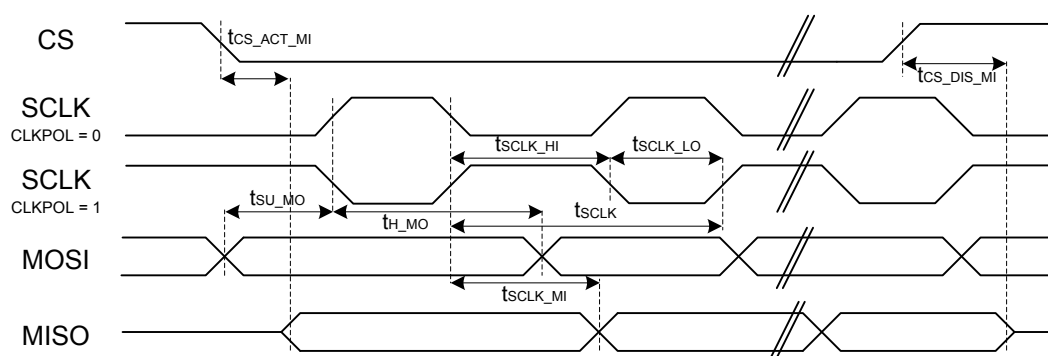


Figure 4.2. SPI Slave Timing Diagram

EBI Read Enable Output Timing

Timing applies to both EBI_REn and EBI_NANDREn for all addressing modes and both polarities. Output timing for EBI_AD applies only to multiplexed addressing modes D8A24ALE and D16A16ALE. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.38. EBI Read Enable Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_REn / EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CS _n , EBI_BLn invalid	t _{OH_REn}	IOVDD ≥ 1.62 V	-23 + (RDHOLD * t _{HFCOR-ECLK})	—	—	ns
		IOVDD ≥ 3.0 V	-13 + (RDHOLD * t _{HFCOR-ECLK})	—	—	ns
Output setup time, from EBI_AD, EBI_A, EBI_CS _n , EBI_BLn valid to leading EBI_REn / EBI_NANDREn edge ¹	t _{OSU_REn}	IOVDD ≥ 1.62 V	-12 + (RDSETUP * t _{HFCOR-ECLK})	—	—	ns
		IOVDD ≥ 3.0 V	-11 + (RDSETUP * t _{HFCOR-ECLK})	—	—	ns
EBI_REn pulse width ^{1 2}	t _{WIDTH_REn}	IOVDD ≥ 1.62 V	-6 + (MAX(1, RDSTRB) * t _{HFCOR-ECLK})	—	—	ns
		IOVDD ≥ 3.0 V	-4 + (MAX(1, RDSTRB) * t _{HFCOR-ECLK})	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of t_{WIDTH_REn} and increases the length of t_{OSU_REn} by 1/2 * t_{HFCLKNODIV}.
2. When page mode is used, RDSTRB is replaced by RDPA for page hits.

RMII Receive Timing

Timing is specified with $3.0\text{ V} \leq \text{IOVDD} \leq 3.8\text{ V}$, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.45. Ethernet RMII Receive Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REF_CLK frequency	$F_{\text{REF_CLK}}$	Output slew rate set to 7	—	50	—	MHz
REF_CLK duty cycle	$DC_{\text{REF_CLK}}$		35	—	65	%
Setup time, RXD[1:0], CRS_DV, RX_ER valid to REF_CLK	t_{SU}		4	—	—	ns
Hold time, REF_CLK to RXD[1:0], CRS_DV, RX_ER change	t_{HD}		2	—	—	ns

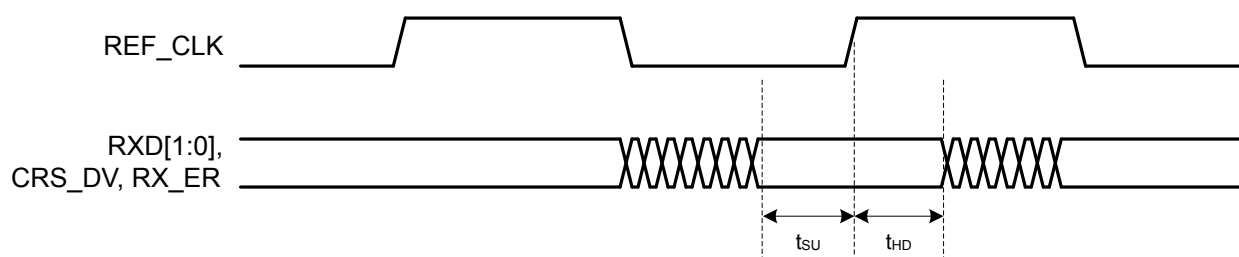


Figure 4.12. Ethernet RMII Receive Timing

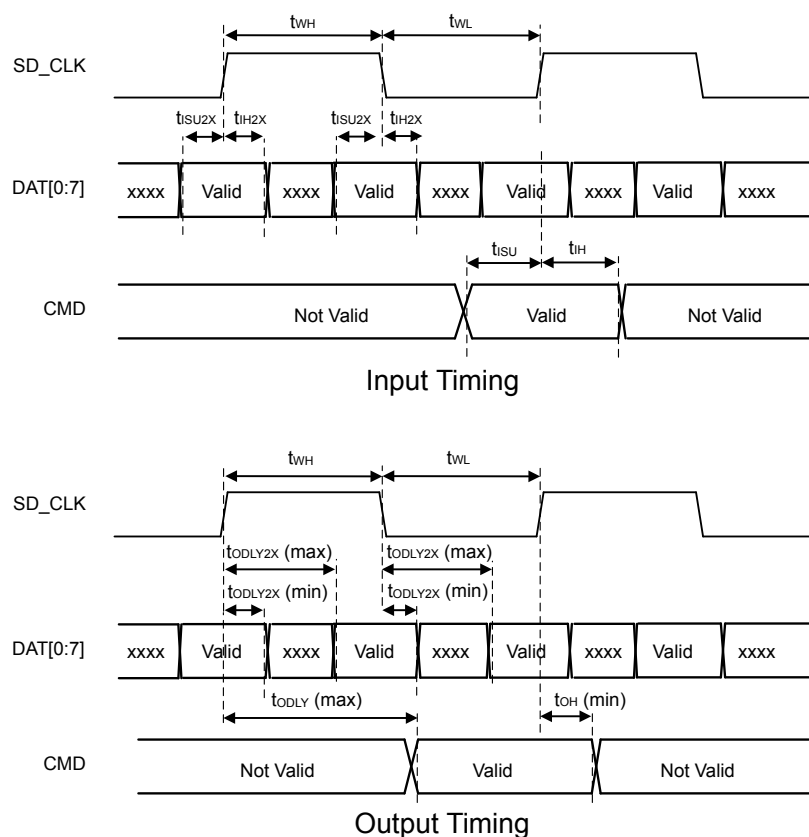


Figure 4.20. SDIO MMC DDR Mode Timing

4.1.28 Quad SPI (QSPI)

4.1.28.1 QSPI SDR Mode

QSPI SDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 23, RX DLL = 48, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.54. QSPI SDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full SCLK period	T		$(1/F_{SCLK}) * 0.95$	—	—	ns
Output valid	t_{OV}		—	—	$T/2 - 2.4$	ns
Output hold	t_{OH}		$T/2 - 32.9$	—	—	ns
Input setup	t_{SU}		$36.2 - T/2$	—	—	ns
Input hold	t_{H}		$T/2 - 3.3$	—	—	ns

4.2.1 Supply Current

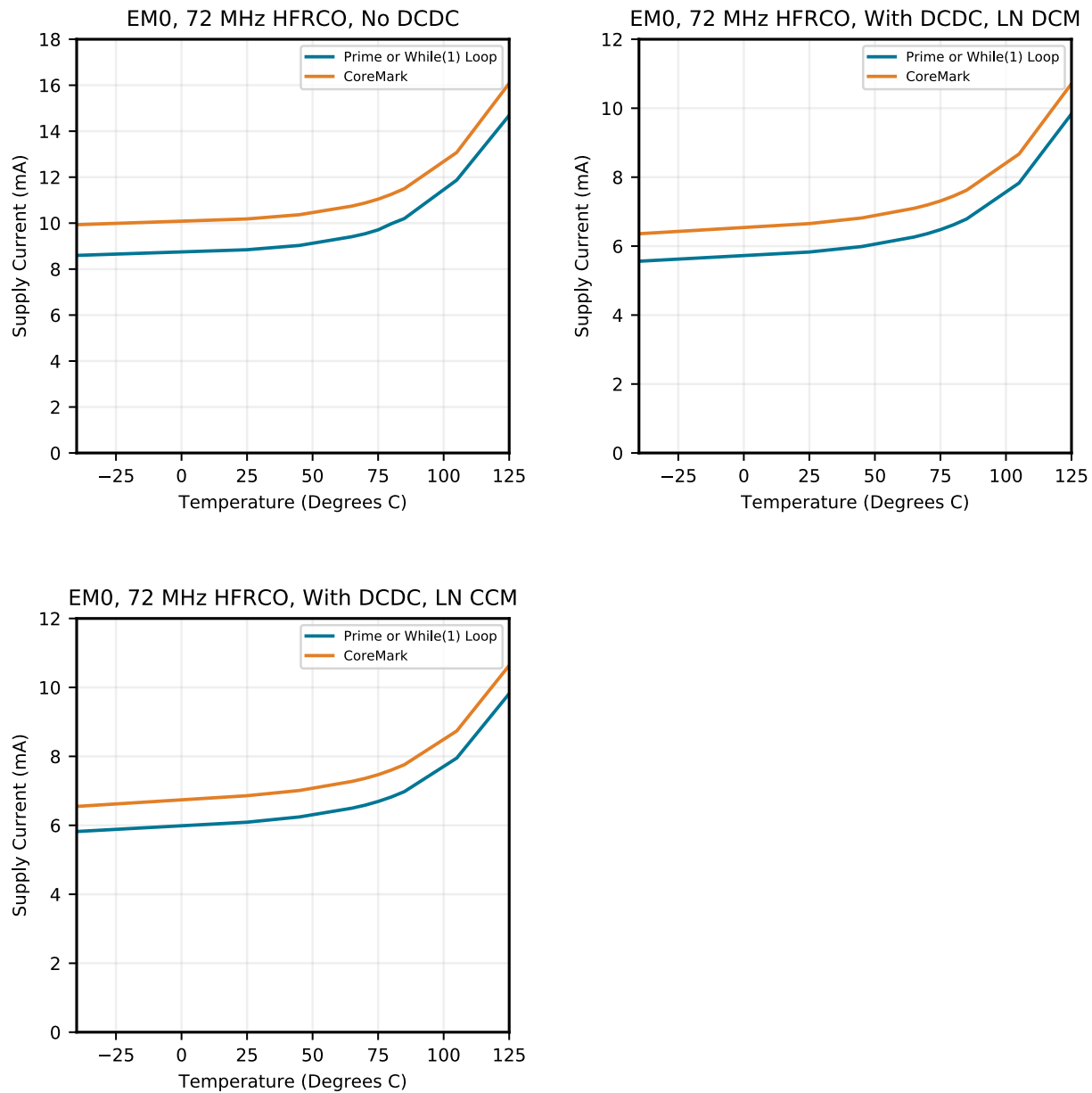


Figure 4.23. EM0 Full Speed Active Mode Typical Supply Current vs. Temperature

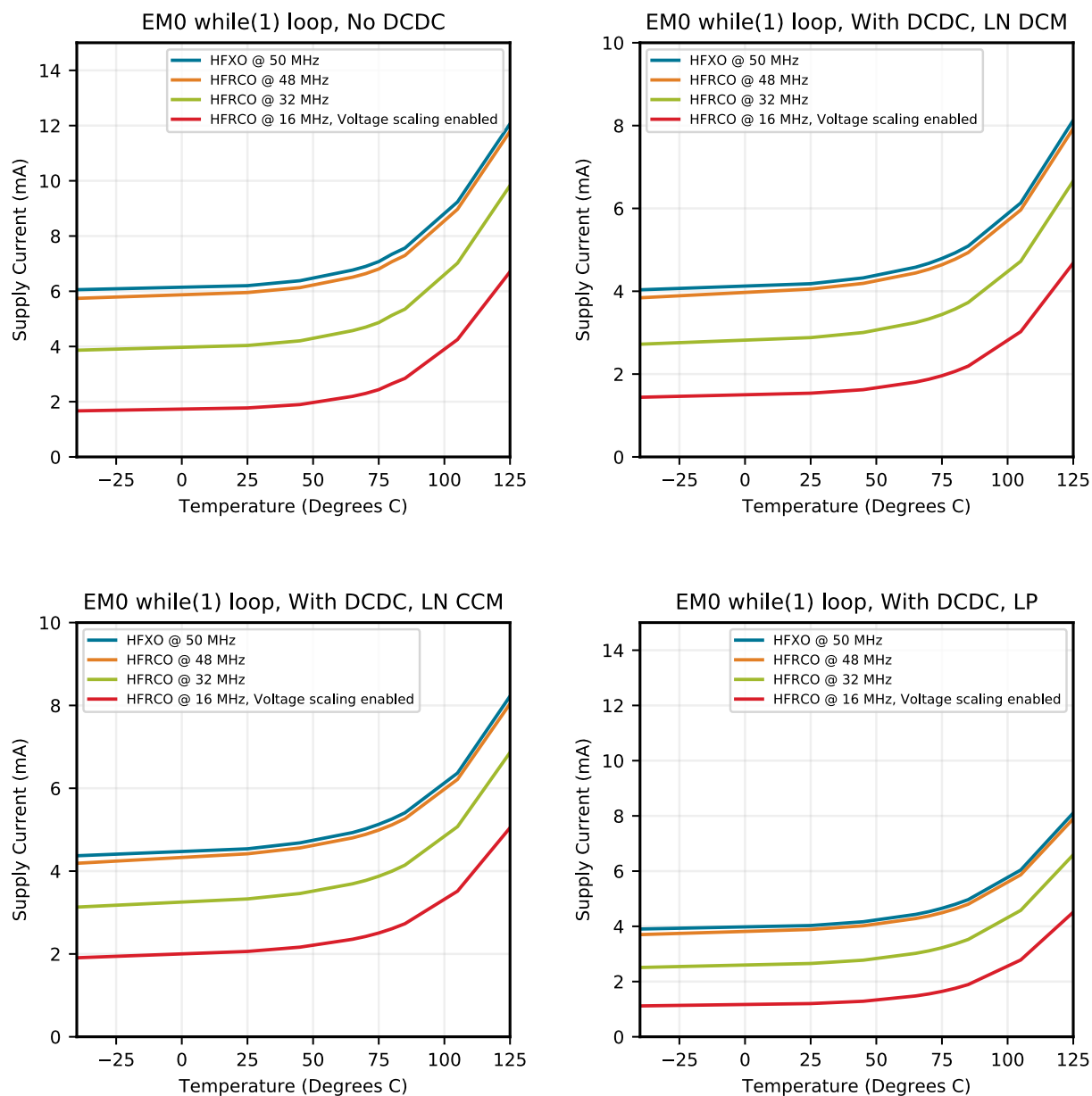


Figure 4.24. EM0 Active Mode Typical Supply Current vs. Temperature

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 μ H, CDCDC = 4.7 μ F, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

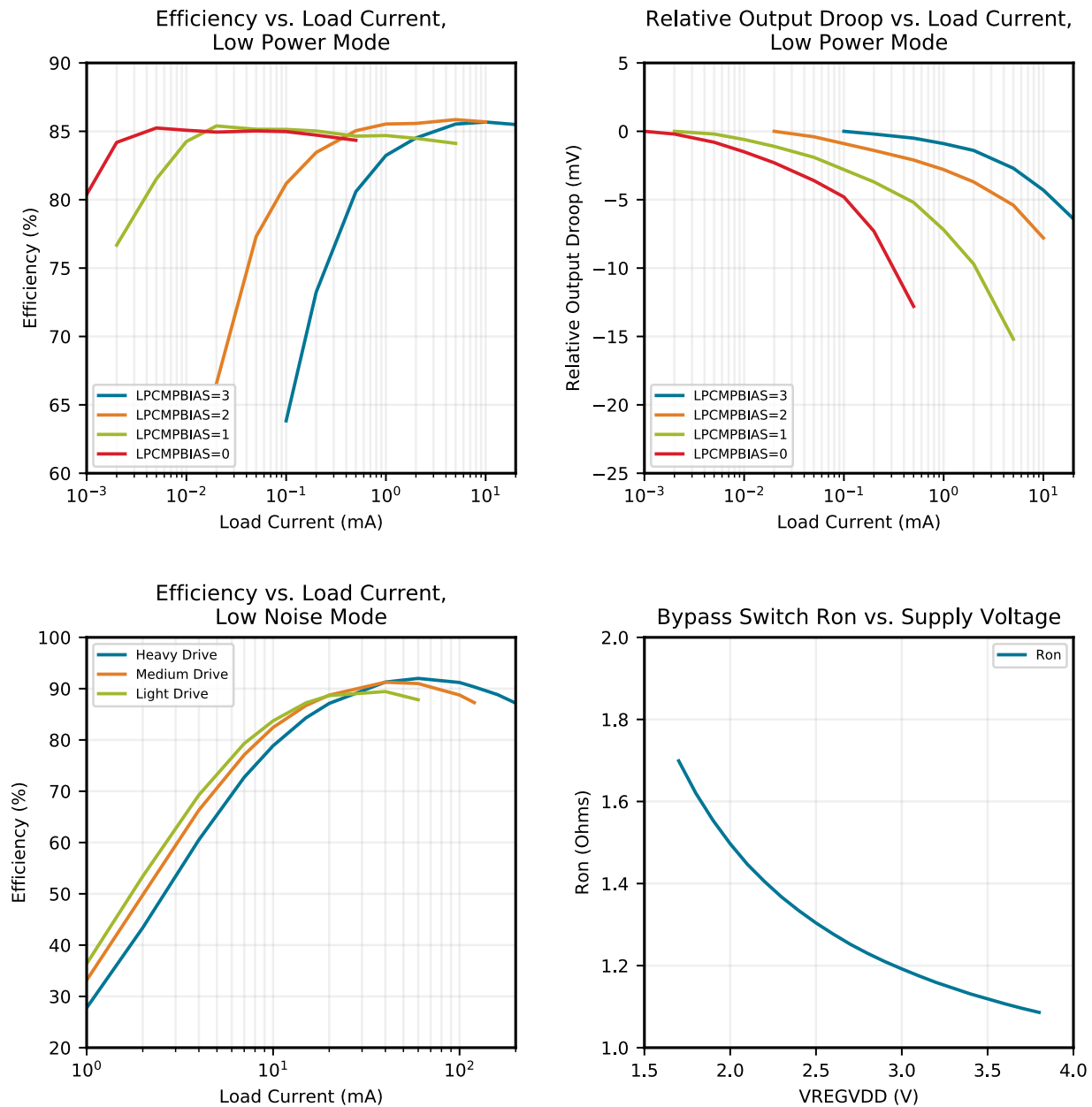


Figure 4.29. DC-DC Converter Typical Performance Characteristics

5.2 EFM32GG11B8xx in BGA152 Device Pinout

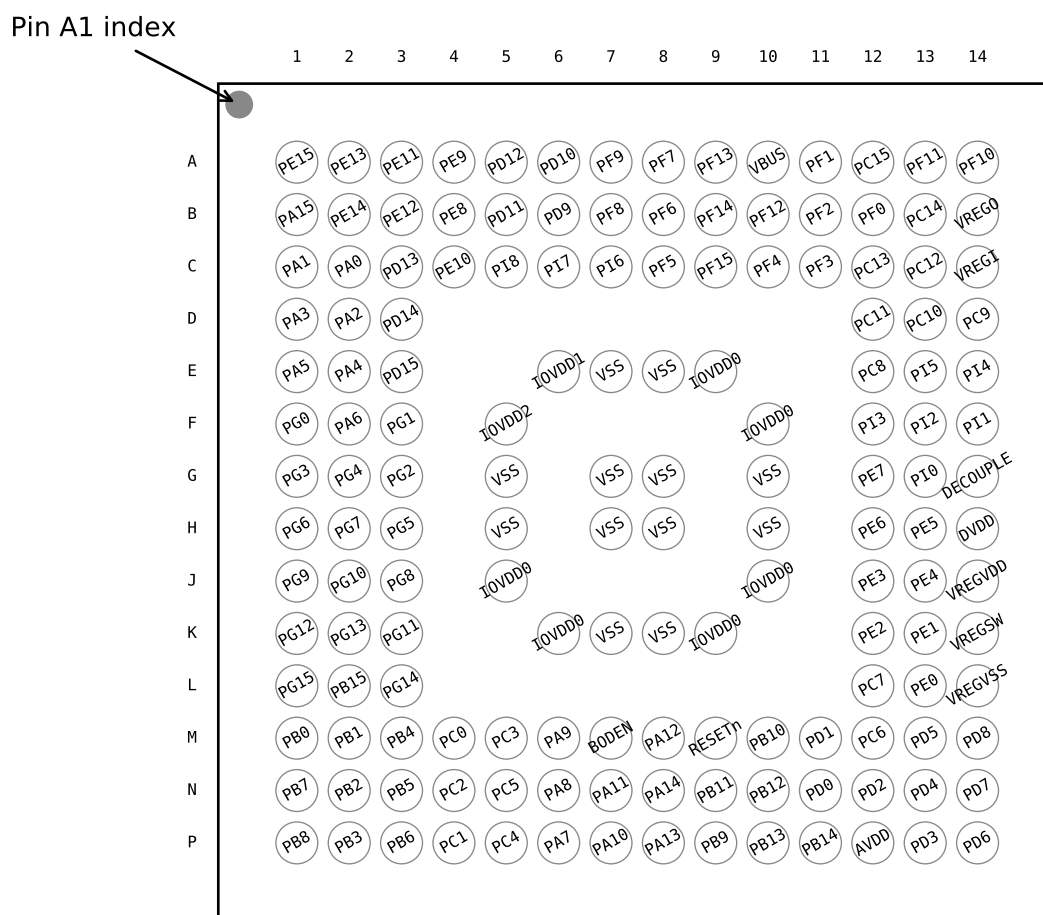


Figure 5.2. EFM32GG11B8xx in BGA152 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.2. EFM32GG11B8xx in BGA152 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE13	A2	GPIO
PE11	A3	GPIO	PE9	A4	GPIO
PD12	A5	GPIO	PD10	A6	GPIO
PF9	A7	GPIO	PF7	A8	GPIO
PF13	A9	GPIO (5V)	VBUS	A10	USB VBUS signal and auxiliary input to 5 V regulator.
PF1	A11	GPIO (5V)	PC15	A12	GPIO (5V)
PF11	A13	GPIO (5V)	PF10	A14	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	K2	GPIO (5V)	PE0	K12	GPIO (5V)
VREGSW	K13	DCDC regulator switching node	PC2	L1	GPIO (5V)
PC3	L2	GPIO (5V)	PA7	L3	GPIO
PB9	L13	GPIO (5V)	PB10	L14	GPIO (5V)
PD1	L17	GPIO	PC6	L18	GPIO
PC7	L19	GPIO	VREGVSS	L20	Voltage regulator VSS
PB7	M1	GPIO	PC4	M2	GPIO
PA8	M3	GPIO	PA10	M4	GPIO
PA13	M5	GPIO (5V)	PA14	M6	GPIO
RESETn	M7	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB12	M8	GPIO
PD0	M9	GPIO (5V)	PD2	M10	GPIO (5V)
PD3	M11	GPIO	PD4	M12	GPIO
PD8	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	BODEN	N7	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.
PB13	N8	GPIO	PB14	N9	GPIO
AVDD	N10	Analog power supply.	PD5	N11	GPIO
PD6	N12	GPIO	PD7	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.5 EFM32GG11B4xx in BGA120 Device Pinout

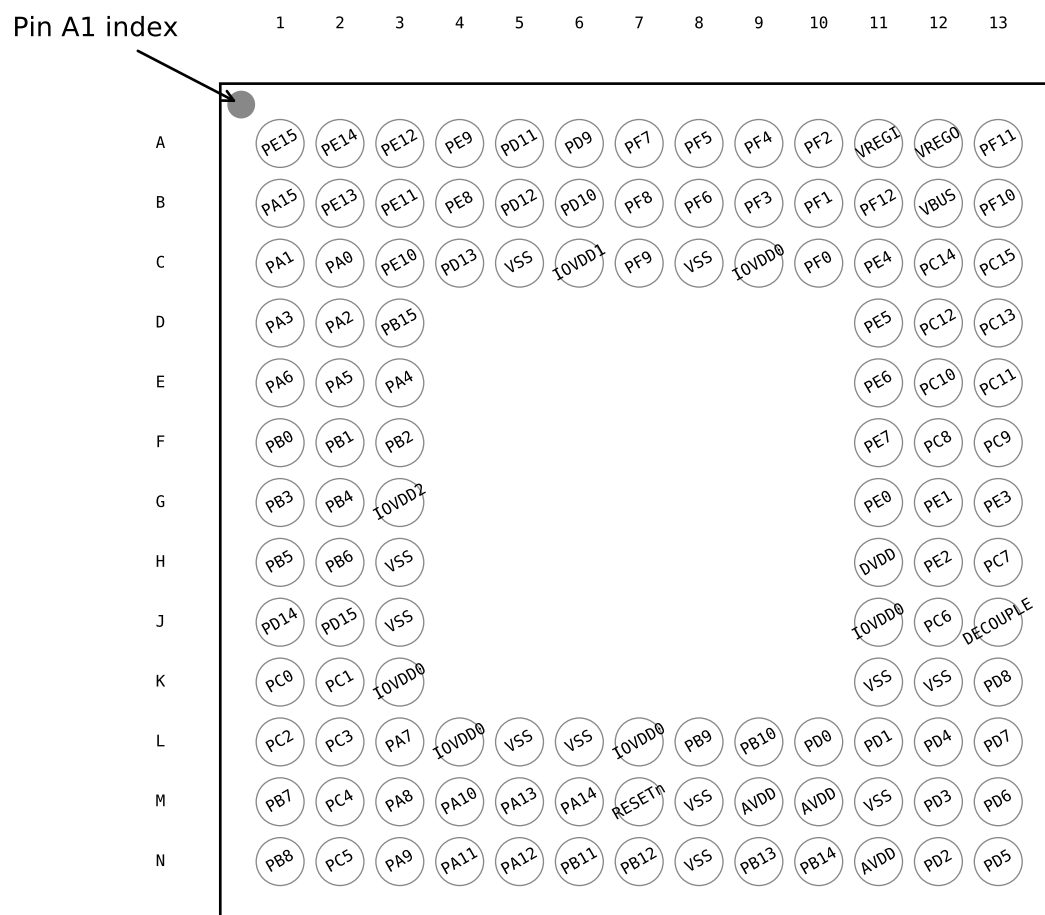


Figure 5.5. EFM32GG11B4xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.5. EFM32GG11B4xx in BGA120 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF4	A9	GPIO	PF2	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF3	B9	GPIO
PF1	B10	GPIO (5V)	PF12	B11	GPIO
VBUS	B12	USB VBUS signal and auxiliary input to 5 V regulator.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 K12 L12 L13 M8 M11 N8	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L14	Digital IO power supply 0.
PF0	C10	GPIO (5V)	PE4	C11	GPIO
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PE5	D11	GPIO
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PE6	E11	GPIO
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE7	F11	GPIO
PC8	F12	GPIO (5V)	PC9	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE0	G11	GPIO (5V)
PE1	G12	GPIO (5V)	PE3	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
PC7	H13	GPIO	PD14	J1	GPIO (5V)

5.14 EFM32GG11B4xx in QFP64 Device Pinout

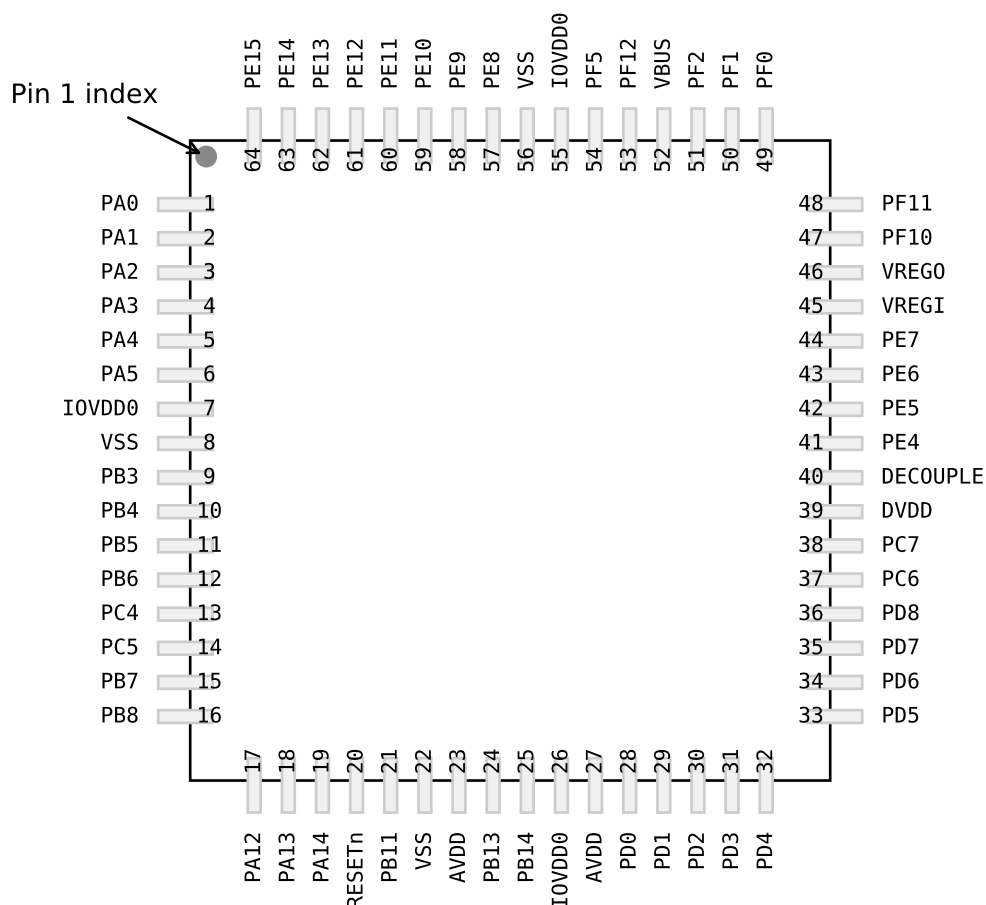


Figure 5.14. EFM32GG11B4xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.14. EFM32GG11B4xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

5.20 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to [5.21 Alternate Functionality Overview](#) for a list of GPIO locations available for each function.

Table 5.20. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PA15	BUSAY BUSBX LCD_SEG12	EBI_AD08 #0	TIM3_CC2 #0	ETH_MIIRXCLK #0 ETH_MDIO #3 US2_CLK #3	PRS_CH15 #0
PE15	BUSCY BUSDX LCD_SEG11	EBI_AD07 #0	TIM2_CDTI2 #2 TIM3_CC1 #0	ETH_RMIITXD0 #0 ETH_MIIRXD3 #0 SDIO_CMD #1 US0_RTS #0 QSPI0_DQS #1 LEU0_RX #2	PRS_CH14 #2 ETM_TD3 #4
PE14	BUSDY BUSCX LCD_SEG10	EBI_AD06 #0	TIM2_CDTI1 #2 TIM3_CC0 #0	ETH_RMIITXD1 #0 ETH_MIIRXD2 #0 SDIO_CLK #1 US0_CTS #0 QSPI0_SCLK #1 LEU0_TX #2	PRS_CH13 #2 ETM_TD2 #4
PE13	BUSCY BUSDX LCD_SEG9	EBI_AD05 #0	TIM1_CC3 #1 TIM2_CC2 #3 LE- TIM0_OUT1 #4	SDIO_CLK #0 ETH_MIIRXD1 #0 US0_TX #3 US0_CS #0 U1_RX #4 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 ETM_TD1 #4 GPIO_EM4WU5
PE12	BUSDY BUSCX LCD_SEG8	EBI_AD04 #0	TIM1_CC2 #1 TIM2_CC1 #3 WTIM0_CDTI2 #0 LETIM0_OUT0 #4	SDIO_CMD #0 ETH_MIIRXD0 #0 US0_RX #3 US0_CLK #0 U1_TX #4 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_ALTEX6 PRS_CH1 #3 ETM_TD0 #4
PE11	BUSCY BUSDX LCD_SEG7	EBI_AD03 #0 EBI_CS3 #4	TIM1_CC1 #1 TIM4_CC2 #7 WTIM0_CDTI1 #0	SDIO_DAT0 #0 QSPI0_DQ7 #0 ETH_MIIRXDV #0 US0_RX #0	LES_ALTEX5 PRS_CH3 #2 ETM_TCLK #4
PE10	BUSDY BUSCX LCD_SEG6	EBI_AD02 #0 EBI_CS2 #4	TIM1_CC0 #1 TIM4_CC1 #7 WTIM0_CDTI0 #0	SDIO_DAT1 #0 QSPI0_DQ6 #0 ETH_MIIRXER #0 US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE9	BUSCY BUSDX LCD_SEG5	EBI_AD01 #0 EBI_CS1 #4	TIM4_CC0 #7 PCNT2_S1IN #1	SDIO_DAT2 #0 QSPI0_DQ5 #0 US5_RX #0	PRS_CH8 #2
PE8	BUSDY BUSCX LCD_SEG4	EBI_AD00 #0 EBI_CS0 #4	TIM2_CDTI0 #2 TIM4_CC2 #6 PCNT2_S0IN #1	SDIO_DAT3 #0 QSPI0_DQ4 #0 US5_TX #0 I2C2_SDA #0	PRS_CH3 #1
PI9		EBI_A14 #2	TIM1_CC3 #7 TIM4_CC1 #3	US4_CS #3	
PI6		EBI_A11 #2	TIM1_CC0 #7 TIM4_CC1 #2 WTIM3_CC0 #5	US4_TX #3	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PB0	BUSBY BUSAX LCD_SEG32	EBI_AD00 #1 EBI_CS0 #3 EBI_A16 #0	TIM2_CDTI0 #0 TIM1_CC0 #2 TIM3_CC2 #7 WTIM0_CC0 #5 PCNT0_S0IN #5 PCNT1_S1IN #2	LEU1_TX #3	PRS_CH4 #1 ACMP0_O #5
PE0	BUSDY BUSCX	EBI_A00 #2 EBI_A07 #0	TIM3_CC0 #1 WTIM1_CC1 #3 PCNT0_S0IN #1	CAN0_RX #6 U0_TX #1 I2C1_SDA #2	PRS_CH22 #1 ACMP2_O #1
PC7	BUSACMP0Y BU- SACMP0X OPA3_N	EBI_A06 #0 EBI_A13 #1 EBI_A21 #3	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 LEU1_RX #0 I2C0_SCL #2	LES_CH7 PRS_CH15 #1 ETM_TD0 #2
PB1	BUSAY BUSBX LCD_SEG33	EBI_AD01 #1 EBI_CS1 #3 EBI_A17 #0	TIM2_CDTI1 #0 TIM1_CC1 #2 WTIM0_CC1 #5 LE- TIM1_OUT1 #5 PCNT0_S1IN #5	ETH_MIICRS #0 US5_RX #2 LEU1_RX #3	PRS_CH5 #1
PB2	BUSBY BUSAX LCD_SEG34	EBI_AD02 #1 EBI_CS2 #3 EBI_A18 #0	TIM2_CDTI2 #0 TIM1_CC2 #2 WTIM0_CC2 #5 LE- TIM1_OUT0 #5	ETH_MIICOL #0 US1_CS #6	PRS_CH18 #0 ACMP0_O #6
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	EBI_AD03 #1 EBI_CS3 #3 EBI_A19 #0	TIM1_CC3 #2 WTIM0_CC0 #6 PCNT1_S0IN #1	ETH_MIICRS #2 ETH_MDIO #0 SDIO_DAT6 #1 US2_TX #1 US3_TX #2 QSPI0_DQ4 #1	PRS_CH19 #0 ACMP0_O #7
PC6	BUSACMP0Y BU- SACMP0X OPA3_P	EBI_A05 #0	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 LEU1_TX #0 I2C0_SDA #2	LES_CH6 PRS_CH14 #1 ETM_TCLK #2
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	EBI_AD04 #1 EBI_ARDY #3 EBI_A20 #0	WTIM0_CC1 #6 PCNT1_S1IN #1	ETH_MIICOL #2 ETH_MDC #0 SDIO_DAT7 #1 US2_RX #1 QSPI0_DQ5 #1 LEU1_TX #4	PRS_CH20 #0
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	EBI_AD05 #1 EBI_ALE #3 EBI_A21 #0	WTIM0_CC2 #6 LE- TIM1_OUT0 #4 PCNT0_S0IN #6	ETH_TSUEXTCLK #0 US0_RTS #4 US2_CLK #1 QSPI0_DQ6 #1 LEU1_RX #4	PRS_CH21 #0
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	EBI_AD06 #1 EBI_WEn #3 EBI_A22 #0	TIM0_CC0 #3 TIM2_CC0 #4 WTIM3_CC0 #6 LE- TIM1_OUT1 #4 PCNT0_S1IN #6	ETH_TSUTMRTOG #0 US0_CTS #4 US2_CS #1 QSPI0_DQ7 #1	PRS_CH12 #1
PD5	BUSADC0Y BU- SADC0X OPA2_OUT	EBI_A09 #1 EBI_A18 #3	TIM6_CC1 #7 WTIM0_CDTI1 #4 WTIM1_CC3 #1 WTIM2_CC2 #5	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3	PRS_CH11 #2 ETM_TD3 #0 ETM_TD3 #2

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
DBG_SWO	0: PF2 1: PC15 2: PD1 3: PD2		Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF5		Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2		Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
EBI_A00	0: PA12 1: PB9 2: PE0 3: PC5		External Bus Interface (EBI) address output pin 00.
EBI_A01	0: PA13 1: PB10 2: PE1 3: PA7		External Bus Interface (EBI) address output pin 01.
EBI_A02	0: PA14 1: PB11 2: PI0 3: PA8		External Bus Interface (EBI) address output pin 02.
EBI_A03	0: PB9 1: PB12 2: PI1 3: PA9		External Bus Interface (EBI) address output pin 03.
EBI_A04	0: PB10 1: PD0 2: PI2 3: PA10		External Bus Interface (EBI) address output pin 04.
EBI_A05	0: PC6 1: PD1 2: PI3 3: PA11		External Bus Interface (EBI) address output pin 05.
EBI_A06	0: PC7 1: PD2 2: PI4 3: PA12		External Bus Interface (EBI) address output pin 06.
EBI_A07	0: PE0 1: PD3 2: PI5 3: PA13		External Bus Interface (EBI) address output pin 07.
EBI_A08	0: PE1 1: PD4 2: PC8 3: PA14		External Bus Interface (EBI) address output pin 08.
EBI_A09	0: PE2 1: PD5 2: PC9 3: PB9		External Bus Interface (EBI) address output pin 09.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US5_RX	0: PE9 1: PA7 2: PB1 3: PH11		USART5 Asynchronous Receive. USART5 Synchronous mode Master Input / Slave Output (MISO).
US5_TX	0: PE8 1: PA6 2: PF15 3: PH10		USART5 Asynchronous Transmit. Also used as receive input in half duplex communication. USART5 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	0: PF10		USB D- pin.
USB_DP	0: PF11		USB D+ pin.
USB_ID	0: PF12		USB ID pin.
USB_VBUSEN	0: PF5		USB 5 V VBUS enable.
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6 2: PG2 3: PG8	4: PC15 5: PB0 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5 1: PD13 2: PG3 3: PG9	4: PF0 5: PB1 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.

Table 5.28. ADC1 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSADC1Y	BUSADC1X	Bus
	PF15	PF15			PB15	PB15				CH31
PF14			PF14	PB14			PB14			CH30
	PF13	PF13			PB13	PB13				CH29
PF12			PF12	PB12			PB12			CH28
	PF11	PF11			PB11	PB11				CH27
PF10			PF10	PB10			PB10			CH26
	PF9	PF9			PB9	PB9				CH25
PF8			PF8							CH24
	PF7	PF7								CH23
PF6			PF6	PB6			PB6			CH22
	PF5	PF5			PB5	PB5				CH21
PF4			PF4	PB4			PB4			CH20
	PF3	PF3			PB3	PB3				CH19
PF2			PF2	PB2			PB2			CH18
	PF1	PF1			PB1	PB1				CH17
PF0			PF0	PB0			PB0			CH16
	PE15	PE15			PA15	PA15				CH15
PE14			PE14	PA14			PA14			CH14
	PE13	PE13			PA13	PA13				CH13
PE12			PE12	PA12			PA12			CH12
	PE11	PE11			PA11	PA11				CH11
PE10			PE10	PA10			PA10			CH10
	PE9	PE9			PA9	PA9				CH9
PE8			PE8	PA8			PA8			CH8
	PE7	PE7			PA7	PA7		PH7	PH7	CH7
PE6			PE6	PA6			PA6	PH6	PH6	CH6
	PE5	PE5			PA5	PA5		PH5	PH5	CH5
PE4			PE4	PA4			PA4	PH4	PH4	CH4
					PA3	PA3		PH3	PH3	CH3
				PA2			PA2	PH2	PH2	CH2
	PE1	PE1			PA1	PA1		PH1	PH1	CH1
PE0			PE0	PA0			PA0	PH0	PH0	CH0

6.2 BGA192 PCB Land Pattern

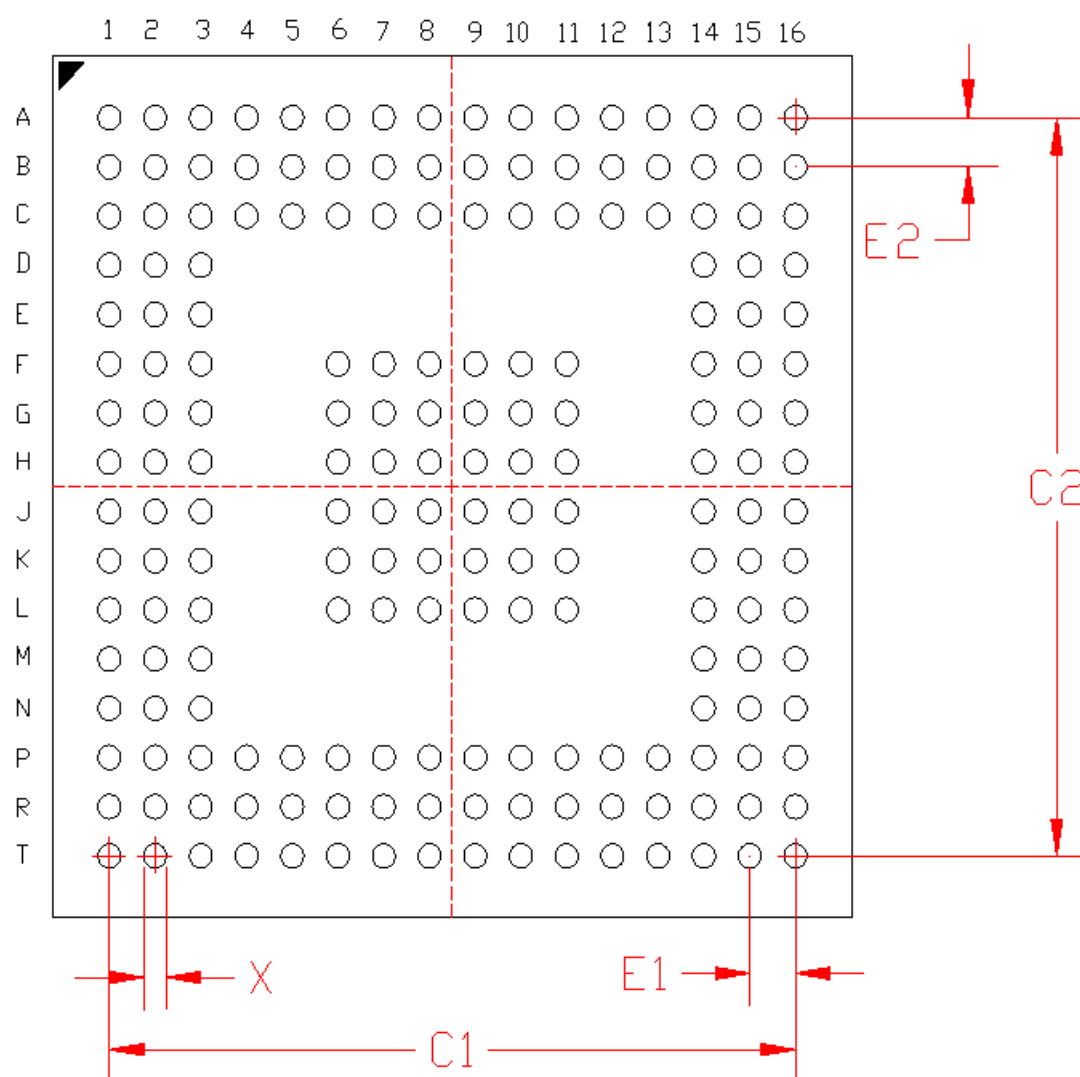


Figure 6.2. BGA192 PCB Land Pattern Drawing