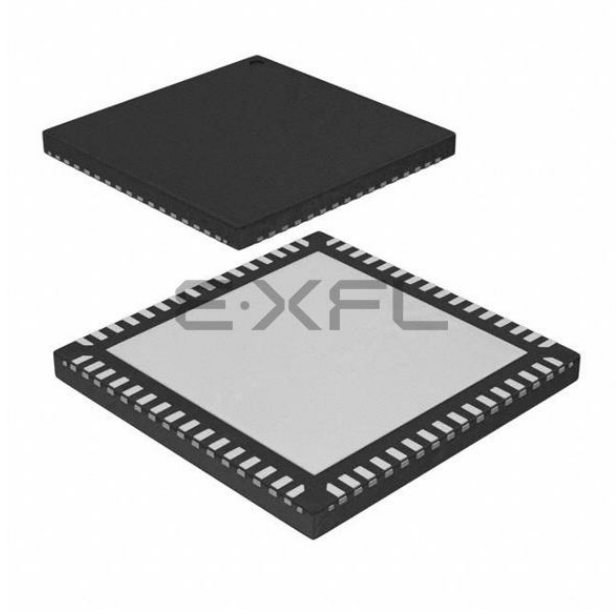
Silicon Labs - EFM32GG11B520F2048GM64-AR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b520f2048gm64-ar

- **Timers/Counters**
  - 7× 16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels (4 + 4 on one timer instance)
    - Dead-Time Insertion on several timer instances
  - 4× 32-bit Timer/Counter
  - 32-bit Real Time Counter and Calendar (RTCC)
  - 24-bit Real Time Counter (RTC)
  - 32-bit Ultra Low Energy CRYOTIMER for periodic wakeup from any Energy Mode
  - 2× 16-bit Low Energy Timer for waveform generation
  - 3× 16-bit Pulse Counter with asynchronous operation
  - 2× Watchdog Timer with dedicated RC oscillator
- **Low Energy Sensor Interface (LESENSE)**
  - Autonomous sensor monitoring in Deep Sleep Mode
  - Wide range of sensors supported, including LC sensors and capacitive buttons
  - Up to 16 inputs
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
  - 2-pin Serial Wire Debug interface
  - 1-pin Serial Wire Viewer
  - 4-pin JTAG interface
  - Embedded Trace Macrocell (ETM)
- **Pre-Programmed USB/UART Bootloader**
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - Standard (-40 °C to 85 °C T_{AMB}) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
  - QFN64 (9x9 mm)
  - TQFP64 (10x10 mm)
  - TQFP100 (14x14 mm)
  - BGA112 (10x10 mm)
  - BGA120 (7x7 mm)
  - BGA152 (8x8 mm)
  - BGA192 (7x7mm)

3.12 Configuration Summary

The features of the EFM32GG11 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA, SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	I^2S, SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	IrDA, SmartCard, High-Speed	US2_TX, US2_RX, US2_CLK, US2_CS
USART3	I^2S, SmartCard	US3_TX, US3_RX, US3_CLK, US3_CS
USART4	I^2S, SmartCard	US4_TX, US4_RX, US4_CLK, US4_CS
USART5	SmartCard	US5_TX, US5_RX, US5_CLK, US5_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
TIMER2	with DTI	TIM2_CC[2:0], TIM2_CDTI[2:0]
TIMER3	-	TIM3_CC[2:0]
TIMER4	with DTI	TIM4_CC[2:0], TIM4_CDTI[2:0]
TIMER5	-	TIM5_CC[2:0]
TIMER6	with DTI	TIM6_CC[2:0], TIM6_CDTI[2:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]
WTIMER1	-	WTIM1_CC[3:0]
WTIMER2	-	WTIM2_CC[2:0]
WTIMER3	-	WTIM3_CC[2:0]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis (V_{CM} = 1.25 V, BIASPROG[4] = 0x10, FULLBIAS[4] = 1)	$V_{ACMPHYST}$	HYSTSEL[5] = HYST0	TBD	0	TBD	mV
		HYSTSEL[5] = HYST1	TBD	18	TBD	mV
		HYSTSEL[5] = HYST2	TBD	33	TBD	mV
		HYSTSEL[5] = HYST3	TBD	46	TBD	mV
		HYSTSEL[5] = HYST4	TBD	57	TBD	mV
		HYSTSEL[5] = HYST5	TBD	68	TBD	mV
		HYSTSEL[5] = HYST6	TBD	79	TBD	mV
		HYSTSEL[5] = HYST7	TBD	90	TBD	mV
		HYSTSEL[5] = HYST8	TBD	0	TBD	mV
		HYSTSEL[5] = HYST9	TBD	-18	TBD	mV
		HYSTSEL[5] = HYST10	TBD	-33	TBD	mV
		HYSTSEL[5] = HYST11	TBD	-45	TBD	mV
		HYSTSEL[5] = HYST12	TBD	-57	TBD	mV
		HYSTSEL[5] = HYST13	TBD	-67	TBD	mV
		HYSTSEL[5] = HYST14	TBD	-78	TBD	mV
		HYSTSEL[5] = HYST15	TBD	-88	TBD	mV
Comparator delay[3]	$t_{ACMPDELAY}$	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	30	—	µs
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	3.7	—	µs
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	360	—	ns
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[4] =0x10, FULLBIAS[4] = 1	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	infinite	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	100	—	kΩ
		CSRESSEL[6] = 6	—	162	—	kΩ
		CSRESSEL[6] = 7	—	235	—	kΩ

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	µs
Settling time, (output settled within 1% of steady state value),	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption[2]	I_{IDAC}	EM0 or EM1 Source mode, excluding output current, Across operating temperature range	—	11	TBD	µA
		EM0 or EM1 Sink mode, excluding output current, Across operating temperature range	—	13	TBD	µA
		EM2 or EM3 Source mode, excluding output current, T = 25 °C	—	0.05	—	µA
		EM2 or EM3 Sink mode, excluding output current, T = 25 °C	—	0.07	—	µA
		EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C	—	11	—	µA
		EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C	—	13	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.11	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.06	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.04	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.03	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.29	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.27	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.12	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.03	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.21 Pulse Counter (PCNT)

Table 4.29. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.22 Analog Port (APORT)

Table 4.30. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current[2] [1]	I_{APORT}	Operation in EM0/EM1	—	7	—	µA
		Operation in EM2/EM3	—	915	—	nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.
2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
MISO hold time [1] [3]	t_{H_MI}	USART2, location 4, IOVDD = 1.8 V	-11.6	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	-11.6	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	-9.1	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	-9.1	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	-8	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	-8	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

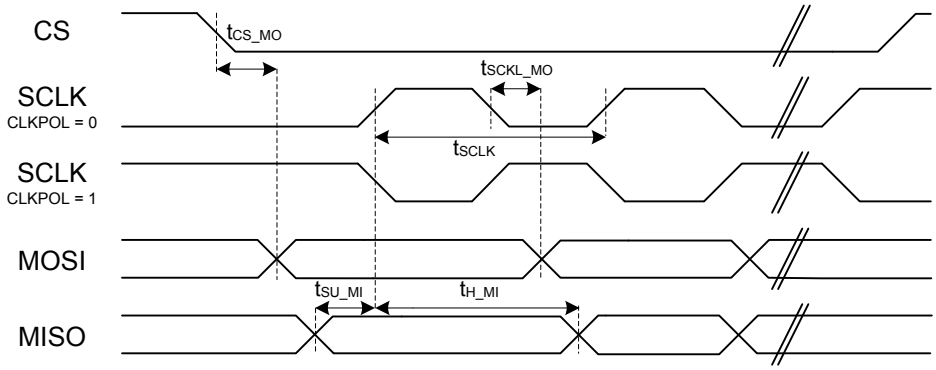

Figure 4.1. SPI Master Timing Diagram

4.1.27 Serial Data I/O Host Controller (SDIO)

SDIO DS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.46. SDIO DS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	23	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.69	3.23	—	ns
Clock fall time	t_F		1.42	2.79	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}		0	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}		0	—	14	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}		5	—	—	ns

SDIO MMC SDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.51. SDIO MMC SDR Mode Timing (Location 0, 3V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	48	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	9.4	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	9.4	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.96	3.87	—	ns
Clock fall time	t_F		1.67	3.31	—	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:7] change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	t_{OH}		3	—	—	ns

QSPI DDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 53, RX DLL = 88, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.57. QSPI DDR Mode Timing (Locations 1, 2)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Half SCLK period	T/2	HFXO	(1/F_{SCLK}) * 0.4 - 0.4	—	—	ns
		HFRCO, AUXHFRCO, USHFRCO	(1/F_{SCLK}) * 0.44	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 6.6	ns
Output hold	t_{OH}		T/2 - 52.2	—	—	ns
Input setup	t_{SU}		44.8	—	—	ns
Input hold	t_H		-2.4	—	—	ns

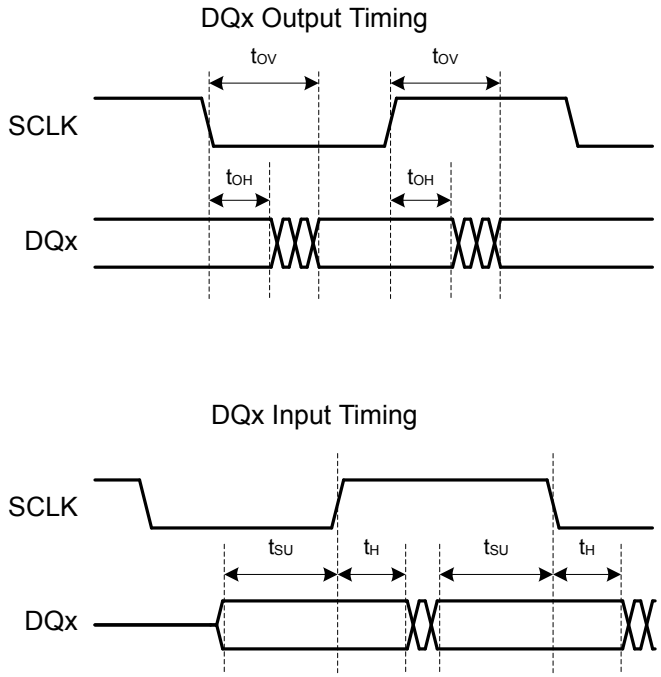

Figure 4.22. QSPI DDR Timing Diagrams

QSPI DDR Flash Timing Example

This example uses timing values for location 0 (DDR mode) to demonstrate the calculation of allowable flash timing using the QSPI in DDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 8 MHz from the HFXO clock source:
- The resulting minimum half-period, T/2(min) = (1/F_{SCLK}) * 0.4 - 0.4 = 49.6 ns.
- Flash will see a minimum setup time of T/2 – t_{OV} = T/2 – (T/2 – 5.0) = 5.0 ns.
- Flash will see a minimum hold time of t_{OH} = T/2 – 39.4 = 49.6 – 39.4 = 10.2 ns.
- Flash can have a maximum output valid time of T/2 – t_{SU} = T/2 – 33.1 = 49.6 – 33.1 = 16.5 ns.
- Flash can have a minimum output hold time of t_H = - 0.9 ns.

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 4.7 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

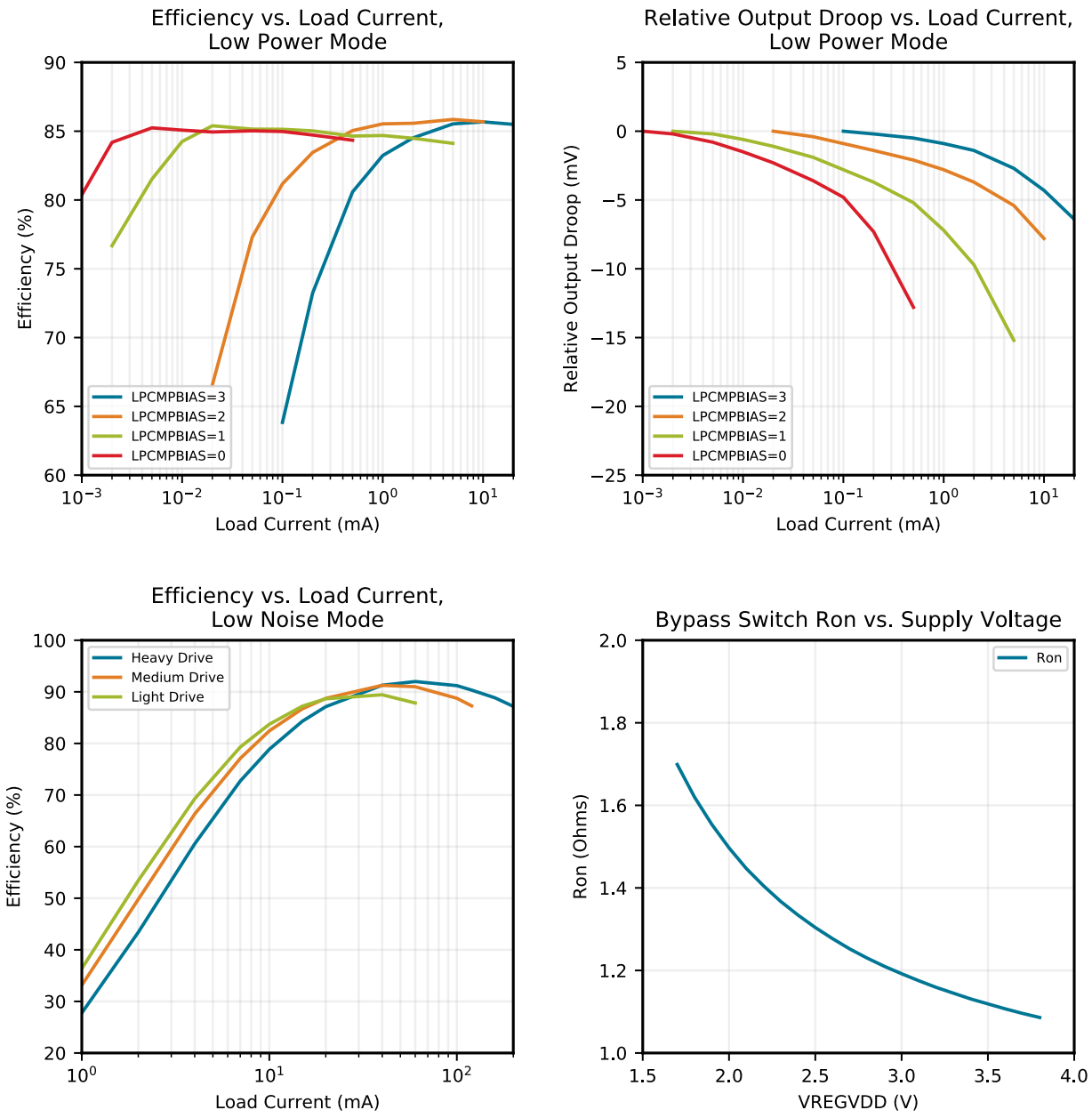

Figure 4.29. DC-DC Converter Typical Performance Characteristics

5. Pin Definitions

5.1 EFM32GG11B8xx in BGA192 Device Pinout

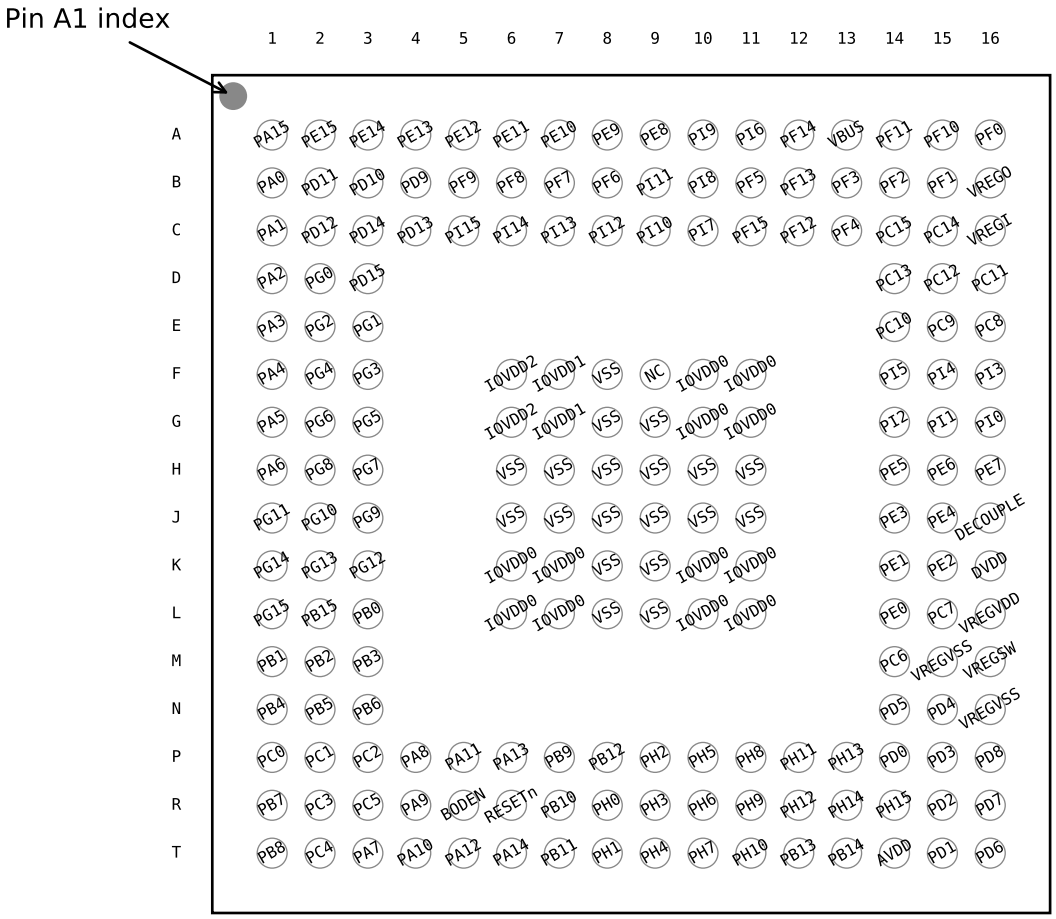

Figure 5.1. EFM32GG11B8xx in BGA192 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.1. EFM32GG11B8xx in BGA192 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA15	A1	GPIO	PE15	A2	GPIO
PE14	A3	GPIO	PE13	A4	GPIO
PE12	A5	GPIO	PE11	A6	GPIO
PE10	A7	GPIO	PE9	A8	GPIO
PE8	A9	GPIO	PI9	A10	GPIO (5V)
PI6	A11	GPIO (5V)	PF14	A12	GPIO (5V)

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD15		EBI_NANDREn #1	TIM2_CDTI2 #1 TIM3_CC0 #7 WTIM0_CDTI0 #1 PCNT1_S0IN #2	ETH_TSUEXTCLK #1 CAN0_TX #5 US5_CTS #1 I2C0_SCL #3	
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSACMP1Y BUSACMP1X	EBI_ARDY #4	TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 TIM5_CC2 #5 WTIM3_CC2 #2 PCNT0_S0IN #0 PCNT2_S1IN #4	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3 U1_RX #0 I2C2_SCL #6	LES_CH13 PRS_CH21 #1 ACMP3_O #3
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSACMP1Y BUSACMP1X		TIM1_CC3 #0 TIM5_CC1 #5 WTIM3_CC1 #2 PCNT2_S0IN #4	CAN1_RX #4 US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3 U1_TX #0 I2C2_SDA #6	CMU_CLK0 #1 LES_CH12 PRS_CH20 #1
PC11	BUSACMP1Y BUSACMP1X	EBI_ALE #4 EBI_ALE #5 EBI_A23 #1	TIM5_CC0 #5 WTIM3_CC0 #2	CAN1_TX #4 US0_TX #2 I2C1_SDA #4	LES_CH11 PRS_CH19 #1
PA3	BUSAY BUSBX LCD_SEG16	EBI_AD12 #0 EBI_VSNC #3	TIM0_CDTI0 #0 TIM3_CC0 #5	ETH_RMIIREFCLK #0 ETH_MIITXD1 #0 SDIO_DAT3 #1 US3_CS #0 U0_TX #2 QSPI0_DQ1 #1	CMU_CLK2 #1 CMU_CLKI0 #1 CMU_CLK2 #4 LES_ALTEX2 PRS_CH9 #1 ETM_TD1 #3
PG2	BUSACMP2Y BUSACMP2X	EBI_AD02 #2	TIM6_CC2 #0 TIM2_CDTI2 #3 WTIM0_CC0 #2 LETIM1_OUT0 #7	ETH_MIITXD2 #1 US3_CLK #4 QSPI0_DQ1 #2	CMU_CLK0 #3
PG1	BUSACMP2Y BUSACMP2X	EBI_AD01 #2	TIM6_CC1 #0 TIM2_CDTI1 #3 WTIM0_CDTI2 #1 LETIM1_OUT1 #6	ETH_MIITXD3 #1 US3_RX #4 QSPI0_DQ0 #2	CMU_CLK1 #3
PC10	BUSACMP1Y BUSACMP1X	EBI_A10 #2 EBI_A22 #1	TIM2_CC2 #2 TIM5_CC2 #4 WTIM3_CC2 #1	CAN1_TX #3 US0_RX #2	LES_CH10 PRS_CH18 #1
PC9	BUSACMP1Y BUSACMP1X	EBI_A09 #2 EBI_A21 #1 EBI_A27 #3	TIM2_CC1 #2 TIM5_CC1 #4 WTIM3_CC1 #1	CAN1_RX #3 US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2
PC8	BUSACMP1Y BUSACMP1X	EBI_A08 #2 EBI_A15 #0 EBI_A20 #1 EBI_A26 #3	TIM2_CC0 #2 TIM5_CC0 #4 WTIM3_CC0 #1	US0_CS #2	LES_CH8 PRS_CH4 #0
PA4	BUSBY BUSAX LCD_SEG17	EBI_AD13 #0 EBI_HSNC #3	TIM0_CDTI1 #0 TIM3_CC1 #5	ETH_RMIICRSDV #0 ETH_MIITXD0 #0 SDIO_DAT4 #1 US3_CTS #0 U0_RX #2 QSPI0_DQ2 #1	LES_ALTEX3 PRS_CH16 #0 ETM_TD2 #3
PG4	BUSACMP2Y BUSACMP2X	EBI_AD04 #2	TIM6_CDTI1 #0 WTIM0_CC2 #2	ETH_MIITXD0 #1 US3_CTS #4 QSPI0_DQ3 #2	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.
LES_CH0	0: PC0		LESENSE channel 0.
LES_CH1	0: PC1		LESENSE channel 1.
LES_CH2	0: PC2		LESENSE channel 2.
LES_CH3	0: PC3		LESENSE channel 3.
LES_CH4	0: PC4		LESENSE channel 4.
LES_CH5	0: PC5		LESENSE channel 5.
LES_CH6	0: PC6		LESENSE channel 6.
LES_CH7	0: PC7		LESENSE channel 7.
LES_CH8	0: PC8		LESENSE channel 8.
LES_CH9	0: PC9		LESENSE channel 9.
LES_CH10	0: PC10		LESENSE channel 10.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_CH11	0: PC11		LESENSE channel 11.
LES_CH12	0: PC12		LESENSE channel 12.
LES_CH13	0: PC13		LESENSE channel 13.
LES_CH14	0: PC14		LESENSE channel 14.
LES_CH15	0: PC15		LESENSE channel 15.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8 7: PB9	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9 7: PB10	Low Energy Timer LETIM0, output channel 1.
LETIM1_OUT0	0: PA7 1: PA11 2: PA12 3: PC2	4: PB5 5: PB2 6: PG0 7: PG2	Low Energy Timer LETIM1, output channel 0.
LETIM1_OUT1	0: PA6 1: PA13 2: PA14 3: PC3	4: PB6 5: PB1 6: PG1 7: PG3	Low Energy Timer LETIM1, output channel 1.
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	0: PC7 1: PA6 2: PD3 3: PB1	4: PB5 5: PH1	LEUART1 Receive input.
LEU1_TX	0: PC6 1: PA5 2: PD2 3: PB0	4: PB4 5: PH0	LEUART1 Transmit output. Also used as receive input in half duplex communication.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PCNT0_S0IN	0: PC13 1: PE0 2: PC0 3: PD6	4: PA0 5: PB0 6: PB5 7: PB12	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PC14 1: PE1 2: PC1 3: PD7	4: PA1 5: PB1 6: PB6 7: PB11	Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	0: PA5 1: PB3 2: PD15 3: PC4	4: PA7 5: PA12 6: PB11 7: PG14	Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	0: PA6 1: PB4 2: PB0 3: PC5	4: PA8 5: PA13 6: PB12 7: PG15	Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	0: PD0 1: PE8 2: PB13 3: PF10	4: PC12 5: PI2 6: PI0 7: PH14	Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	0: PD1 1: PE9 2: PB14 3: PF11	4: PC13 5: PI1 6: PH15 7: PH13	Pulse Counter PCNT2 input number 1.
PRS_CH0	0: PA0 1: PF3 2: PC14 3: PF2		Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PA1 1: PF4 2: PC15 3: PE12		Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PC0 1: PF5 2: PE10 3: PE13		Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PC1 1: PE8 2: PE11 3: PA0		Peripheral Reflex System PRS, channel 3.
PRS_CH4	0: PC8 1: PB0 2: PF1		Peripheral Reflex System PRS, channel 4.
PRS_CH5	0: PC9 1: PB1 2: PD6		Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA6 1: PB14 2: PE6		Peripheral Reflex System PRS, channel 6.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM4_CDTI2	0: PD3		Timer 4 Complimentary Dead Time Insertion channel 2.
TIM5_CC0	0: PE4 1: PE7 2: PH13 3: PI0	4: PC8 5: PC11 6: PC14 7: PF12	Timer 5 Capture Compare input / output channel 0.
TIM5_CC1	0: PE5 1: PH11 2: PH14 3: PI1	4: PC9 5: PC12 6: PF10 7: PF13	Timer 5 Capture Compare input / output channel 1.
TIM5_CC2	0: PE6 1: PH12 2: PH15 3: PI2	4: PC10 5: PC13 6: PF11 7: PF14	Timer 5 Capture Compare input / output channel 2.
TIM6_CC0	0: PG0 1: PG6 2: PG12 3: PH2	4: PH8 5: PB13 6: PD1 7: PD4	Timer 6 Capture Compare input / output channel 0.
TIM6_CC1	0: PG1 1: PG7 2: PG13 3: PH3	4: PH9 5: PB14 6: PD2 7: PD5	Timer 6 Capture Compare input / output channel 1.
TIM6_CC2	0: PG2 1: PG8 2: PG14 3: PH4	4: PH10 5: PD0 6: PD3 7: PD6	Timer 6 Capture Compare input / output channel 2.
TIM6_CDTI0	0: PG3 1: PG9 2: PE4 3: PH5		Timer 6 Complimentary Dead Time Insertion channel 0.
TIM6_CDTI1	0: PG4 1: PG10 2: PE5 3: PH6		Timer 6 Complimentary Dead Time Insertion channel 1.
TIM6_CDTI2	0: PG5 1: PG11 2: PE6 3: PH7		Timer 6 Complimentary Dead Time Insertion channel 2.
U0_CTS	0: PF8 1: PE2 2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.
U0_RTS	0: PF9 1: PE3 2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	0: PF7 1: PE1 2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
U0_TX	0: PF6 1: PE0 2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.
U1_CTS	0: PC14 1: PF9 2: PB11 3: PE4	4: PC4 5: PH13	UART1 Clear To Send hardware flow control input.
U1_RTS	0: PC15 1: PF8 2: PB12 3: PE5	4: PC5 5: PH14	UART1 Request To Send hardware flow control output.
U1_RX	0: PC13 1: PF11 2: PB10 3: PE3	4: PE13 5: PH12	UART1 Receive input.
U1_TX	0: PC12 1: PF10 2: PB9 3: PE2	4: PE12 5: PH11	UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12 6: PG14	USART0 clock input / output.
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13 6: PG15	USART0 chip select input / output.
US0_CTS	0: PE14 1: PE3 2: PC7 3: PC13	4: PB6 5: PB11 6: PH0	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PE15 1: PE2 2: PC6 3: PC12	4: PB5 5: PD6 6: PH1	USART0 Request To Send hardware flow control output.
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1 6: PG13	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0 6: PG12	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4 6: PB2	USART1 chip select input / output.

6.3 BGA192 Package Marking

Figure 6.3. BGA192 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

Table 7.1. BGA152 Package Dimensions

Dimension	Min	Typ	Max
A	0.78	0.84	0.90
A1	0.13	0.18	0.23
A3	0.16	0.20	0.24
A2		0.45 REF	
D		8.00 BSC	
e		0.50 BSC	
E		8.00 BSC	
D1		6.50 BSC	
E1		6.50 BSC	
b	0.20	0.25	0.30
aaa		0.10	
bbb		0.10	
ddd		0.08	
eee		0.15	
fff		0.05	

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 11.2. TQFP64 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11.3 TQFP64 Package Marking

Figure 11.3. TQFP64 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.