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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I <sup>2</sup> C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b520f2048gq100-a

Email: info@E-XFL.COM

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# Timers/Counters

- 7× 16-bit Timer/Counter
  - 3 + 4 Compare/Capture/PWM channels (4 + 4 on one timer instance)
  - Dead-Time Insertion on several timer instances
- 4× 32-bit Timer/Counter
- 32-bit Real Time Counter and Calendar (RTCC)
- 24-bit Real Time Counter (RTC)
- 32-bit Ultra Low Energy CRYOTIMER for periodic wakeup from any Energy Mode
- 2× 16-bit Low Energy Timer for waveform generation
- 3× 16-bit Pulse Counter with asynchronous operation
- 2× Watchdog Timer with dedicated RC oscillator

# Low Energy Sensor Interface (LESENSE)

- Autonomous sensor monitoring in Deep Sleep Mode
- Wide range of sensors supported, including LC sensors and capacitive buttons
- Up to 16 inputs
- Ultra efficient Power-on Reset and Brown-Out Detector
- Debug Interface
  - 2-pin Serial Wire Debug interface
  - 1-pin Serial Wire Viewer
  - 4-pin JTAG interface
  - Embedded Trace Macrocell (ETM)

Pre-Programmed USB/UART Bootloader

# Wide Operating Range

- 1.8 V to 3.8 V single power supply
- Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
- Standard (-40  $^\circ C$  to 85  $^\circ C$   $T_{AMB})$  and Extended (-40  $^\circ C$  to 125  $^\circ C$   $T_J)$  temperature grades available
- Packages
  - QFN64 (9x9 mm)
  - TQFP64 (10x10 mm)
  - TQFP100 (14x14 mm)
  - BGA112 (10x10 mm)
  - BGA120 (7x7 mm)
  - BGA152 (8x8 mm)
  - BGA192 (7x7mm)

#### 3.7 Security Features

#### 3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

### 3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Giant Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2<sup>m</sup>), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

#### 3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

#### 3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

### 3.8 Analog

### 3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

### 3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

### 3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

# 4. Electrical Specifications

### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on  $T_{AMB}$ =25 °C and  $V_{DD}$ = 3.3 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to 4.1.2.1 General Operating Conditions for more details about operational supply and temperature limits.

### 4.1.7.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.8.	<b>Current Co</b>	nsumption 3.3	V using	DC-DC	Converter
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Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_DCM	72 MHz HFRCO, CPU running Prime from flash	_	80	—	µA/MHz
DCM mode <sup>2</sup>		72 MHz HFRCO, CPU running while loop from flash	—	80		µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	92		µA/MHz
		50 MHz crystal, CPU running while loop from flash	_	84		µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	84		µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	90		µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	_	94		µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	_	109		µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	_	698		µA/MHz
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_CCM	72 MHz HFRCO, CPU running Prime from flash	_	84		µA/MHz
CCM mode <sup>1</sup>		72 MHz HFRCO, CPU running while loop from flash	—	84		µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	_	95		µA/MHz
		50 MHz crystal, CPU running while loop from flash	_	91		µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	92		µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	_	104		µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	113	_	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	_	142	_	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1264		µA/MHz

### 4.1.7.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

# Table 4.9. Current Consumption 1.8 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Current consumption in EM0 mode with all peripherals dis-	IACTIVE	72 MHz HFRCO, CPU running Prime from flash	_	120	—	µA/MHz
abled		72 MHz HFRCO, CPU running while loop from flash	_	120	_	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	_	140	_	µA/MHz
		50 MHz crystal, CPU running while loop from flash	_	122	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	_	122	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	_	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	_	126	_	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	_	131	_	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	_	315	—	µA/MHz
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_VS	19 MHz HFRCO, CPU running while loop from flash	_	107	—	µA/MHz
enabled		1 MHz HFRCO, CPU running while loop from flash	_	259	—	µA/MHz
Current consumption in EM1	IEM1	72 MHz HFRCO	_	57	_	µA/MHz
abled		50 MHz crystal	_	59	_	µA/MHz
		48 MHz HFRCO	_	59	—	µA/MHz
		32 MHz HFRCO	_	61	_	µA/MHz
		26 MHz HFRCO	_	63	_	µA/MHz
		16 MHz HFRCO	_	68	_	µA/MHz
		1 MHz HFRCO	_	252	—	µA/MHz
Current consumption in EM1	I <sub>EM1_VS</sub>	19 MHz HFRCO	_	55	_	µA/MHz
abled and voltage scaling enabled		1 MHz HFRCO	_	207	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling	I <sub>EM2_VS</sub>	Full 512 kB RAM retention and RTCC running from LFXO	_	3.7	_	μA
enabled		Full 512 kB RAM retention and RTCC running from LFRCO	_	4.0	_	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO <sup>2</sup>	_	2.5	_	μA

# 4.1.15 Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input voltage range		ACMPVDD = ACMPn_CTRL_PWRSEL <sup>1</sup>	—	—	V <sub>ACMPVDD</sub>	V
Supply voltage	VACMPVDD	$BIASPROG^4 \le 0x10 \text{ or } FULL-BIAS^4 = 0$	1.8	_	V <sub>VREGVDD</sub> MAX	V
		$0x10 < BIASPROG^4 \le 0x20$ and FULLBIAS <sup>4</sup> = 1	2.1	_	V <sub>VREGVDD</sub> MAX	V
Active current not including	I <sub>ACMP</sub>	$BIASPROG^4 = 1$ , $FULLBIAS^4 = 0$		50	_	nA
voltage reference <sup>2</sup>		$BIASPROG^4 = 0x10, FULLBIAS^4 = 0$	_	306	—	nA
		$BIASPROG^4 = 0x02, FULLBIAS^4$ $= 1$	_	6.5	—	μA
		BIASPROG <sup>4</sup> = 0x20, FULLBIAS <sup>4</sup> = 1	_	74	TBD	μA
Current consumption of inter- nal voltage reference <sup>2</sup>	IACMPREF	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	_	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	μA
		VADIV selected as input using VDD/1		2.4	_	μA

# Table 4.23. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Supply current, continuous conversions, WARMUP- MODE=KEEPCSENWARM	ICSEN_ACTIVE	SAR or Delta Modulation conver- sions of 33 pF capacitor, CS0CG=0 (Gain = 10x), always on		90.5		μA
HFPERCLK supply current	ICSEN_HFPERCLK	Current contribution from HFPERCLK when clock to CSEN block is enabled.	_	2.25	_	µA/MHz

# Note:

 Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total\_current = single\_sample\_current \* (number\_of\_channels \* accumulation)).

# 4.1.23.3 I2C Fast-mode Plus (Fm+)<sup>1</sup>

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
SCL clock frequency <sup>2</sup>	f <sub>SCL</sub>		0	_	1000	kHz
SCL clock low time	t <sub>LOW</sub>		0.5	_	_	μs
SCL clock high time	t <sub>ніGH</sub>		0.26	—	_	μs
SDA set-up time	t <sub>SU_DAT</sub>		50	_	—	ns
SDA hold time	t <sub>HD_DAT</sub>		100	_	_	ns
Repeated START condition set-up time	t <sub>SU_STA</sub>		0.26	_	_	μs
(Repeated) START condition hold time	t <sub>HD_STA</sub>		0.26	—	—	μs
STOP condition set-up time	t <sub>SU_STO</sub>		0.26	_	_	μs
Bus free time between a STOP and START condition	t <sub>BUF</sub>		0.5	—	—	μs

# Table 4.33. I2C Fast-mode Plus (Fm+)<sup>1</sup>

## Note:

1. For CLHR set to 0 or 1 in the I2Cn\_CTRL register.

2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

# 4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF3	В9	GPIO
PF1	B10	GPIO (5V)	PF12	B11	GPIO
VBUS	B12	USB VBUS signal and auxiliary input to 5 V regulator.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 K12 L12 L13 M8 M11 N8	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L14	Digital IO power supply 0.
PF0	C10	GPIO (5V)	PE4	C11	GPIO
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PE5	D11	GPIO
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PE6	E11	GPIO
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE7	F11	GPIO
PC8	F12	GPIO (5V)	PC9	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE0	G11	GPIO (5V)
PE1	G12	GPIO (5V)	PE3	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
PC7	H13	GPIO	PD14	J1	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 59 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB9	37	GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	45	GPIO (5V)	PD1	46	GPIO
PD2	47	GPIO (5V)	PD3	48	GPIO
PD4	49	GPIO	PD5	50	GPIO
PD6	51	GPIO	PD7	52	GPIO
PD8	53	GPIO	PC7	54	GPIO
VREGVSS	55	Voltage regulator VSS	VREGSW	56	DCDC regulator switching node
VREGVDD	57	Voltage regulator VDD input	DVDD	58	Digital power supply.
DECOUPLE	60	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE1	61	GPIO (5V)
PE2	62	GPIO	PE3	63	GPIO
PE4	64	GPIO	PE5	65	GPIO
PE6	66	GPIO	PE7	67	GPIO
PC8	68	GPIO (5V)	PC9	69	GPIO (5V)
PC10	70	GPIO (5V)	PC11	71	GPIO (5V)
VREGI	72	Input to 5 V regulator.	VREGO	73	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs
PF10	74	GPIO (5V)	PF11	75	GPIO (5V)
PF0	76	GPIO (5V)	PF1	77	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF1	77	GPIO (5V)	PF2	78	GPIO
VBUS	79	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	80	GPIO
PF5	81	GPIO	PF6	84	GPIO
PF7	85	GPIO	PF8	86	GPIO
PF9	87	GPIO	PD9	88	GPIO
PD10	89	GPIO	PD11	90	GPIO
PD12	91	GPIO	PE8	92	GPIO
PE9	93	GPIO	PE10	94	GPIO
PE11	95	GPIO	PE12	96	GPIO
PE13	97	GPIO	PE14	98	GPIO
PE15	99	GPIO	PA15	100	GPIO
Note:	•			•	•

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description							
	Analog	EBI	Timers	Communication	Other			
PH14	BUSACMP3Y BU- SACMP3X	EBI_A26 #2	TIM5_CC1 #2 WTIM1_CC2 #7 PCNT2_S0IN #7	US5_CTS #3 U1_RTS #5 I2C1_SCL #6				
PH15	BUSACMP3Y BU- SACMP3X	EBI_A27 #2	TIM5_CC2 #2 WTIM1_CC3 #7 PCNT2_S1IN #6	US5_RTS #3				
PD2	BUSADC0Y BU- SADC0X	EBI_A06 #1 EBI_A15 #3 EBI_A27 #0	TIM0_CC1 #2 TIM6_CC1 #6 WTIM1_CC0 #1	US1_CLK #1 LEU1_TX #2	DBG_SWO #3			
PD7	BUSADCOY BU- SADCOX ADC0_EXTN ADC1_EXTN OPA1_N	EBI_A11 #1 EBI_A20 #3	TIM1_CC1 #4 WTIM1_CC1 #2 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 US3_CLK #1 U0_TX #6 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 ACMP1_O #2 ETM_TCLK #0			
PB8	LFXTAL_N		TIM0_CDTI1 #4 TIM1_CC1 #3	US0_RX #4 US1_CS #0 US4_RX #0 U0_RTS #4	CMU_CLKI0 #2 PRS_CH23 #0			
PC4	BUSACMP0Y BU- SACMP0X OPA0_P	EBI_AD11 #1 EBI_ALE #2 EBI_NANDREn #3 EBI_A26 #0	TIM0_CC0 #5 TIM0_CDTI2 #3 TIM2_CC2 #5 LE- TIM0_OUT0 #3 PCNT1_S0IN #3	SDIO_CD #1 US2_CLK #0 US4_CLK #0 U0_TX #4 U1_CTS #4 I2C1_SDA #0	LES_CH4 PRS_CH18 #2 GPIO_EM4WU6			
PA7	BUSAY BUSBX LCD_SEG35	EBI_AD13 #1 EBI_A01 #3 EBI_CSTFT #0	TIM0_CC2 #5 LE- TIM1_OUT0 #0 PCNT1_S0IN #4	US2_TX #2 US4_CTS #0 US5_RX #1	PRS_CH7 #1			
PA10	BUSBY BUSAX LCD_SEG38	EBI_CS0 #1 EBI_A04 #3 EBI_VSNC #0	TIM2_CC2 #0 TIM0_CC2 #6 WTIM2_CC1 #0	US2_CS #2	PRS_CH10 #0			
PA12	BUSBY BUSAX	EBI_CS2 #1 EBI_REn #2 EBI_A00 #0 EBI_A06 #3	TIM2_CC0 #1 WTIM0_CDTI0 #2 WTIM2_CC0 #1 LE- TIM1_OUT0 #2 PCNT1_S0IN #5	CAN1_RX #5 US0_CLK #5 US2_RTS #2	CMU_CLK0 #5 PRS_CH12 #0 ACMP1_O #3			
PA14	BUSBY BUSAX LCD_BEXT	EBI_REn #1 EBI_A02 #0 EBI_A08 #3	TIM2_CC2 #1 WTIM0_CDTI2 #2 WTIM2_CC2 #1 LE- TIM1_OUT1 #2	US1_TX #6 US2_RX #3 US3_RTS #2	PRS_CH14 #0 ACMP1_O #4			
PB11	BUSAY BUSBX VDAC0_OUT0 / OPA0_OUT IDAC0_OUT	EBI_BL1 #2 EBI_A02 #1 EBI_A11 #3	TIM0_CDTI2 #4 TIM1_CC2 #3 WTIM2_CC2 #2 LE- TIM0_OUT0 #1 PCNT0_S1IN #7 PCNT1_S0IN #6	US0_CTS #5 US1_CLK #5 US2_CS #3 US5_CLK #0 U1_CTS #2 I2C1_SDA #1	CMU_CLK1 #5 CMU_CLK10 #7 PRS_CH21 #2 ACMP0_O #3 GPIO_EM4WU7			
PH1	BUSADC1Y BU- SADC1X	EBI_DTEN #2		US0_RTS #6 LEU1_RX #5				
PH4	BUSADC1Y BU- SADC1X	EBI_A16 #2	TIM6_CC2 #3 WTIM2_CC0 #6	US4_TX #4				
PH7	BUSADC1Y BU- SADC1X	EBI_A19 #2	TIM6_CDTI2 #3 WTIM2_CC0 #7	US4_CS #4				
PH10	BUSACMP3Y BU- SACMP3X	EBI_A22 #2	TIM6_CC2 #4 WTIM1_CC2 #6	US5_TX #3				

Alternate	LOCA		
Functionality	0 - 3	4 - 7	Description
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PF6		LCD segment line 24.
LCD_SEG25	0: PF7		LCD segment line 25.
LCD_SEG26	0: PF8		LCD segment line 26.
LCD_SEG27	0: PF9		LCD segment line 27.
LCD_SEG28	0: PD9		LCD segment line 28.
LCD_SEG29	0: PD10		LCD segment line 29.
LCD_SEG30	0: PD11		LCD segment line 30.
LCD_SEG31	0: PD12		LCD segment line 31.
LCD_SEG32	0: PB0		LCD segment line 32.

Alternate LOCATION			
Functionality	0 - 3	4 - 7	Description
US5 RX	0: PE9 1: PA7		USART5 Asynchronous Receive.
	2: PB1 3: PH11		USART5 Synchronous mode Master Input / Slave Output (MISO).
US5_TX	0: PE8 1: PA6		USART5 Asynchronous Transmit. Also used as receive input in half duplex communica- tion.
	2. PF 15 3: PH10		USART5 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	0: PF10		USB D- pin.
USB_DP	0: PF11		USB D+ pin.
USB_ID	0: PF12		USB ID pin.
USB_VBUSEN	0: PF5		USB 5 V VBUS enable.
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6 2: PG2 3: PG8	4: PC15 5: PB0 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5 1: PD13 2: PG3 3: PG9	4: PF0 5: PB1 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.

Alternate Functionality	Location	Priority
QSPI0_DQS	0: PF9	High Speed
QSPI0_SCLK	0: PF6	High Speed
SDIO_CLK	0: PE13	High Speed
SDIO_CMD	0: PE12	High Speed
SDIO_DAT0	0: PE11	High Speed
SDIO_DAT1	0: PE10	High Speed
SDIO_DAT2	0: PE9	High Speed
SDIO_DAT3	0: PE8	High Speed
SDIO_DAT4	0: PD12	High Speed
SDIO_DAT5	0: PD11	High Speed
SDIO_DAT6	0: PD10	High Speed
SDIO_DAT7	0: PD9	High Speed
TIM0_CC0	3: PB6	Non-interference
TIM0_CC1	3: PC0	Non-interference
TIM0_CC2	3: PC1	Non-interference
TIM0_CDTI0	1: PC13	Non-interference
TIM0_CDTI1	1: PC14	Non-interference
TIM0_CDTI2	1: PC15	Non-interference
TIM2_CC0	0: PA8	Non-interference
TIM2_CC1	0: PA9	Non-interference
TIM2_CC2	0: PA10	Non-interference
TIM2_CDTI0	0: PB0	Non-interference
TIM2_CDTI1	0: PB1	Non-interference
TIM2_CDTI2	0: PB2	Non-interference
TIM4_CC0	0: PF3	Non-interference
TIM4_CC1	0: PF4	Non-interference
TIM4_CC2	0: PF12	Non-interference
TIM4_CDTI0	0: PD0	Non-interference
TIM4_CDTI1	0: PD1	Non-interference
TIM4_CDTI2	0: PD3	Non-interference
TIM6_CC0	0: PG0	Non-interference
TIM6_CC1	0: PG1	Non-interference
TIM6_CC2	0: PG2	Non-interference
TIM6_CDTI0	0: PG3	Non-interference
TIM6_CDTI1	0: PG4	Non-interference
TIM6_CDTI2	0: PG5	Non-interference

Port	sng	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
<b>APORT0X</b>	<b>BUSADC0X</b>																									PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
<b>APORT0Y</b>	<b>BUSADC0Y</b>																									PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	Xasua	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

# Table 5.27. ADC0 Bus and Pin Mapping

#### 7.2 BGA152 PCB Land Pattern



Figure 7.2. BGA152 PCB Land Pattern Drawing

### Table 7.2. BGA152 PCB Land Pattern Dimensions

Dimension	Min	Nom	Мах
X		0.20	
C1		6.50	
C2		6.50	
E1		0.5	
E2		0.5	

## Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.

3. This Land Pattern Design is based on the IPC-7351 guidelines.

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

6. The stencil thickness should be 0.125 mm (5 mils).

7. The ratio of stencil aperture to land pad size should be 1:1.

8. A No-Clean, Type-3 solder paste is recommended.

9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Dimension	Min	Тур	Мах							
A	-	-	1.30							
A1	0.55	0.60	0.65							
A2	0.21 BSC									
A3	0.30	0.35	0.40							
d	0.43	0.48	0.53							
D	10.00 BSC									
D1	8.00 BSC									
E	10.00 BSC									
E1	8.00 BSC									
e1	0.80 BSC									
e2	0.80 BSC									
L1		1.00 REF								
L2	1.00 REF									

### Table 9.1. BGA112 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.