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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

# Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

# Details

E·XFI

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I <sup>2</sup> C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b520f2048gq64-br

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# 3. System Overview

# 3.1 Introduction

The Giant Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Giant Gecko Series 1 Reference Manual.

A block diagram of the Giant Gecko Series 1 family is shown in Figure 3.1 Detailed EFM32GG11 Block Diagram on page 11. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.



Figure 3.1. Detailed EFM32GG11 Block Diagram

# 3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

# 3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

# 3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

# 3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

# 3.4.2 Internal and External Oscillators

The EFM32GG11 supports two crystal oscillators and fully integrates five RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 50 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxiliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (USHFRCO) is available for timing the USB, SDIO and QSPI peripherals. The USHFRCO can be syncronized to the host's USB clock to allow the USB to operate in device mode without the additional cost of an external crystal.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

# 3.5 Counters/Timers and PWM

# 3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER\_0 only.

# 3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER\_0 only.

### 3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

### 3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of wave-forms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

### 3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

# 3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

### 3.8.5 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05  $\mu$ A and 64  $\mu$ A with several ranges consisting of various step sizes.

# 3.8.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per singleended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

# 3.8.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

### 3.8.8 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x36 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

### 3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32GG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

# 3.10 Core and Memory

### 3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor with FPU achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 2048 kB flash program memory
  - · Dual-bank memory with read-while-write support
- Up to 512 kB RAM data memory
- · Configuration and event handling of all modules
- · 2-pin Serial-Wire or 4-pin JTAG debug interface

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Frequency limits	f <sub>HFRCO_BAND</sub>	FREQRANGE = 0, FINETUNIN- GEN = 0	1	_	10	MHz
		FREQRANGE = 3, FINETUNIN- GEN = 0	2	—	17	MHz
		FREQRANGE = 6, FINETUNIN- GEN = 0	4	—	30	MHz
		FREQRANGE = 7, FINETUNIN- GEN = 0	5	—	34	MHz
		FREQRANGE = 8, FINETUNIN- GEN = 0	7	_	42	MHz
		FREQRANGE = 10, FINETUNIN- GEN = 0	12	_	58	MHz
		FREQRANGE = 11, FINETUNIN- GEN = 0	15		68	MHz
		FREQRANGE = 12, FINETUNIN- GEN = 0	18	_	83	MHz
		FREQRANGE = 13, FINETUNIN- GEN = 0	24		100	MHz
		FREQRANGE = 14, FINETUNIN- GEN = 0	28	_	119	MHz
		FREQRANGE = 15, FINETUNIN- GEN = 0	33	_	138	MHz
		FREQRANGE = 16, FINETUNIN- GEN = 0	43		163	MHz

### Note:

1. Maximum DPLL lock time ~= 6 x (M+1) x  $t_{REF}$ , where  $t_{REF}$  is the reference clock period.

# 4.1.17 Current Digital to Analog Converter (IDAC)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Number of ranges	N <sub>IDAC_RANGES</sub>		—	4	_	ranges
Output current	IIDAC_OUT	RANGSEL <sup>1</sup> = RANGE0	0.05	_	1.6	μA
		RANGSEL <sup>1</sup> = RANGE1	1.6	_	4.7	μA
		RANGSEL <sup>1</sup> = RANGE2	0.5	_	16	μA
		RANGSEL <sup>1</sup> = RANGE3	2	_	64	μA
Linear steps within each range	N <sub>IDAC_STEPS</sub>		_	32	_	steps
Step size	SSIDAC	RANGSEL <sup>1</sup> = RANGE0	_	50	_	nA
		RANGSEL <sup>1</sup> = RANGE1	—	100	_	nA
		RANGSEL <sup>1</sup> = RANGE2	_	500	_	nA
		RANGSEL <sup>1</sup> = RANGE3	—	2	—	μA
Total accuracy, STEPSEL <sup>1</sup> = 0x10	ACCIDAC	EM0 or EM1, AVDD=3.3 V, T = 25 °C	TBD	_	TBD	%
		EM0 or EM1, Across operating temperature range	TBD	—	TBD	%
		EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE0, AVDD=3.3 V, T = 25 °C	_	-2.7	_	%
		EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE1, AVDD=3.3 V, T = 25 °C	_	-2.5	_	%
		EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE2, AVDD=3.3 V, T = 25 °C	_	-1.5	_	%
		EM2 or EM3, Source mode, RANGSEL <sup>1</sup> = RANGE3, AVDD=3.3 V, T = 25 °C	_	-1.0	_	%
		EM2 or EM3, Sink mode, RANG- SEL <sup>1</sup> = RANGE0, AVDD=3.3 V, T = 25 °C	_	-1.1	_	%
		EM2 or EM3, Sink mode, RANG- SEL <sup>1</sup> = RANGE1, AVDD=3.3 V, T = 25 °C	_	-1.1	_	%
		EM2 or EM3, Sink mode, RANG- SEL <sup>1</sup> = RANGE2, AVDD=3.3 V, T = 25 °C	_	-0.9	_	%
		EM2 or EM3, Sink mode, RANG- SEL <sup>1</sup> = RANGE3, AVDD=3.3 V, T = 25 °C	_	-0.9	_	%

# Table 4.25. Current Digital to Analog Converter (IDAC)

# 4.1.19 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1,  $C_{LOAD}$  = 75 pF with OUTSCALE = 0, or  $C_{LOAD}$  = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes<sup>8 1</sup>.

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Supply voltage (from AVDD)	V <sub>OPA</sub>	HCMDIS = 0, Rail-to-rail input range	2	—	3.8	V
		HCMDIS = 1	1.62	_	3.8	V
Input voltage	V <sub>IN</sub>	HCMDIS = 0, Rail-to-rail input range	V <sub>VSS</sub>	_	V <sub>OPA</sub>	V
		HCMDIS = 1	V <sub>VSS</sub>	_	V <sub>OPA</sub> -1.2	V
Input impedance	R <sub>IN</sub>		100	_	—	MΩ
Output voltage	V <sub>OUT</sub>		V <sub>VSS</sub>	_	V <sub>OPA</sub>	V
Load capacitance <sup>2</sup>	C <sub>LOAD</sub>	OUTSCALE = 0	_	—	75	pF
		OUTSCALE = 1	_	_	37.5	pF
Output impedance	R <sub>OUT</sub>	$\label{eq:VOUT} \begin{array}{l} DRIVESTRENGTH = 2 \text{ or } 3, 0.4 \text{ V} \\ \leq V_{OUT} \leq V_{OPA} \text{ - } 0.4 \text{ V}, \text{ -8 mA } < \\ I_{OUT} < 8 \text{ mA}, \text{ Buffer connection}, \\ \text{Full supply range} \end{array}$	_	0.25		Ω
		$      DRIVESTRENGTH = 0 \text{ or } 1, 0.4 \text{ V} \\ \leq \text{V}_{\text{OUT}} \leq \text{V}_{\text{OPA}} - 0.4 \text{ V}, -400 \mu\text{A} < \\ \text{I}_{\text{OUT}} < 400 \mu\text{A}, \text{Buffer connection,} \\ \text{Full supply range} $	_	0.6	_	Ω
		$ \begin{array}{l} DRIVESTRENGTH = 2 \text{ or } 3, 0.1 \text{ V} \\ \leq V_{OUT} \leq V_{OPA} - 0.1 \text{ V}, -2 \text{ mA} < \\ I_{OUT} < 2 \text{ mA}, \text{ Buffer connection}, \\ Full supply range \end{array} $		0.4	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V $\leq V_{OUT} \leq V_{OPA} - 0.1 V$ , -100 µA < $I_{OUT} < 100 µA$ , Buffer connection, Full supply range	_	1	_	Ω
Internal closed-loop gain	G <sub>CL</sub>	Buffer connection	TBD	1	TBD	-
		3x Gain connection	TBD	2.99	TBD	-
		16x Gain connection	TBD	15.7	TBD	-
Active current <sup>4</sup>	I <sub>OPA</sub>	DRIVESTRENGTH = 3, OUT- SCALE = 0	—	580	_	μA
		DRIVESTRENGTH = 2, OUT- SCALE = 0	_	176	_	μA
		DRIVESTRENGTH = 1, OUT- SCALE = 0	—	13	_	μA
		DRIVESTRENGTH = 0, OUT- SCALE = 0	_	4.7	_	μA

# Table 4.27. Operational Amplifier (OPAMP)

# **EBI Read Enable Timing Requirements**

Timing applies to both EBI\_REn and EBI\_NANDREn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

# Table 4.40. EBI Read Enable Timing Requirements

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Setup time, from EBI_AD	t <sub>SU_REn</sub>	IOVDD ≥ 1.62 V	55	—	—	ns
edge		IOVDD ≥ 3.0 V	36	—	—	ns
Hold time, from trailing EBI_REn edge to EBI_AD in- valid	t <sub>H_REn</sub>	IOVDD ≥ 1.62 V	-9	_	_	ns



Figure 4.7. EBI Read Enable Timing Requirements

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VBUS	A13	USB VBUS signal and auxiliary input to 5 V regulator.	PF11	A14	GPIO (5V)
PF10	A15	GPIO (5V)	PF0	A16	GPIO (5V)
PA0	B1	GPIO	PD11	B2	GPIO
PD10	B3	GPIO	PD9	B4	GPIO
PF9	B5	GPIO	PF8	B6	GPIO
PF7	B7	GPIO	PF6	B8	GPIO
PI11	B9	GPIO (5V)	PI8	B10	GPIO (5V)
PF5	B11	GPIO	PF13	B12	GPIO (5V)
PF3	B13	GPIO	PF2	B14	GPIO
PF1	B15	GPIO (5V)	VREGO	B16	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs
PA1	C1	GPIO	PD12	C2	GPIO
PD14	C3	GPIO (5V)	PD13	C4	GPIO (5V)
PI15	C5	GPIO (5V)	PI14	C6	GPIO (5V)
PI13	C7	GPIO (5V)	PI12	C8	GPIO (5V)
PI10	C9	GPIO (5V)	PI7	C10	GPIO (5V)
PF15	C11	GPIO (5V)	PF12	C12	GPIO
PF4	C13	GPIO	PC15	C14	GPIO (5V)
PC14	C15	GPIO (5V)	VREGI	C16	Input to 5 V regulator.
PA2	D1	GPIO	PG0	D2	GPIO (5V)
PD15	D3	GPIO (5V)	PC13	D14	GPIO (5V)
PC12	D15	GPIO (5V)	PC11	D16	GPIO (5V)
PA3	E1	GPIO	PG2	E2	GPIO (5V)
PG1	E3	GPIO (5V)	PC10	E14	GPIO (5V)
PC9	E15	GPIO (5V)	PC8	E16	GPIO (5V)
PA4	F1	GPIO	PG4	F2	GPIO (5V)
PG3	F3	GPIO (5V)	IOVDD2	F6 G6	Digital IO power supply 2.

PB2M3GPIOPB3M3GPIOPC6M1GPIOVRECVSM1value regulator VSSVREGWM4DCO regulator switching nodePB4N1GPIOPB5M2GPIOPD4M3GPIOPD5M1GPIOPD4M2GPIOPC0P1GPIO(SV)PA6P2GPIO(SV)PH1P5GPIO(SV)PH2P4GPIOPH2P1GPIO(SV)PH1P12GPIOPH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P14GPIO(SV)PH3P1GPIO(SV)PH1P14GPIO(SV)PH3P3GPIO(SV)PH1P14GPIO(SV)PH3P3GPIO(SV)PH1P14GPIO(SV)PH4P3GPIO(SV)PH2R2GPIO(SV)PH3P3GPIO(SV)PH3R4GPIO(SV)PH4S1GPIO(SV)GPICR2GPIO(SV)PS0R3GPIO(SV)GPISR4GPIO(SV)PS0R4GPIO(SV)GPISR4 <td< th=""><th>Pin Name</th><th>Pin(s)</th><th>Description</th><th>Pin Name</th><th>Pin(s)</th><th>Description</th></td<>	Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC6M14GPI0VREGVSM15Voltage regulator VSSVREGSWM16DCDC regulator switching nodePP84N1GPI0PB65N2GPI0PP80N3GPI0PD55N14GPI0PP10PP2GPI0PC0P1GPI0PP10PP2GPI0PC1P3GPI0PP10PP2GPI0PC2P3GPI0GPI0PP3GPI0PC1P4GPI0GPI0PP3GPI0PC2P3GPI0GPI0PP41GPI0PC3P3GPI0GPI0PP3GPI0PH3P16GPI0PP30PP3GPI0PH3P17GPI0GPI0PP40GPI0PH3P13GPI0PP10P11GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30R2GPI0PH3P13GPI0PP30R4GPI0P15R11GPI0GPI0PP30R4P16P13GPI0PP40P14GPI0P14P13GPI0PP40P14GPI0P14P13GPI0PP40P14GPI0P15R14GPI0GPI0P14GPI0P16P13GPI0GPI0P14<	PB2	M2	GPIO	PB3	M3	GPIO
VREGSWM14DCD regulator switching nodePB4N1CPI0PB5N2GPI0PPB6N3GPI0PD5N14GPI0PD4N15GPI0PC0P3GPI0 (5V)PA1PA2GPI0PA1P5GPI0PA3P6GPI0PA1P5GPI0PA3P6GPI0P14P7GPI0 (5V)PH12P8GPI0P14P1GPI0 (5V)PH13P10GPI0 (5V)P14P1GPI0 (5V)PH14P12GPI0 (5V)P14P13GPI0 (5V)PH10P12GPI0 (5V)P143P13GPI0 (5V)PH10P14GPI0 (5V)P143P14GPI0 (5V)PH10P14GPI0 (5V)P143P15GPI0 (5V)PD0P14GPI0 (5V)P15GPI0 (5V)PD0P14GPI0 (5V)P16R1GPI0 (5V)GPI0 (5V)Restingut active low. To apply an extractive low. To apply an extractina	PC6	M14	GPIO	VREGVSS	M15 N16	Voltage regulator VSS
PB5N2GPIOPB6N3GPIOPD5N14GPIOPD4N15GPIOPC0P1GPIO (5V)PC1P2GPIO (5V)PC1P3GPIO (5V)PA8P4GPIO (5V)PB9P7GPIO (5V)PB12P8GPIO (5V)PH8P1GPIO (5V)PH10P12GPIO (5V)PH3P13GPIO (5V)PD0PH10P12GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3SP15GPIO (5V)PD0P14GPIO (5V)PD3P15GPIO (5V)PD0PD0P14GPIO (5V)PD4R11GPIO (5V)PD0PA9R4GPIO (5V)PD5R3GPIO (5V)PA9R4GPIO (5V)PD6R7GPIO (5V)PH10R8GPIO (5V)PH4R1GPIO (5V)PH10R14GPIO (5V)PH4R13GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH10R14GPIO (5V)PH4R14GPIO (5V)PH10R14GPIO (5V)PH4R13GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH1R14	VREGSW	M16	DCDC regulator switching node	PB4	N1	GPIO
PD5N14GP0PD4N15GP10PC0P1GP10 (5V)PC1P2GP10 (5V)PC2P3GP10 (5V)PA8P4GP10 (5V)PB9P7GP10 (5V)PB12P8GP10 (5V)PH2P9GP10 (5V)PH11P12GP10 (5V)PH3P11GP10 (5V)PH11P12GP10 (5V)PH3P13GP10 (5V)PD0P14GP10 (5V)PH3P13GP10 (5V)PD0P14GP10 (5V)PH3P15GP10 (5V)PD0P14GP10 (5V)PB7R1GP10 (5V)PD0P14GP10 (5V)PB7R3GP10 - Controlled to failed to main extension may be of the single active tow. To apply an extend extension exten	PB5	N2	GPIO	PB6	N3	GPIO
PC0P1GPI0 (5V)PC1P2GPI0 (5V)PC2P3GPI0 (5V)PA8P4GPI0PA11P5GPI0 (5V)PA13P6GPI0 (5V)PB9P7GPI0 (5V)PB12P8GPI0 (5V)PH2P9GPI0 (5V)PH15P10GPI0 (5V)PH3P11GPI0 (5V)PH11P12GPI0 (5V)PH3P13GPI0 (5V)PH10P14GPI0 (5V)PH3P13GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0 (5V)PD0P14GPI0 (5V)PD3R1GPI0 (5V)PD3R2GPI0 (5V)PC5R3GPI0 (5V)PA9R4GPI0 (5V)PC5R3GPI0 (5V)PA9R4GPI0 (5V)BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to M20D.R68GPI0 (5V)PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH10R14GPI0 (5V)PH4R13GPI0 (5V)PH10R14GPI0 (5V)PH4R13GPI0 (5V)PH10R14GPI0 (5V)PH4R15GPI0 (5V)PA14T6GPI0PH4R13GPI0 (5V)PA14T6GPI0PH4R13GPI0 (5V)PA14T6GPI0 (5V)PH4T3GPI0 (5V) <td>PD5</td> <td>N14</td> <td>GPIO</td> <td>PD4</td> <td>N15</td> <td>GPIO</td>	PD5	N14	GPIO	PD4	N15	GPIO
PC2         P3         GPIO (5V)         PA8         P4         GPIO           PA11         P5         GPIO         PA13         P6         GPIO (5V)           PB9         P7         GPIO (5V)         PB12         P8         GPIO           PH2         P9         GPIO (5V)         PH5         P10         GPIO           PH3         P11         GPIO (5V)         PH11         P12         GPIO (5V)           PH3         P13         GPIO (5V)         PD0         P14         GPIO (5V)           PH3         P13         GPIO (5V)         PD0         P14         GPIO (5V)           PD3         P15         GPIO         PD3         P15         GPIO (5V)           PD3         P15         GPIO         PC3         R2         GPIO (5V)           PD5         R3         GPIO         PA9         R4         GPIO           BODEN         R5         Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.         RESETn         R6         GPIO (5V)           PB10         R7         GPIO (5V)         PH0         R8         GPIO (5V)           PH3         R9         GPIO (5V)         PH10         R1         GPIO	PC0	P1	GPIO (5V)	PC1	P2	GPIO (5V)
PA11         P5         GPIO         PA13         P6         GPIO (5V)           PB9         P7         GPIO (5V)         PB12         P8         GPIO           PH2         P9         GPIO (5V)         PH5         P10         GPIO           PH8         P11         GPIO (5V)         PH11         P12         GPIO (5V)           PH3         P13         GPIO (5V)         PD0         P14         GPIO (5V)           PD3         P15         GPIO (5V)         PD0         P14         GPIO (5V)           PD3         P15         GPIO         PD3         P15         GPIO         PD4           PB7         R1         GPIO         PC3         R2         GPIO (5V)           PC5         R3         GPIO         PA9         R4         GPIO           BODEN         R5         Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.         RESETn         R6         Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and left the internal pul-upensure that reset is released.           PB10         R7         GPIO (5V)         PH0         R8         GPIO (5V)           PH3         R9         GPIO (5V)         P	PC2	P3	GPIO (5V)	PA8	P4	GPIO
PB9P7GPIO (5V)PB12P8GPIOPH2P9GPIO (5V)PH5P10GPIOPH8P11GPIO (5V)PD11P12GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD2P23R2GPIO (5V)PB7R1GPIOPA9R4GPIOPC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin wyb be left disconnected or tied to AVDD.RESETNR6Reset input, active low. To apply an ex- terral reset source to this pin, it is re- arrest only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIOPH4R13GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PD7R16GPIOPH3T1GPIOPA10T4GPIOPH4T3GPIO (5V)PA14T6GPIOPH4T3GPIO (5V)PH11T8GPIO (5V)PH4T9GPIO (5V)PH1T10GPIOPH4T9GPIO (5V)PH7T10GPIOPH4T9GPIO (5V)PH3T12GPIOPH4T13GPIO (5V)PH3T12GPIOPH4T14GPIO (5V)PH3T14Anal	PA11	P5	GPIO	PA13	P6	GPIO (5V)
PH2P9GPI0 (5V)PH5P10GPI0PH8P11GPI0 (5V)PH11P12GPI0 (5V)PH3P13GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0PD0P14GPI0 (5V)PB7R1GPI0PC3R2GPI0 (5V)PC5R3GPI0PA9R4GPI0BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin out during reset, and let the internal pull-up ensure that reset is released.PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH6R10GPI0PH4R13GPI0 (5V)PH12R12GPI0 (5V)PH4R13GPI0 (5V)PH15R14GPI0 (5V)PH4R13GPI0 (5V)PD7R16GPI0PH3T1GPI0 (5V)PD7R16GPI0PH4T3GPI0 (5V)PA14T6GPI0PH4T3GPI0 (5V)PA14T6GPI0PH4T7GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T1GPI0 (5V)PB13T12GPI0PH4<	PB9	P7	GPIO (5V)	PB12	P8	GPIO
PH8P11GPIO (5V)PH11P12GPIO (5V)PH13P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD8P16GPIOPB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENRsBrown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETNR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and left the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIOPH4R13GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPA3T3GPIO (5V)PD7R16GPIOPH4T3GPIO (5V)PD7R16GPIOPH4T3GPIO (5V)PA14T6GPIOPH4T9GPIO (5V)PH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIOPH7 <t< td=""><td>PH2</td><td>P9</td><td>GPIO (5V)</td><td>PH5</td><td>P10</td><td>GPIO</td></t<>	PH2	P9	GPIO (5V)	PH5	P10	GPIO
PH13P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD8P16GPIOPB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPA7T3GPIO (5V)PA14T6GPIOPA12T5GPIO (5V)PA14T6GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH3T12GPIOPH4T9GPIO (5V)PH3T12GPIOPH4T13GPIOAVDDT14Analog power supply.PH4T15GPIO <td>PH8</td> <td>P11</td> <td>GPIO (5V)</td> <td>PH11</td> <td>P12</td> <td>GPIO (5V)</td>	PH8	P11	GPIO (5V)	PH11	P12	GPIO (5V)
PD3P15GPI0PD8P16GPI0PB7R1GPI0PC3R2GPI0 (5V)PC5R3GPI0PA9R4GPI0BC5R3GPI0PA9R4GPI0BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnReset input, active low. To apply an ex- ternal reset source to this pin, it is re- quied to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH6R10GPI0PH3R9GPI0 (5V)PH6R10GPI0 (5V)PH3R1GPI0 (5V)PH12R12GPI0 (5V)PH4R13GPI0 (5V)PH15R14GPI0 (5V)PD2R15GPI0 (5V)PD7R16GPI0PB8T1GPI0PA10T4GPI0PA12T5GPI0 (5V)PA14T6GPI0PA14T9GPI0 (5V)PH1T8GPI0 (5V)PH4T9GPI0 (5V)PB13T12GPI0PH4T13GPI0 (5V)PB13T12GPI0PB14T13GPI0AVDDT14Analog power supply.PB14T15GPI0PD6T16GPI0	PH13	P13	GPIO (5V)	PD0	P14	GPIO (5V)
PB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnReset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R13GPIO (5V)PH15R14GPIO (5V)PH14R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPA12T5GPIO (5V)PA14T6GPIOPH14T9GPIO (5V)PH1T10GPIO (5V)PH14T1GPIO (5V)PA14T6GPIOPH15T11GPIO (5V)PA14T6GPIOPH10T11GPIO (5V)PH1T10GPIO (5V)PH14T9GPIO (5V)PH3T12GPIOPH4T9GPIO (5V)PH3T12GPIOPH10T11GPIO (5V)PH3T12GPIOPH10T11GPIO (5V)PH3T14 </td <td>PD3</td> <td>P15</td> <td>GPIO</td> <td>PD8</td> <td>P16</td> <td>GPIO</td>	PD3	P15	GPIO	PD8	P16	GPIO
PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIO (5V)PH4R11GPIO (5V)PH6R10GPIO (5V)PH4R13GPIO (5V)PH12R12GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PD7R16GPIOPA7T3GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PH3T12GPIOPH4T13GPIO (5V)PH6T14Analog power supply.PH10T15GPIOPD6T16GPIO	PB7	R1	GPIO	PC3	R2	GPIO (5V)
BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- termal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensurePB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R1GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PD7R16GPIOPA12T5GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PB13T12GPIOPH10T11GPIO (5V)PB13T12GPIOPB14T13GPIO (5V)PD6T16GPIOPD1T15GPIOPD6T16GPIO	PC5	R3	GPIO	PA9	R4	GPIO
PB10         R7         GPIO (5V)         PH0         R8         GPIO (5V)           PH3         R9         GPIO (5V)         PH6         R10         GPIO           PH9         R11         GPIO (5V)         PH12         R12         GPIO (5V)           PH14         R13         GPIO (5V)         PH12         R14         GPIO (5V)           PD14         R13         GPIO (5V)         PH12         R14         GPIO (5V)           PD2         R15         GPIO (5V)         PD7         R16         GPIO           PD2         R15         GPIO (5V)         PD7         R16         GPIO           PB8         T1         GPIO (5V)         PD7         R16         GPIO           PB4         T3         GPIO (5V)         PC4         T2         GPIO           PA12         T5         GPIO (5V)         PA14         T6         GPIO           PB11         T7         GPIO (5V)         PH1         T8         GPIO (5V)           PH4         T9         GPIO (5V)         PH7         T10         GPIO (5V)           PH10         T11         GPIO (5V)         PB13         T12         GPIO           PB14	BODEN	R5	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	RESETn	R6	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PH3R9GPIO (5V)PH6R10GPIOPH9R11GPIO (5V)PH12R12GPIO (5V)PH14R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIO (5V)PB8T1GPIO (5V)PC4T2GPIOPA7T3GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PB10	R7	GPIO (5V)	PH0	R8	GPIO (5V)
PH9         R11         GPIO (5V)         PH12         R12         GPIO (5V)           PH14         R13         GPIO (5V)         PH15         R14         GPIO (5V)           PD2         R15         GPIO (5V)         PD7         R16         GPIO           PB8         T1         GPIO (5V)         PC4         T2         GPIO           PA7         T3         GPIO         PA10         T4         GPIO           PA12         T5         GPIO (5V)         PA10         T4         GPIO           PA12         T5         GPIO (5V)         PA14         T6         GPIO           PB11         T7         GPIO         PH1         T8         GPIO (5V)           PH10         T1         GPIO         PH1         T8         GPIO (5V)           PH4         T9         GPIO         PH7         T10         GPIO (5V)           PH10         T11         GPIO (5V)         PB13         T12         GPIO           PB14         T13         GPIO         AVDD         T14         Analog power supply.           PD1         T15         GPIO         PD6         T16         GPIO	PH3	R9	GPIO (5V)	PH6	R10	GPIO
PH14         R13         GPIO (5V)         PH15         R14         GPIO (5V)           PD2         R15         GPIO (5V)         PD7         R16         GPIO           PB8         T1         GPIO (5V)         PC4         T2         GPIO           PA7         T3         GPIO (5V)         PA10         T4         GPIO           PA12         T5         GPIO (5V)         PA14         T6         GPIO           PB11         T7         GPIO (5V)         PA14         T6         GPIO (5V)           PH44         T9         GPIO (5V)         PH1         T8         GPIO (5V)           PH4         T9         GPIO (5V)         PH7         T10         GPIO (5V)           PH10         T11         GPIO (5V)         PB13         T12         GPIO           PB14         T13         GPIO (5V)         PB13         T14         Analog power supply.           PD1         T15         GPIO         PD6         T16         GPIO	PH9	R11	GPIO (5V)	PH12	R12	GPIO (5V)
PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIOPC4T2GPIOPA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PH14	R13	GPIO (5V)	PH15	R14	GPIO (5V)
PB8T1GPIOPC4T2GPIOPA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PD2	R15	GPIO (5V)	PD7	R16	GPIO
PA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PB8	T1	GPIO	PC4	T2	GPIO
PA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PA7	Т3	GPIO	PA10	T4	GPIO
PB11         T7         GPIO         PH1         T8         GPIO (5V)           PH4         T9         GPIO         PH7         T10         GPIO (5V)           PH10         T11         GPIO (5V)         PB13         T12         GPIO           PB14         T13         GPIO         AVDD         T14         Analog power supply.           PD1         T15         GPIO         PD6         T16         GPIO	PA12	T5	GPIO (5V)	PA14	Т6	GPIO
PH4         T9         GPIO         PH7         T10         GPIO (5V)           PH10         T11         GPIO (5V)         PB13         T12         GPIO           PB14         T13         GPIO         AVDD         T14         Analog power supply.           PD1         T15         GPIO         PD6         T16         GPIO	PB11	T7	GPIO	PH1	Т8	GPIO (5V)
PH10         T11         GPIO (5V)         PB13         T12         GPIO           PB14         T13         GPIO         AVDD         T14         Analog power supply.           PD1         T15         GPIO         PD6         T16         GPIO	PH4	Т9	GPIO	PH7	T10	GPIO (5V)
PB14         T13         GPIO         AVDD         T14         Analog power supply.           PD1         T15         GPIO         PD6         T16         GPIO	PH10	T11	GPIO (5V)	PB13	T12	GPIO
PD1 T15 GPIO PD6 T16 GPIO	PB14	T13	GPIO	AVDD	T14	Analog power supply.
	PD1	T15	GPIO	PD6	T16	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.



# Figure 5.4. EFM32GG11B5xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.4. EFM32GG11B5xx in BGA120 Device Pino	ut
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF14	A9	GPIO (5V)	PF12	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs



# Figure 5.10. EFM32GG11B4xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.10. EFM32GG11B4xx in QFP100 Device Pino	ut
---	----

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO



# Figure 5.17. EFM32GG11B5xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description	
VSS	0	Ground	PA0	1	GPIO	
PA1	2	GPIO	PA2	3	GPIO	
PA3	4	GPIO	PA4	5	GPIO	
PA5	6	GPIO	PA6	7	GPIO	
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO	
PB4	10	GPIO	PB5	11	GPIO	

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description	
PB6	12	GPIO	PC4	13	GPIO	
PC5	14	GPIO	PB7	15	GPIO	
PB8	16	GPIO	PA12	17	GPIO (5V)	
PA13	18	GPIO (5V)	PA14	19	GPIO	
RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO	
PB12	22	GPIO	AVDD	23 27	Analog power supply.	
PB13	24	GPIO	PB14	25	GPIO	
PD0	28	GPIO (5V)	PD1	29	GPIO	
PD2	30	GPIO (5V)	PD3	31	GPIO	
PD4	32	GPIO	PD5	33	GPIO	
PD6	34	GPIO	PD7	35	GPIO	
PD8	36	GPIO	PC6	37	GPIO	
PC7	38	GPIO	DVDD	39	Digital power supply.	
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO	
PE5	42	GPIO	PE6	43	GPIO	
PE7	44	GPIO	VREGI	45	Input to 5 V regulator.	
VREGO	46	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs	PF10	47	GPIO (5V)	
PF11	48	GPIO (5V)	PF0	49	GPIO (5V)	
PF1	50	GPIO (5V)	PF2	51	GPIO	
VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	53	GPIO	
PF5	54	GPIO	PE8	56	GPIO	
PE9	57	GPIO	PE10	58	GPIO	
PE11	59	GPIO	PE12	60	GPIO	
PE13	61	GPIO	PE14	62	GPIO	
PE15	63	GPIO	PA15	64	GPIO	
Note:		·				

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCA	TION			
Functionality	0 - 3	4 - 7	Description		
PRS_CH7	0: PB13 1: PA7 2: PE7		Peripheral Reflex System PRS, channel 7.		
PRS_CH8	0: PA8 1: PA2 2: PE9		Peripheral Reflex System PRS, channel 8.		
PRS_CH9	0: PA9 1: PA3 2: PB10		Peripheral Reflex System PRS, channel 9.		
PRS_CH10	0: PA10 1: PC2 2: PD4		Peripheral Reflex System PRS, channel 10.		
PRS_CH11	0: PA11 1: PC3 2: PD5		Peripheral Reflex System PRS, channel 11.		
PRS_CH12	0: PA12 1: PB6 2: PD8		Peripheral Reflex System PRS, channel 12.		
PRS_CH13	0: PA13 1: PB9 2: PE14		Peripheral Reflex System PRS, channel 13.		
PRS_CH14	0: PA14 1: PC6 2: PE15		Peripheral Reflex System PRS, channel 14.		
PRS_CH15	0: PA15 1: PC7 2: PF0		Peripheral Reflex System PRS, channel 15.		
PRS_CH16	0: PA4 1: PB12 2: PE4		Peripheral Reflex System PRS, channel 16.		
PRS_CH17	0: PA5 1: PB15 2: PE5		Peripheral Reflex System PRS, channel 17.		
PRS_CH18	0: PB2 1: PC10 2: PC4		Peripheral Reflex System PRS, channel 18.		
PRS_CH19	0: PB3 1: PC11 2: PC5		Peripheral Reflex System PRS, channel 19.		

# 7.2 BGA152 PCB Land Pattern



Figure 7.2. BGA152 PCB Land Pattern Drawing

Dimension	Min	Тур	Мах		
A	-	-	1.30		
A1	0.55	0.60	0.65		
A2	0.21 BSC				
A3	0.30	0.35	0.40		
d	0.43	0.48	0.53		
D	10.00 BSC				
D1	8.00 BSC				
E	10.00 BSC				
E1	8.00 BSC				
e1	0.80 BSC				
e2	0.80 BSC				
L1	1.00 REF				
L2	1.00 REF				

# Table 9.1. BGA112 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 10.2 TQFP100 PCB Land Pattern



Figure 10.2. TQFP100 PCB Land Pattern Drawing

# 12. QFN64 Package Specifications

# 12.1 QFN64 Package Dimensions



Figure 12.1. QFN64 Package Drawing





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