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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E-XF

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	95
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	· ·
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b520f2048il120-a

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3.11 Memory Map

The EFM32GG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

	8xfq1qqqe]		
CM4 Peripherals	8xe88fffff			
	8×85555555			
QSPIO	0xcfffffff			
	8886666666			
EBI Region 3	8×855555555			
EBI Region 2	8×8844444	i \		
EBI Region 1	8×87555555			0xe0100000
EBI Region 0	8×83555555		CM4 ROM Table	0xe00ff000
5	8×7fffffff			0xe0042000
Bit Set	0x460f03ff		EIM	0xe0041000
(Peripherals / CRYPTO0)	0×46000000		TPIO	0xe0040000
	8×455f5455) `, F	System Control Space	0xe000f000
Bit Clear (Paripherals / CRXPTOD)	0x440f03ff		b)stern control opace	0xe000e000
(Feripherals / CKTF100)	0x44000000 0x43ffffff		FPB	0xe0003000
Pit Pand	0x43e40000 0x43e3ffff		DWT	0xe0002000
(Peripherals / CRYPTO0 / SDIO)	0×42000000		ITM	0xe0001000
	8×41146666	1 -		0xe0000000
USB	8×48136666	1 _		
	8×488‡£555	1 /-	DAMO	0x10080000
SDIO	8×488f1666	1 /	(code space)	0100.40000
	8×488f8455		RAM1	0X10040000
CRYPT00	8×488‡8355	1 / -	(code space)	0x10020000
Peripherals 1	8×48825555		(code space)	0
Peripherals 0	8×48834444			0x10000000 0x0fe09000
	8×36666666	1 / F	Chip config	0x0fe08000
SRAM (bit-band)	8×355555555		Lock bits	0x0fe05000
	8×21ffffff			0x0fe04000
RAM2 (data space)	8×28871111		User Data	0x0fe00000
RAM1 (data space)	8×2883ffff		QSPI0	0x0c000000
BAMO (data space)	0x20020000 0x2001ffff	1/		0x04000000 0x00200000
(data space)	0x1ffffff	ł –		0.00200000
Code			F l ash (2048 KB)	
	0×000000000			0×00000000
				- 0.000000000

Figure 3.2. EFM32GG11 Memory Map — Core Peripherals and Code Space

4.1.7.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.8.	Current Co	nsumption 3.3	V using	DC-DC	Converter
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Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_DCM	72 MHz HFRCO, CPU running Prime from flash	_	80	—	µA/MHz
DCM mode ²		72 MHz HFRCO, CPU running while loop from flash	—	80	_	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	92		µA/MHz
		50 MHz crystal, CPU running while loop from flash	_	84		µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	84		µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	90		µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	_	94		µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	_	109		µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	_	698		µA/MHz
Current consumption in EM0 mode with all peripherals dis-	I _{ACTIVE_CCM}	72 MHz HFRCO, CPU running Prime from flash	_	84		µA/MHz
CCM mode ¹		72 MHz HFRCO, CPU running while loop from flash	—	84		µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	_	95		µA/MHz
		50 MHz crystal, CPU running while loop from flash	_	91		µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	92		µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	_	104		µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	113	_	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	_	142	_	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1264		µA/MHz

4.1.9 Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
DVDD BOD threshold	V _{DVDDBOD}	DVDD rising	_	—	1.62	V
		DVDD falling (EM0/EM1)	1.35	—	—	V
		DVDD falling (EM2/EM3)	TBD	—	_	V
DVDD BOD hysteresis	V _{DVDDBOD_HYST}		_	18	—	mV
DVDD BOD response time	t _{DVDDBOD_DELAY}	Supply drops at 0.1V/µs rate	_	2.4	—	μs
AVDD BOD threshold	V _{AVDDBOD}	AVDD rising	_	_	1.8	V
		AVDD falling (EM0/EM1)	1.62	—	_	V
		AVDD falling (EM2/EM3)	TBD	—	—	V
AVDD BOD hysteresis	V _{AVDDBOD_HYST}			20	_	mV
AVDD BOD response time	t _{AVDDBOD_DELAY}	Supply drops at 0.1V/µs rate	—	2.4	—	μs
EM4 BOD threshold	V _{EM4DBOD}	AVDD rising	_	_	1.7	V
		AVDD falling	1.45	_	—	V
EM4 BOD hysteresis	V _{EM4BOD_HYST}		_	25	_	mV
EM4 BOD response time	t _{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	_	300	—	μs

Table 4.11. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Signal to noise and distortion ratio (1 kHz sine wave),	SNDR _{DAC}	500 ksps, single-ended, internal 1.25V reference	—	60.4	_	dB
KHz		500 ksps, single-ended, internal 2.5V reference	—	61.6		dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	_	dB
		500 ksps, differential, internal 1.25V reference		63.3		dB
		500 ksps, differential, internal 2.5V reference	_	64.4	_	dB
		500 ksps, differential, 3.3V VDD reference	_	65.8		dB
Signal to noise and distortion ratio (1 kHz sine wave),	SNDR _{DAC_BAND}	500 ksps, single-ended, internal 1.25V reference	—	65.3	_	dB
Noise band limited to 22 kHz		500 ksps, single-ended, internal 2.5V reference	—	66.7	_	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	_	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	_	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	_	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0		dB
Total harmonic distortion	THD		—	70.2	_	dB
Differential non-linearity ³	DNL _{DAC}		TBD	_	TBD	LSB
Intergral non-linearity	INL _{DAC}		TBD	_	TBD	LSB
Offset error ⁵	V _{OFFSET}	T = 25 °C	TBD	_	TBD	mV
		Across operating temperature range	TBD	—	TBD	mV
Gain error ⁵	V _{GAIN}	T = 25 °C, Low-noise internal ref- erence (REFSEL = 1V25LN or 2V5LN)	TBD	_	TBD	%
		Across operating temperature range, Low-noise internal refer- ence (REFSEL = 1V25LN or 2V5LN)	TBD		TBD	%
External load capactiance, OUTSCALE=0	C _{LOAD}		—	_	75	pF

4.1.18 Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Single conversion time (1x	t _{CNV}	12-bit SAR Conversions		20.2	—	μs
accumulation)		16-bit SAR Conversions	—	26.4	_	μs
		Delta Modulation Conversion (sin- gle comparison)		1.55		μs
Maximum external capacitive load	C _{EXTMAX}	CS0CG=7 (Gain = 1x), including routing parasitics	—	68	—	pF
		CS0CG=0 (Gain = 10x), including routing parasitics	_	680	_	pF
Maximum external series impedance	R _{EXTMAX}			1		kΩ
Supply current, EM2 bonded conversions, WARMUP- MODE=NORMAL, WAR- MUPCNT=0	I _{CSEN_BOND}	12-bit SAR conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	_	326	_	nA
		Delta Modulation conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹	_	226	_	nA
		12-bit SAR conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF) ¹		33	_	nA
		Delta Modulation conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 chan- nels bonded (total capacitance of 330 pF) ¹	_	25	_	nA
Supply current, EM2 scan conversions, WARMUP- MODE=NORMAL, WAR-	ICSEN_EM2	12-bit SAR conversions, 20 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan ¹	_	690	_	nA
MUPCNT=0		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 sam- ples per scan ¹		515		nA
		12-bit SAR conversions, 200 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan ¹	_	79	_	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan ¹		57	_	nA

Table 4.26. Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Supply current, continuous conversions, WARMUP- MODE=KEEPCSENWARM	ICSEN_ACTIVE	SAR or Delta Modulation conver- sions of 33 pF capacitor, CS0CG=0 (Gain = 10x), always on		90.5		μA
HFPERCLK supply current	ICSEN_HFPERCLK	Current contribution from HFPERCLK when clock to CSEN block is enabled.	_	2.25	_	µA/MHz

Note:

 Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).





Figure 4.14. SDIO HS Mode Timing



Figure 4.24. EM0 Active Mode Typical Supply Current vs. Temperature



Figure 4.27. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description			
Note:								
1. GPIO with 5V tolerance are indicated by (5V).								
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hard- ware compatibility, do not use these pins with 5V domains.								



Figure 5.4. EFM32GG11B5xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.4. EFM32GG11B5xx in BGA120 Device Pino	ut
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF14	A9	GPIO (5V)	PF12	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs

5.20 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 5.21 Alternate Functionality Overview for a list of GPIO locations available for each function.

GPIO Name	Pin Alternate Functionality / Description						
	Analog	EBI	Timers	Communication	Other		
PA15	BUSAY BUSBX LCD_SEG12	EBI_AD08 #0	TIM3_CC2 #0	ETH_MIIRXCLK #0 ETH_MDIO #3 US2_CLK #3	PRS_CH15 #0		
PE15	BUSCY BUSDX LCD_SEG11	EBI_AD07 #0	TIM2_CDTI2 #2 TIM3_CC1 #0	ETH_RMIITXD0 #0 ETH_MIIRXD3 #0 SDIO_CMD #1 US0_RTS #0 QSPI0_DQS #1 LEU0_RX #2	PRS_CH14 #2 ETM_TD3 #4		
PE14	BUSDY BUSCX LCD_SEG10	EBI_AD06 #0	TIM2_CDTI1 #2 TIM3_CC0 #0	ETH_RMIITXD1 #0 ETH_MIIRXD2 #0 SDIO_CLK #1 US0_CTS #0 QSPI0_SCLK #1 LEU0_TX #2	PRS_CH13 #2 ETM_TD2 #4		
PE13	BUSCY BUSDX LCD_SEG9	EBI_AD05 #0	TIM1_CC3 #1 TIM2_CC2 #3 LE- TIM0_OUT1 #4	SDIO_CLK #0 ETH_MIIRXD1 #0 US0_TX #3 US0_CS #0 U1_RX #4 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 ETM_TD1 #4 GPIO_EM4WU5		
PE12	BUSDY BUSCX LCD_SEG8	EBI_AD04 #0	TIM1_CC2 #1 TIM2_CC1 #3 WTIM0_CDTI2 #0 LETIM0_OUT0 #4	SDIO_CMD #0 ETH_MIIRXD0 #0 US0_RX #3 US0_CLK #0 U1_TX #4 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_ALTEX6 PRS_CH1 #3 ETM_TD0 #4		
PE11	BUSCY BUSDX LCD_SEG7	EBI_AD03 #0 EBI_CS3 #4	TIM1_CC1 #1 TIM4_CC2 #7 WTIM0_CDTI1 #0	SDIO_DAT0 #0 QSPI0_DQ7 #0 ETH_MIIRXDV #0 US0_RX #0	LES_ALTEX5 PRS_CH3 #2 ETM_TCLK #4		
PE10	BUSDY BUSCX LCD_SEG6	EBI_AD02 #0 EBI_CS2 #4	TIM1_CC0 #1 TIM4_CC1 #7 WTIM0_CDTI0 #0	SDIO_DAT1 #0 QSPI0_DQ6 #0 ETH_MIIRXER #0 US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9		
PE9	BUSCY BUSDX LCD_SEG5	EBI_AD01 #0 EBI_CS1 #4	TIM4_CC0 #7 PCNT2_S1IN #1	SDIO_DAT2 #0 QSPI0_DQ5 #0 US5_RX #0	PRS_CH8 #2		
PE8	BUSDY BUSCX LCD_SEG4	EBI_AD00 #0 EBI_CS0 #4	TIM2_CDTI0 #2 TIM4_CC2 #6 PCNT2_S0IN #1	SDIO_DAT3 #0 QSPI0_DQ4 #0 US5_TX #0 I2C2_SDA #0	PRS_CH3 #1		
PI9		EBI_A14 #2	TIM1_CC3 #7 TIM4_CC1 #3	US4_CS #3			
PI6		EBI_A11 #2	TIM1_CC0 #7 TIM4_CC1 #2 WTIM3_CC0 #5	US4_TX #3			

Table 5.20. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD15		EBI_NANDREn #1	TIM2_CDTI2 #1 TIM3_CC0 #7 WTIM0_CDTI0 #1 PCNT1_S0IN #2	ETH_TSUEXTCLK #1 CAN0_TX #5 US5_CTS #1 I2C0_SCL #3	
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSACMP1Y BU- SACMP1X	EBI_ARDY #4	TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 TIM5_CC2 #5 WTIM3_CC2 #2 PCNT0_S0IN #0 PCNT2_S1IN #4	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3 U1_RX #0 I2C2_SCL #6	LES_CH13 PRS_CH21 #1 ACMP3_O #3
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSACMP1Y BU- SACMP1X		TIM1_CC3 #0 TIM5_CC1 #5 WTIM3_CC1 #2 PCNT2_S0IN #4	CAN1_RX #4 US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3 U1_TX #0 I2C2_SDA #6	CMU_CLK0 #1 LES_CH12 PRS_CH20 #1
PC11	BUSACMP1Y BU- SACMP1X	EBI_ALE #4 EBI_ALE #5 EBI_A23 #1	TIM5_CC0 #5 WTIM3_CC0 #2	CAN1_TX #4 US0_TX #2 I2C1_SDA #4	LES_CH11 PRS_CH19#1
PA3	BUSAY BUSBX LCD_SEG16	EBI_AD12 #0 EBI_VSNC #3	TIM0_CDTI0 #0 TIM3_CC0 #5	ETH_RMIIREFCLK #0 ETH_MIITXD1 #0 SDIO_DAT3 #1 US3_CS #0 U0_TX #2 QSPI0_DQ1 #1	CMU_CLK2 #1 CMU_CLK10 #1 CMU_CLK2 #4 LES_ALTEX2 PRS_CH9 #1 ETM_TD1 #3
PG2	BUSACMP2Y BU- SACMP2X	EBI_AD02 #2	TIM6_CC2 #0 TIM2_CDTI2 #3 WTIM0_CC0 #2 LE- TIM1_OUT0 #7	ETH_MIITXD2 #1 US3_CLK #4 QSPI0_DQ1 #2	CMU_CLK0 #3
PG1	BUSACMP2Y BU- SACMP2X	EBI_AD01 #2	TIM6_CC1 #0 TIM2_CDTI1 #3 WTIM0_CDTI2 #1 LETIM1_OUT1 #6	ETH_MIITXD3 #1 US3_RX #4 QSPI0_DQ0 #2	CMU_CLK1 #3
PC10	BUSACMP1Y BU- SACMP1X	EBI_A10 #2 EBI_A22 #1	TIM2_CC2 #2 TIM5_CC2 #4 WTIM3_CC2 #1	CAN1_TX #3 US0_RX #2	LES_CH10 PRS_CH18 #1
PC9	BUSACMP1Y BU- SACMP1X	EBI_A09 #2 EBI_A21 #1 EBI_A27 #3	TIM2_CC1 #2 TIM5_CC1 #4 WTIM3_CC1 #1	CAN1_RX #3 US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2
PC8	BUSACMP1Y BU- SACMP1X	EBI_A08 #2 EBI_A15 #0 EBI_A20 #1 EBI_A26 #3	TIM2_CC0 #2 TIM5_CC0 #4 WTIM3_CC0 #1	US0_CS #2	LES_CH8 PRS_CH4 #0
PA4	BUSBY BUSAX LCD_SEG17	EBI_AD13 #0 EBI_HSNC #3	TIM0_CDTI1 #0 TIM3_CC1 #5	ETH_RMIICRSDV #0 ETH_MIITXD0 #0 SDIO_DAT4 #1 US3_CTS #0 U0_RX #2 QSPI0_DQ2 #1	LES_ALTEX3 PRS_CH16 #0 ETM_TD2 #3
PG4	BUSACMP2Y BU- SACMP2X	EBI_AD04 #2	TIM6_CDTI1 #0 WTIM0_CC2 #2	ETH_MIITXD0 #1 US3_CTS #4 QSPI0_DQ3 #2	

GPIO Name	Pin Alternate Functionality / Description					
	Analog	EBI	Timers	Communication	Other	
PD4	BUSADC0Y BU- SADC0X OPA2_P	EBI_A08 #1 EBI_A17 #3	TIM6_CC0 #7 WTIM0_CDTI0 #4 WTIM1_CC2 #1 WTIM2_CC1 #5	CAN1_TX #2 US1_CTS #1 US3_CLK #2 LEU0_TX #0 I2C1_SDA #3	CMU_CLKI0 #0 PRS_CH10 #2 ETM_TD2 #0 ETM_TD2 #2	
PC0	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSACMP0Y BU- SACMP0X	EBI_AD07 #1 EBI_CS0 #2 EBI_REn #3 EBI_A23 #0	TIM0_CC1 #3 TIM2_CC1 #4 PCNT0_S0IN #2	ETH_MDIO #2 CAN0_RX #0 US0_TX #5 US1_TX #0 US1_CS #4 US2_RTS #0 US3_CS #3 I2C0_SDA #4	LES_CH0 PRS_CH2 #0	
PC1	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSACMP0Y BU- SACMP0X	EBI_AD08 #1 EBI_CS1 #2 EBI_BL0 #3 EBI_A24 #0	TIM0_CC2 #3 TIM2_CC2 #4 WTIM0_CC0 #7 PCNT0_S1IN #2	ETH_MDC #2 CAN0_TX #0 US0_RX #5 US1_TX #4 US1_RX #0 US2_CTS #0 US3_RTS #1 I2C0_SCL #4	LES_CH1 PRS_CH3 #0	
PC2	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSACMP0Y BU- SACMP0X	EBI_AD09 #1 EBI_CS2 #2 EBI_NANDWEn #3 EBI_A25 #0	TIM0_CDTI0 #3 TIM2_CC0 #5 WTIM0_CC1 #7 LE- TIM1_OUT0 #3	ETH_TSUEXTCLK #2 CAN1_RX #0 US1_RX #4 US2_TX #0	LES_CH2 PRS_CH10 #1	
PA8	BUSBY BUSAX LCD_SEG36	EBI_AD14 #1 EBI_A02 #3 EBI_DCLK #0	TIM2_CC0 #0 TIM0_CC0 #6 LE- TIM0_OUT0 #6 PCNT1_S1IN #4	US2_RX #2 US4_RTS #0	PRS_CH8 #0	
PA11	BUSAY BUSBX LCD_SEG39	EBI_CS1 #1 EBI_A05 #3 EBI_HSNC #0	WTIM2_CC2 #0 LE- TIM1_OUT0 #1	US2_CTS #2	PRS_CH11 #0	
PA13	BUSAY BUSBX	EBI_WEn #1 EBI_NANDWEn #2 EBI_A01 #0 EBI_A07 #3	TIM0_CC2 #7 TIM2_CC1 #1 WTIM0_CDTI1 #2 WTIM2_CC1 #1 LE- TIM1_OUT1 #1 PCNT1_S1IN #5	CAN1_TX #5 US0_CS #5 US2_TX #3	PRS_CH13 #0	
PB9	BUSAY BUSBX	EBI_ALE #1 EBI_NANDREn #2 EBI_A00 #1 EBI_A03 #0 EBI_A09 #3	WTIM2_CC0 #2 LE- TIM0_OUT0 #7	SDIO_WP #3 CAN0_RX #3 US1_CTS #0 U1_TX #2	PRS_CH13 #1 ACMP1_O #5	
PB12	BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT	EBI_A03 #1 EBI_A12 #3 EBI_CSTFT #2	TIM1_CC3 #3 WTIM2_CC0 #3 LE- TIM0_OUT1 #1 PCNT0_S0IN #7 PCNT1_S1IN #6	US2_CTS #1 US5_RTS #0 U1_RTS #2 I2C1_SCL #1	PRS_CH16 #1	
PH2	BUSADC1Y BU- SADC1X	EBI_VSNC #2	TIM6_CC0 #3	US1_CTS #6		
PH5	BUSADC1Y BU- SADC1X	EBI_A17 #2	TIM6_CDTI0 #3 WTIM2_CC1 #6	US4_RX #4		
PH8	BUSACMP3Y BU- SACMP3X	EBI_A20 #2	TIM6_CC0 #4 WTIM1_CC0 #6 WTIM2_CC1 #7	US4_CTS #4		

Alternate	LOC	ATION		
Functionality	0 - 3	4 - 7	Description	
BU_STAT	0: PE3		Backup Power Domain status, whether or not the system is in backup mode.	
BU_VIN	0: PD8		Battery input for Backup Power Domain.	
BU_VOUT	0: PE2		Power output for Backup Power Domain.	
CAN0_RX	0: PC0 1: PF0 2: PD0 3: PB9	4: PG8 5: PD14 6: PE0 7: PI12	CAN0 RX.	
CAN0_TX	0: PC1 1: PF2 2: PD1 3: PB10	4: PG9 5: PD15 6: PE1 7: PI13	CAN0 TX.	
CAN1_RX	0: PC2 1: PF1 2: PD3 3: PC9	4: PC12 5: PA12 6: PG10 7: PI14	CAN1 RX.	
CAN1_TX	0: PC3 1: PF3 2: PD4 3: PC10	4: PC11 5: PA13 6: PG11 7: PI15	CAN1 TX.	
CMU_CLK0	0: PA2 1: PC12 2: PD7 3: PG2	4: PF2 5: PA12	Clock Management Unit, clock output number 0.	
CMU_CLK1	0: PA1 1: PD8 2: PE12 3: PG1	4: PF3 5: PB11	Clock Management Unit, clock output number 1.	
CMU_CLK2	0: PA0 1: PA3 2: PD6 3: PG0	4: PA3 5: PD10	Clock Management Unit, clock output number 2.	
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	4: PE1 5: PD10 6: PE12 7: PB11	Clock Management Unit, clock input number 0.	
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.	
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.	

Alternate	LOCA		
Functionality	0 - 3	4 - 7	Description
ETH_MIITXD2	0: PA2 1: PG2		Ethernet MII Transmit Data Bit 2.
ETH_MIITXD3	0: PA1 1: PG1		Ethernet MII Transmit Data Bit 3.
ETH_MIITXEN	0: PA5 1: PG5		Ethernet MII Transmit Enable.
ETH_MIITXER	0: PA6 1: PG6		Ethernet MII Transmit Error.
ETH_RMIICRSDV	0: PA4 1: PD11		Ethernet RMII Carrier Sense / Data Valid.
ETH_RMIIREFCLK	0: PA3 1: PD10		Ethernet RMII Reference Clock.
ETH_RMIIRXD0	0: PA2 1: PD9		Ethernet RMII Receive Data Bit 0.
ETH_RMIIRXD1	0: PA1 1: PF9		Ethernet RMII Receive Data Bit 1.
ETH_RMIIRXER	0: PA5 1: PD12		Ethernet RMII Receive Error.
ETH_RMIITXD0	0: PE15 1: PF7		Ethernet RMII Transmit Data Bit 0.
ETH_RMIITXD1	0: PE14 1: PF6		Ethernet RMII Transmit Data Bit 1.
ETH_RMIITXEN	0: PA0 1: PF8		Ethernet RMII Transmit Enable.
ETH_TSUEXTCLK	0: PB5 1: PD15 2: PC2 3: PF8		Ethernet IEEE1588 External Reference Clock.

7.2 BGA152 PCB Land Pattern



Figure 7.2. BGA152 PCB Land Pattern Drawing

Table 7.2. BGA152 PCB Land Pattern Dimensions

Dimension	Min	Nom	Мах	
X	0.20			
C1	6.50			
C2	6.50			
E1	0.5			
E2	0.5			

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.

3. This Land Pattern Design is based on the IPC-7351 guidelines.

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

6. The stencil thickness should be 0.125 mm (5 mils).

7. The ratio of stencil aperture to land pad size should be 1:1.

8. A No-Clean, Type-3 solder paste is recommended.

9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.



Figure 8.3. BGA120 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.

Table 10.2. TQFP100 PCB Land Pattern Dimensions

Dimension	Min	Nom	Мах		
C1	15.4				
C2	15.4				
E	0.50 BSC				
X	0.30				
Y	1.50				

Note:

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. This Land Pattern Design is based on the IPC-7351 guidelines.
- 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
- 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 5. The stencil thickness should be 0.125 mm (5 mils).
- 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
- 7. A No-Clean, Type-3 solder paste is recommended.
- 8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10.3 TQFP100 Package Marking



Figure 10.3. TQFP100 Package Marking

The package marking consists of:

- PPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- · WW The 2-digit workweek when the device was assembled.