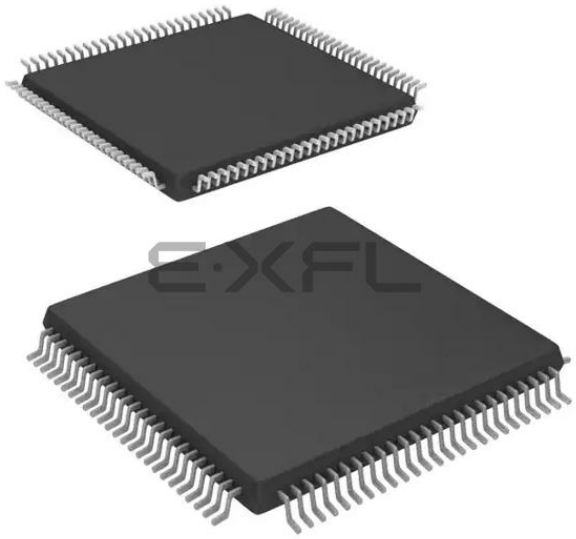
Silicon Labs - EFM32GG11B520F2048IQ100-A Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b520f2048iq100-a

1. Feature List

The EFM32GG11 highlighted features are listed below.

- **ARM Cortex-M4 CPU platform**
  - High performance 32-bit processor @ up to 72 MHz
  - DSP instruction support and Floating Point Unit
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 80 µA/MHz in Active Mode (EM0)
  - 2.1 µA EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Up to 2048 kB flash program memory**
  - Dual-bank with read-while-write support
- **Up to 512 kB RAM data memory**
  - 256 kB with ECC (SEC-DED)
- **Octal/Quad-SPI Flash Memory Interface**
  - Supports 3 V and 1.8 V memories
  - 1/2/4/8-bit data bus
  - Quad-SPI Execute In Place (XIP)
- **Communication Interfaces**
  - Low-energy Universal Serial Bus (USB) with Device and Host support
    - Fully USB 2.0 compliant
    - On-chip PHY and embedded 5V to 3.3V regulator
    - Crystal-free Device mode operation
    - Patent-pending Low-Energy Mode (LEM)
  - SD/MMC/SDIO Host Controller
    - SD v3.01, SDIO v3.0 and MMC v4.51
    - 1/4/8-bit bus width
  - 10/100 Ethernet MAC with MII/RMII interface
    - IEEE1588-2008 precision time stamping
    - Energy Efficient Ethernet (802.3az)
  - Up to 2× CAN Bus Controller
    - Version 2.0A and 2.0B up to 1 Mbps
  - 6× Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
    - Triple buffered full/half-duplex operation with flow control
    - Ultra high speed (36 MHz) operation on one instance
  - 2× Universal Asynchronous Receiver/ Transmitter
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 3× I^2C Interface with SMBus support
    - Address recognition in EM3 Stop Mode
- **Up to 144 General Purpose I/O Pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 5 V tolerance on select pins
  - Asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **Up to 24 Channel DMA Controller**
- **Up to 24 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **External Bus Interface for up to 4x256 MB of external memory mapped space**
  - TFT Controller with Direct Drive
  - Per-pixel alpha-blending engine
- **Hardware Cryptography**
  - AES 128/256-bit keys
  - ECC B/K163, B/K233, P192, P224, P256
  - SHA-1 and SHA-2 (SHA-224 and SHA-256)
  - True Random Number Generator (TRNG)
- **Hardware CRC engine**
  - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
  - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8×36 segments**
  - Voltage boost, contrast and autonomous animation
  - Patented low-energy LCD driver
- **Backup Power Domain**
  - RTCC and retention registers in a separate power domain, available down to energy mode EM4H
  - Operation from backup battery when main power absent/ insufficient
- **Ultra Low-Power Precision Analog Peripherals**
  - 2× 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
    - On-chip temperature sensor
  - 2× 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
  - Digital to Analog Current Converter (IDAC)
  - Up to 4× Analog Comparator (ACMP)
  - Up to 4× Operational Amplifier (OPAMP)
  - Robust current-based capacitive sensing with up to 64 inputs and wake-on-touch (CSEN)
  - Up to 108 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
  - Supply Voltage Monitor

4.1.10 Oscillators

4.1.10.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.12. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}		6	—	18	pF
On-chip tuning cap range [2]	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup [3]	I_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2, AGC[4] = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{LFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

4.1.12 General-Purpose I/O (GPIO)

Table 4.20. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	IOVDD*0.3	V
Input high voltage	V_{IH}	GPIO pins	IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C	—	—	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T > 85 °C	—	—	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	TBD	µA
I/O pin pull-up/pull-down resistor	R_{PUD}		TBD	40	TBD	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		15	25	35	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current, continuous conversions, WARMUP-MODE=KEEPCSENWARM	I_{CSEN_ACTIVE}	SAR or Delta Modulation conversions of 33 pF capacitor, CS0CG=0 (Gain = 10x), always on	—	90.5	—	µA
HFPERCLK supply current	$I_{CSEN\_HFPERCLK}$	Current contribution from HFPERCLK when clock to CSEN block is enabled.	—	2.25	—	µA/MHz

Note:

1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

EBI TFT Output Timing

All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.39. EBI TFT Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, EBI_DCLK to EBI_AD invalid	t_{OH_DCLK}	IOVDD ≥ 1.62 V	-23 + (TFTHOLD * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-12 + (TFTHOLD * $t_{HFCORECLK}$)	—	—	ns
Output setup time, EBI_AD valid to EBI_DCLK	t_{OSU_DCLK}	IOVDD ≥ 1.62 V	-11 + (TFTSETUP * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-9 + (TFTSETUP * $t_{HFCORECLK}$)	—	—	ns

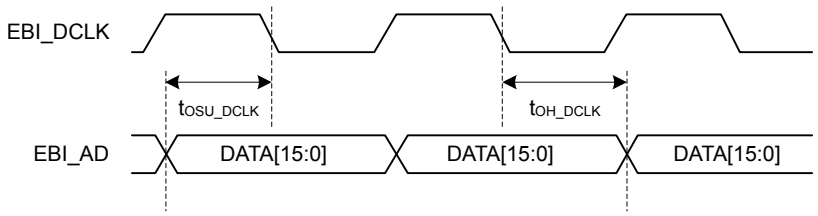

Figure 4.6. EBI TFT Output Timing

SDIO MMC DDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Table 4.53. SDIO MMC DDR Mode Timing (Location 0, 3V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.13	2.37	—	ns
Clock fall time	t_F		1.01	2.02	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		3	—	—	ns
Input setup time, DAT[0:7] valid to SD_CLK	t_{ISU2X}		5.3	—	—	ns
Input hold time, SD_CLK to DAT[0:7] change	t_{IH2X}		2.5	—	—	ns
Output delay time, SD_CLK to DAT[0:7] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:7] change	t_{OH2X}		3	—	—	ns

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PG6	H1	GPIO (5V)	PG7	H2	GPIO (5V)
PG5	H3	GPIO (5V)	PE6	H12	GPIO
PE5	H13	GPIO	DVDD	H14	Digital power supply.
PG9	J1	GPIO (5V)	PG10	J2	GPIO (5V)
PG8	J3	GPIO (5V)	PE3	J12	GPIO
PE4	J13	GPIO	VREGVDD	J14	Voltage regulator VDD input
PG12	K1	GPIO	PG13	K2	GPIO
PG11	K3	GPIO (5V)	PE2	K12	GPIO
PE1	K13	GPIO (5V)	VREGSW	K14	DCDC regulator switching node
PG15	L1	GPIO (5V)	PB15	L2	GPIO (5V)
PG14	L3	GPIO	PC7	L12	GPIO
PE0	L13	GPIO (5V)	VREGVSS	L14	Voltage regulator VSS
PB0	M1	GPIO	PB1	M2	GPIO
PB4	M3	GPIO	PC0	M4	GPIO (5V)
PC3	M5	GPIO (5V)	PA9	M6	GPIO
BODEN	M7	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	PA12	M8	GPIO (5V)
RESETn	M9	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB10	M10	GPIO (5V)
PD1	M11	GPIO	PC6	M12	GPIO
PD5	M13	GPIO	PD8	M14	GPIO
PB7	N1	GPIO	PB2	N2	GPIO
PB5	N3	GPIO	PC2	N4	GPIO (5V)
PC5	N5	GPIO	PA8	N6	GPIO
PA11	N7	GPIO	PA14	N8	GPIO
PB11	N9	GPIO	PB12	N10	GPIO
PD0	N11	GPIO (5V)	PD2	N12	GPIO (5V)
PD4	N13	GPIO	PD7	N14	GPIO
PB8	P1	GPIO	PB3	P2	GPIO
PB6	P3	GPIO	PC1	P4	GPIO (5V)
PC4	P5	GPIO	PA7	P6	GPIO
PA10	P7	GPIO	PA13	P8	GPIO (5V)
PB9	P9	GPIO (5V)	PB13	P10	GPIO
PB14	P11	GPIO	AVDD	P12	Analog power supply.
PD3	P13	GPIO	PD6	P14	GPIO

5.10 EFM32GG11B4xx in QFP100 Device Pinout

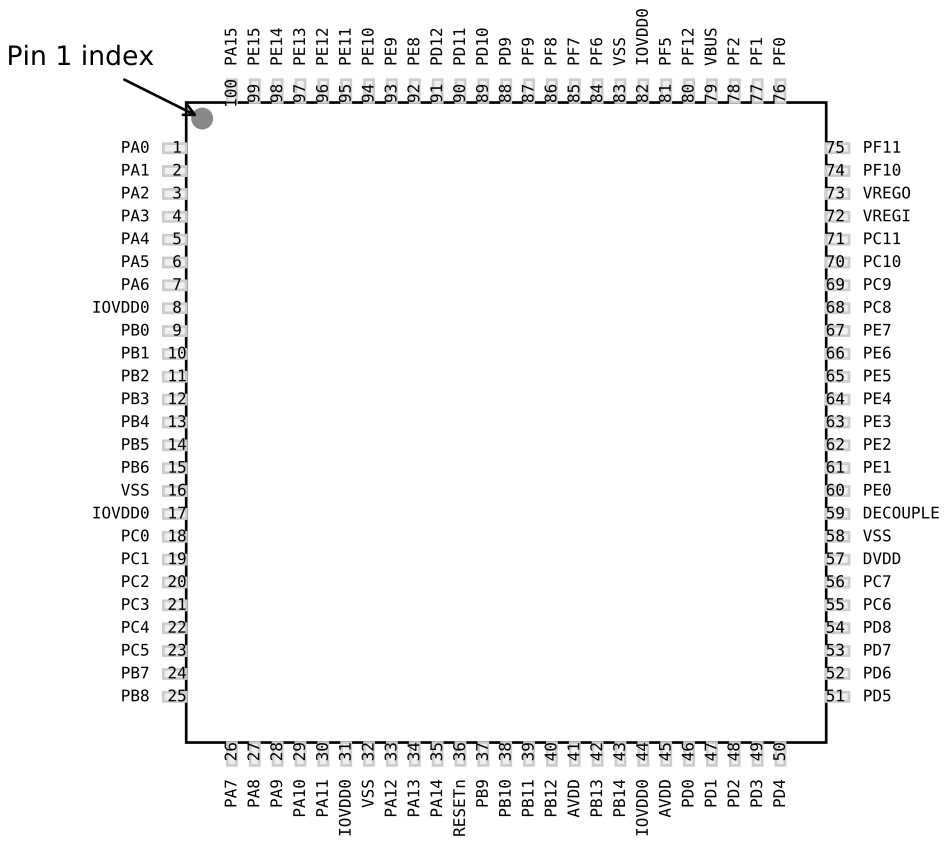

Figure 5.10. EFM32GG11B4xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.10. EFM32GG11B4xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA12	18	GPIO (5V)	PA13	19	GPIO (5V)
PA14	20	GPIO	RESETn	21	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	22	GPIO	PB12	23	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD7	35	GPIO	PD8	36	GPIO
PC7	37	GPIO	VREGVSS	38	Voltage regulator VSS
VREGSW	39	DCDC regulator switching node	VREGVDD	40	Voltage regulator VDD input
DVDD	41	Digital power supply.	DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	43	GPIO	PE5	44	GPIO
PE6	45	GPIO	PE7	46	GPIO
PC12	47	GPIO (5V)	PC13	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	PF3	52	GPIO
PF4	53	GPIO	PF5	54	GPIO
PE8	56	GPIO	PE9	57	GPIO
PE10	58	GPIO	PE11	59	GPIO
PE12	60	GPIO	PE13	61	GPIO
PE14	62	GPIO	PE15	63	GPIO
PA15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A23	0: PC0 1: PC11 2: PH11 3: PE5		External Bus Interface (EBI) address output pin 23.
EBI_A24	0: PC1 1: PF0 2: PH12 3: PE6		External Bus Interface (EBI) address output pin 24.
EBI_A25	0: PC2 1: PF1 2: PH13 3: PE7		External Bus Interface (EBI) address output pin 25.
EBI_A26	0: PC4 1: PF2 2: PH14 3: PC8		External Bus Interface (EBI) address output pin 26.
EBI_A27	0: PD2 1: PF5 2: PH15 3: PC9		External Bus Interface (EBI) address output pin 27.
EBI_AD00	0: PE8 1: PB0 2: PG0		External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	0: PE9 1: PB1 2: PG1		External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	0: PE10 1: PB2 2: PG2		External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	0: PE11 1: PB3 2: PG3		External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	0: PE12 1: PB4 2: PG4		External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	0: PE13 1: PB5 2: PG5		External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	0: PE14 1: PB6 2: PG6		External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	0: PE15 1: PC0 2: PG7		External Bus Interface (EBI) address and data input / output pin 07.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US5_RX	0: PE9 1: PA7 2: PB1 3: PH11		USART5 Asynchronous Receive. USART5 Synchronous mode Master Input / Slave Output (MISO).
US5_TX	0: PE8 1: PA6 2: PF15 3: PH10		USART5 Asynchronous Transmit. Also used as receive input in half duplex communication. USART5 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	0: PF10		USB D- pin.
USB_DP	0: PF11		USB D+ pin.
USB_ID	0: PF12		USB ID pin.
USB_VBUSEN	0: PF5		USB 5 V VBUS enable.
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6 2: PG2 3: PG8	4: PC15 5: PB0 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5 1: PD13 2: PG3 3: PG9	4: PF0 5: PB1 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.

Alternate Functionality	Location	Priority
US2_CLK	4: PF8 5: PF2	High Speed High Speed
US2_CS	4: PF9 5: PF5	High Speed High Speed
US2_RX	4: PF7 5: PF1	High Speed High Speed
US2_TX	4: PF6 5: PF0	High Speed High Speed

Table 5.23. ACMP0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP0X																									PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
APORT0Y	BUSACMP0Y																									PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.28. ADC1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSADC1X																									PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
APORT0Y	BUSADC1Y																									PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
VDAC0_OUT1 / OPA1_OUT																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 9.1. BGA112 Package Dimensions

Dimension	Min	Typ	Max
A	-	-	1.30
A1	0.55	0.60	0.65
A2		0.21 BSC	
A3	0.30	0.35	0.40
d	0.43	0.48	0.53
D		10.00 BSC	
D1		8.00 BSC	
E		10.00 BSC	
E1		8.00 BSC	
e1		0.80 BSC	
e2		0.80 BSC	
L1		1.00 REF	
L2		1.00 REF	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. TQFP100 Package Specifications

10.1 TQFP100 Package Dimensions

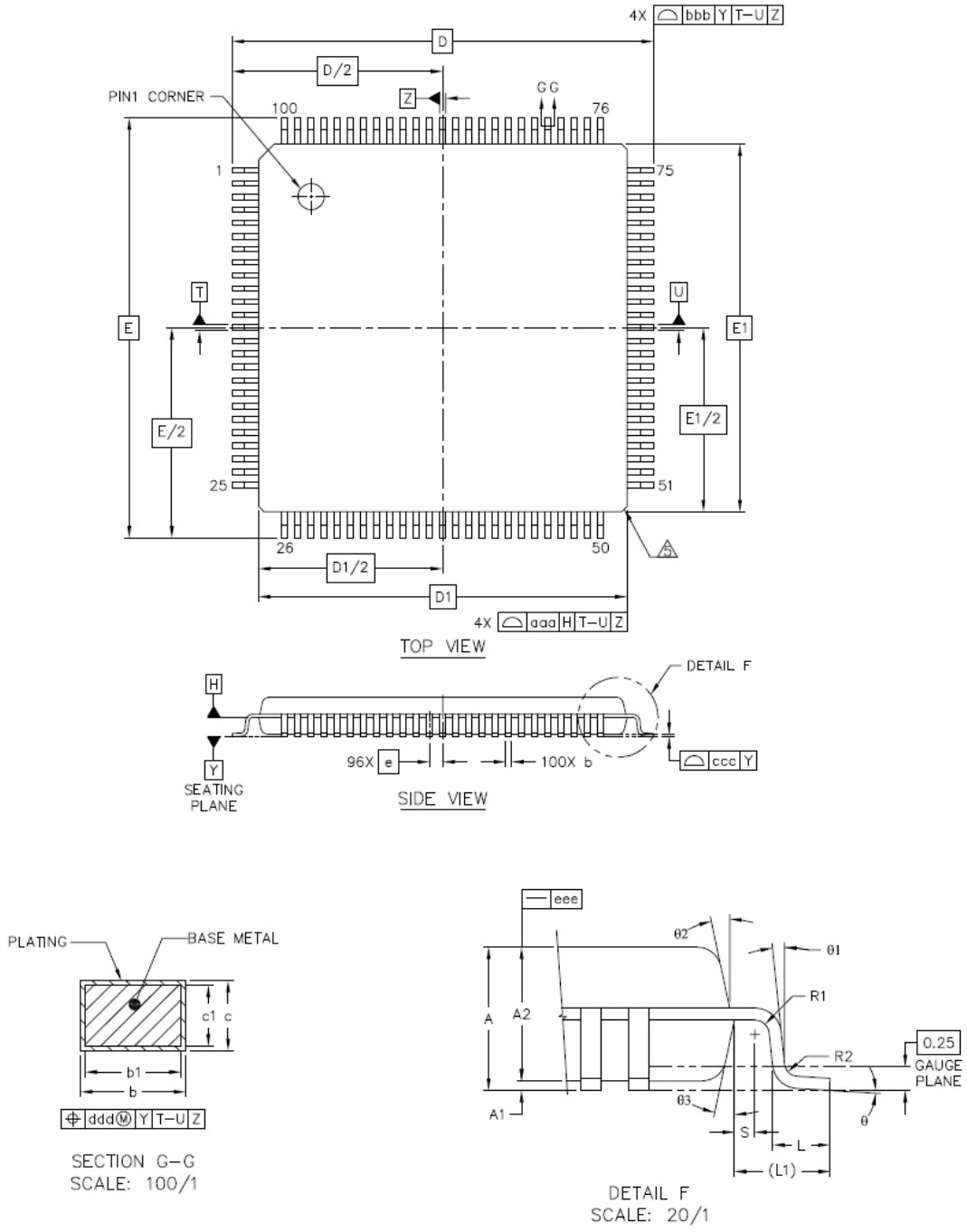

Figure 10.1. TQFP100 Package Drawing

Table 12.1. QFN64 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.203 REF		
D	9.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.