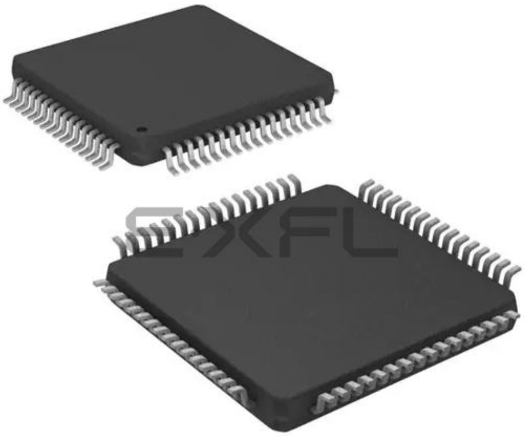

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b520f2048iq64-ar

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.
6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - (THETA_{JA} x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and THETA_{JA}.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN64 Package	$\text{THETA}_{\text{JA\_QFN64}}$	4-Layer PCB, Air velocity = 0 m/s	—	17.8	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	15.4	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	13.8	—	°C/W
Thermal resistance, TQFP64 Package	$\text{THETA}_{\text{JA\_TQFP64}}$	4-Layer PCB, Air velocity = 0 m/s	—	33.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	32.1	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	30.1	—	°C/W
Thermal resistance, TQFP100 Package	$\text{THETA}_{\text{JA\_TQFP100}}$	4-Layer PCB, Air velocity = 0 m/s	—	44.1	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	37.7	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	35.5	—	°C/W
Thermal resistance, BGA112 Package	$\text{THETA}_{\text{JA\_BGA112}}$	4-Layer PCB, Air velocity = 0 m/s	—	42.0	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	37.0	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	35.3	—	°C/W
Thermal resistance, BGA120 Package	$\text{THETA}_{\text{JA\_BGA120}}$	4-Layer PCB, Air velocity = 0 m/s	—	47.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	41.8	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	39.6	—	°C/W
Thermal resistance, BGA152 Package	$\text{THETA}_{\text{JA\_BGA152}}$	4-Layer PCB, Air velocity = 0 m/s	—	35.7	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	31.0	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	29.5	—	°C/W
Thermal resistance, BGA192 Package	$\text{THETA}_{\text{JA\_BGA192}}$	4-Layer PCB, Air velocity = 0 m/s	—	47.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	41.8	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	39.6	—	°C/W

4.1.11 Flash Memory Characteristics[5]

Table 4.19. Flash Memory Characteristics[5]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}	T ≤ 85 °C	10	—	—	years
		T ≤ 125 °C	10	—	—	years
Word (32-bit) programming time	t_{W_PROG}	Burst write, 128 words, average time per word	20	26.2	32	µs
		Single word	59	68.7	83	µs
Page erase time[4]	t_{PERASE}		20	26.8	35	ms
Mass erase time[1]	t_{MERASE}		20	26.9	35	ms
Device erase time[2] [3]	t_{DERASE}	T ≤ 85 °C	—	80.7	95	ms
		T ≤ 125 °C	—	80.7	100	ms
Erase current[6]	I_{ERASE}	Page Erase	—	—	1.7	mA
		Mass or Device Erase	—	—	2.1	mA
Write current[6]	I_{WRITE}		—	—	3.9	mA
Supply voltage during flash erase and write	V_{FLASH}		1.62	—	3.6	V

Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
5. Flash data retention information is published in the Quarterly Quality and Reliability Report.
6. Measured at 25 °C.

4.1.23 I2C

4.1.23.1 I2C Standard-mode (Sm)[1]

Table 4.31. I2C Standard-mode (Sm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	3450	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		4	—	—	µs
STOP condition set-up time	t_{SU_STO}		4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

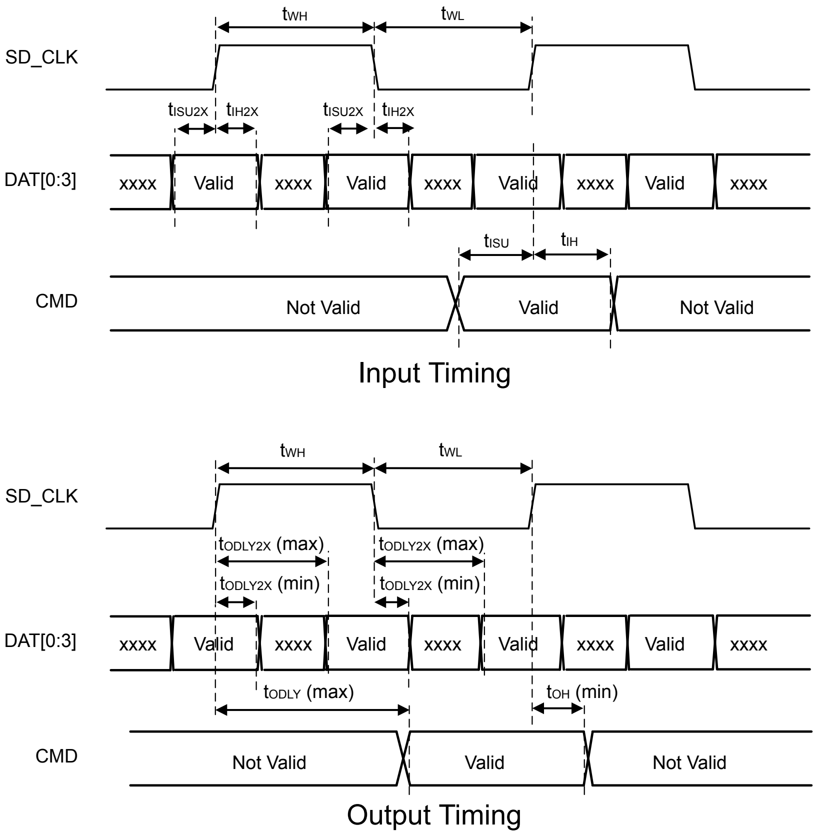

Figure 4.16. SDIO DDR Mode Timing

SDIO MMC SDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.50. SDIO MMC SDR Mode Timing (Location 0, 1.8V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	25	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.96	8.27	—	ns
Clock fall time	t_F		1.67	6.90	—	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:7] change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	t_{OH}		3	—	—	ns

SDIO MMC DDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Table 4.53. SDIO MMC DDR Mode Timing (Location 0, 3V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.13	2.37	—	ns
Clock fall time	t_F		1.01	2.02	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		3	—	—	ns
Input setup time, DAT[0:7] valid to SD_CLK	t_{ISU2X}		5.3	—	—	ns
Input hold time, SD_CLK to DAT[0:7] change	t_{IH2X}		2.5	—	—	ns
Output delay time, SD_CLK to DAT[0:7] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:7] change	t_{OH2X}		3	—	—	ns

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF13	B9	GPIO (5V)
PF4	B10	GPIO	PF3	B11	GPIO
NC	B12	No Connect.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 L12 L15	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L16	Digital IO power supply 0.
PF2	C10	GPIO	PF1	C11	GPIO (5V)
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PF0	D11	GPIO (5V)
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PC9	E11	GPIO (5V)
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE6	F11	GPIO
PE7	F12	GPIO	PC8	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE3	G11	GPIO
PE4	G12	GPIO	PE5	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
DECOUPLE	H13	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PD14	J1	GPIO (5V)
PD15	J2	GPIO (5V)	PE1	J12	GPIO (5V)
VREGVDD	J13	Voltage regulator VDD input	PC0	K1	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA12	17	GPIO (5V)	PA13	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	VREGI	45	Input to 5 V regulator.
VREGO	46	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs	PF10	47	GPIO (5V)
PF11	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.17 EFM32GG11B5xx in QFN64 Device Pinout

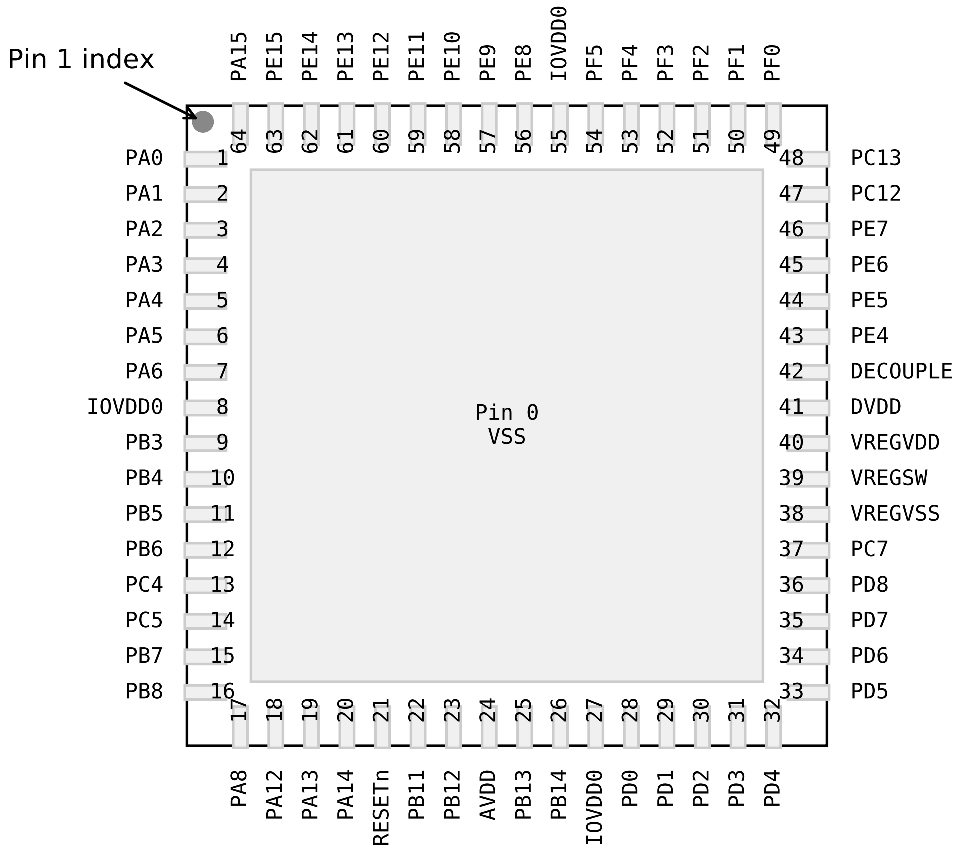

Figure 5.17. EFM32GG11B5xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.17. EFM32GG11B5xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Alternate	LOCATION		
Functionality	**0 - 3**	**4 - 7**	**Description**
EBI_CS1	0: PD10 1: PA11 2: PC1 3: PB1	4: PE9	External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	0: PD11 1: PA12 2: PC2 3: PB2	4: PE10	External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	0: PD12 1: PB15 2: PC3 3: PB3	4: PE11	External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	0: PA7 1: PF6 2: PB12 3: PA0		External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	0: PA8 1: PF7 2: PH0 3: PA1		External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	0: PA9 1: PD9 2: PH1 3: PA2		External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	0: PA11 1: PD11 2: PH3 3: PA4		External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	0: PC3 1: PD15 2: PB9 3: PC4	4: PC15 5: PF12	External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	0: PC5 1: PD14 2: PA13 3: PC2	4: PC14 5: PF11	External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	0: PF5 1: PA14 2: PA12 3: PC0	4: PF9 5: PF5	External Bus Interface (EBI) Read Enable output.
EBI_VSNC	0: PA10 1: PD10 2: PH2 3: PA3		External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	0: PF4 1: PA13 2: PC5 3: PB6	4: PF8 5: PF4	External Bus Interface (EBI) Write Enable output.
ETH_MDC	0: PB4 1: PD14 2: PC1 3: PA6		Ethernet Management Data Clock.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_TSUTMR-TOG	0: PB6 1: PB15 2: PC3 3: PF9		Ethernet IEEE1588 Timer Toggle.
ETM_TCLK	0: PD7 1: PF8 2: PC6 3: PA6	4: PE11 5: PG15	Embedded Trace Module ETM clock .
ETM_TD0	0: PD6 1: PF9 2: PC7 3: PA2	4: PE12 5: PG14	Embedded Trace Module ETM data 0.
ETM_TD1	0: PD3 1: PD13 2: PD3 3: PA3	4: PE13 5: PG13	Embedded Trace Module ETM data 1.
ETM_TD2	0: PD4 1: PB15 2: PD4 3: PA4	4: PE14 5: PG12	Embedded Trace Module ETM data 2.
ETM_TD3	0: PD5 1: PF3 2: PD5 3: PA5	4: PE15 5: PG11	Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PRS_CH7	0: PB13 1: PA7 2: PE7		Peripheral Reflex System PRS, channel 7.
PRS_CH8	0: PA8 1: PA2 2: PE9		Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA9 1: PA3 2: PB10		Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PA10 1: PC2 2: PD4		Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PA11 1: PC3 2: PD5		Peripheral Reflex System PRS, channel 11.
PRS_CH12	0: PA12 1: PB6 2: PD8		Peripheral Reflex System PRS, channel 12.
PRS_CH13	0: PA13 1: PB9 2: PE14		Peripheral Reflex System PRS, channel 13.
PRS_CH14	0: PA14 1: PC6 2: PE15		Peripheral Reflex System PRS, channel 14.
PRS_CH15	0: PA15 1: PC7 2: PF0		Peripheral Reflex System PRS, channel 15.
PRS_CH16	0: PA4 1: PB12 2: PE4		Peripheral Reflex System PRS, channel 16.
PRS_CH17	0: PA5 1: PB15 2: PE5		Peripheral Reflex System PRS, channel 17.
PRS_CH18	0: PB2 1: PC10 2: PC4		Peripheral Reflex System PRS, channel 18.
PRS_CH19	0: PB3 1: PC11 2: PC5		Peripheral Reflex System PRS, channel 19.

Table 5.24. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP1X																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT0Y	BUSACMP1Y																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

7. BGA152 Package Specifications

7.1 BGA152 Package Dimensions

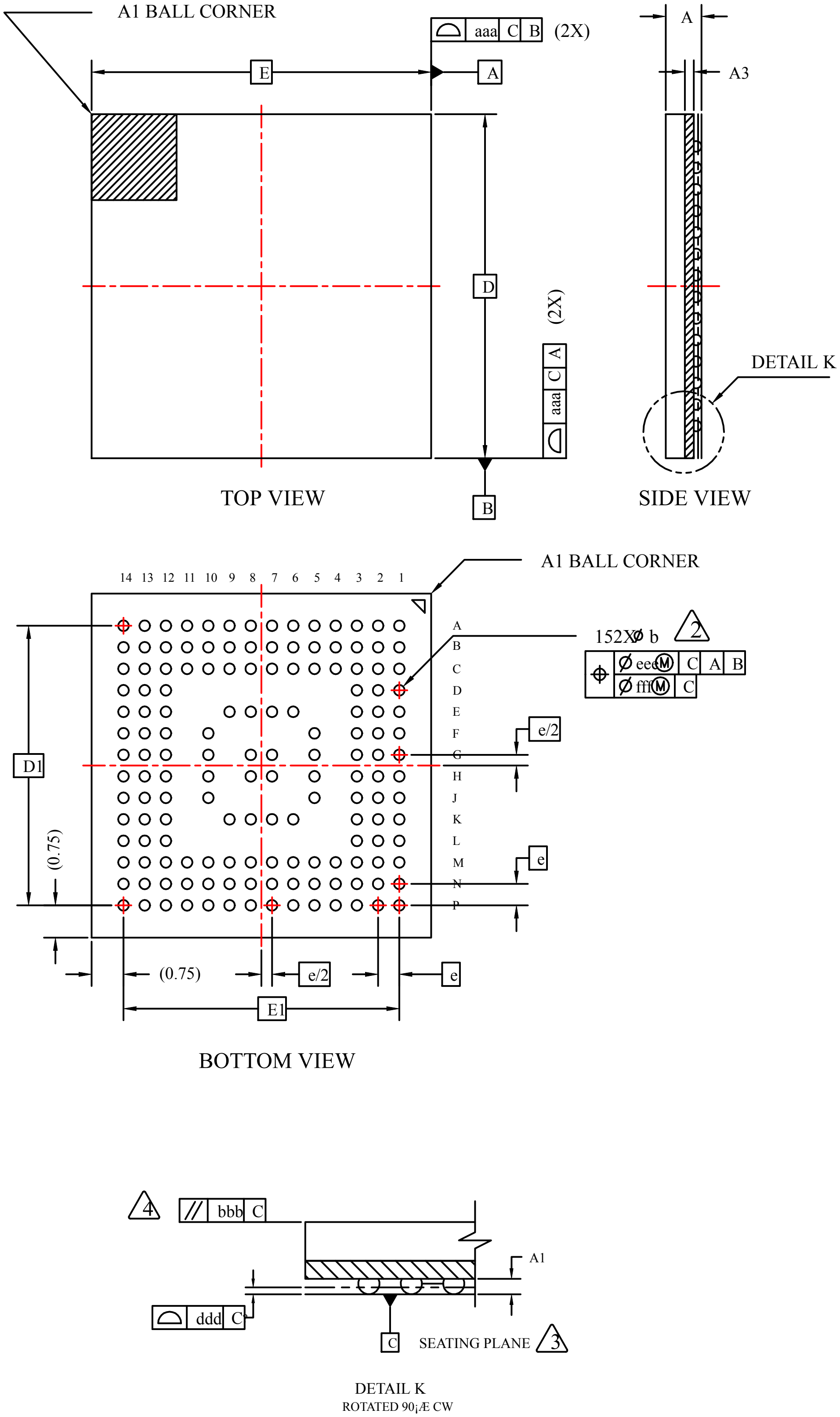

Figure 7.1. BGA152 Package Drawing

7.2 BGA152 PCB Land Pattern

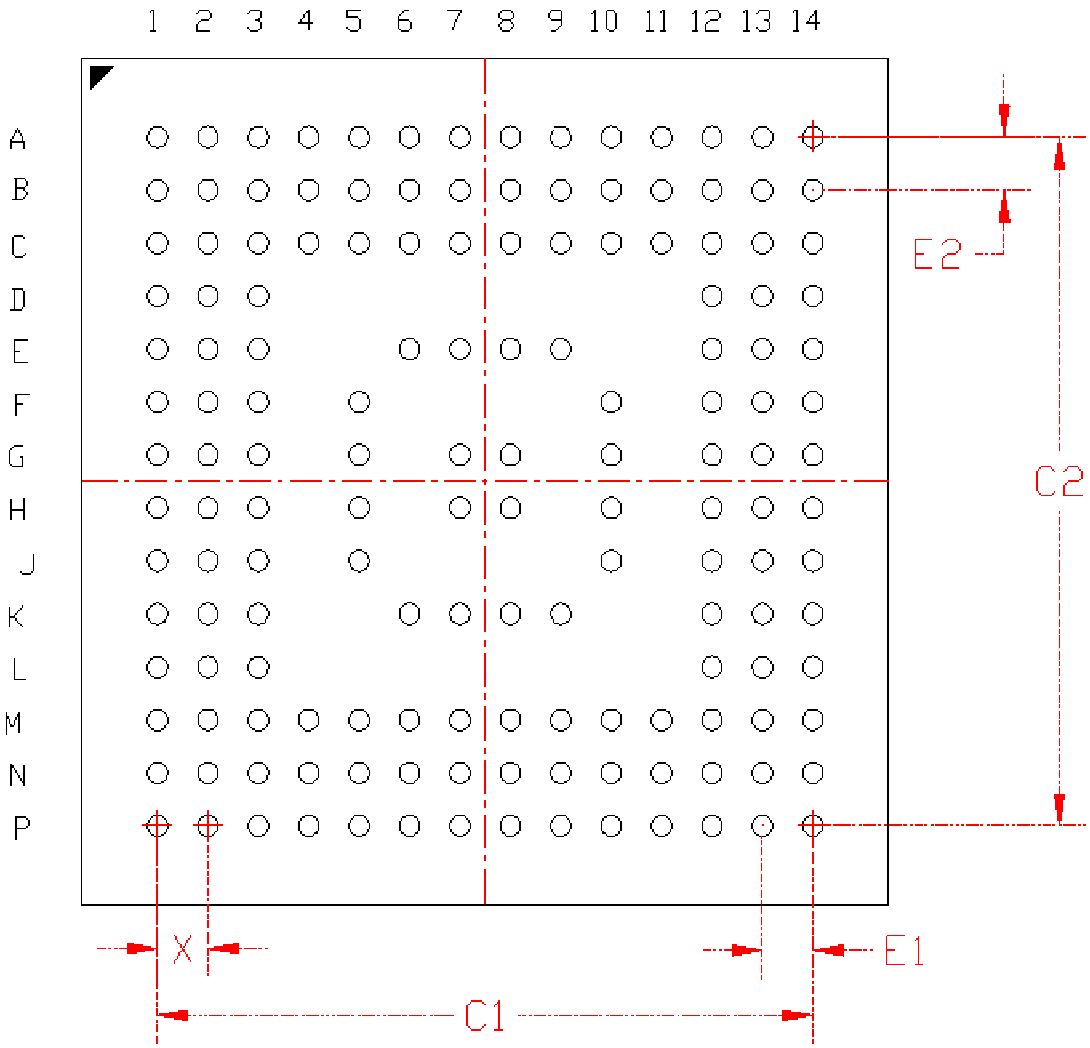

Figure 7.2. BGA152 PCB Land Pattern Drawing

Table 7.2. BGA152 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X	0.20		
C1	6.50		
C2	6.50		
E1	0.5		
E2	0.5		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Table 10.2. TQFP100 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
C1		15.4	
C2		15.4	
E		0.50 BSC	
X		0.30	
Y		1.50	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10.3 TQFP100 Package Marking

Figure 10.3. TQFP100 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

13. Revision History

Revision 0.6

March, 2018

- Removed "Confindential" watermark.
- Updated 4.1 Electrical Characteristics and 4.2 Typical Performance Curves with latest characterization data.

Revision 0.2

October, 2017

- Updated memory maps to latest formatting and to include all peripherals.
- Updated all electrical specifications tables with latest characterization results.
- **Absolute Maximum Ratings** Table:
  - Removed redundant I_{VSSMAX} line.
  - Added footnote to clarify V_{DIGPIN} specification for 5V tolerant GPIO.
- **General Operating Conditions** Table:
  - Removed dV_{DD} specification and redundant footnote about shorting VREGVDD and AVDD together.
  - Added footnote about IOVDD voltage restriction when CSEN peripheral is used with chopping enabled.
- **Flash Memory Characteristics** Table: Added timing measurement clarification for Device Erase and Mass Erase.
- **Analog to Digital Converter (ADC)** Table:
  - Added header text for general specification conditions.
  - Added footnote for clarification of input voltage limits.
- Minor typographical corrections, including capitalization, mis-spellings and punctuation marks, throughout document.
- Minor formatting and styling updates, including table formats, TOC location, and boilerplate information throughout document.

Revision 0.1

April 27th, 2017

Initial release.