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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, I <sup>2</sup> C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b520f2048iq64-b">https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b520f2048iq64-b</a>

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode <sup>3</sup>	I <sub>ACTIVE_LPM</sub>	32 MHz HFRCO, CPU running while loop from flash	—	82	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	83	—	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	88	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	257	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode <sup>1</sup>	I <sub>ACTIVE_CCM_VS</sub>	19 MHz HFRCO, CPU running while loop from flash	—	117	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1231	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode <sup>3</sup>	I <sub>ACTIVE_LPM_VS</sub>	19 MHz HFRCO, CPU running while loop from flash	—	72	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	219	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode <sup>2</sup>	I <sub>EM1_DCM</sub>	72 MHz HFRCO	—	42	—	μA/MHz
		50 MHz crystal	—	46	—	μA/MHz
		48 MHz HFRCO	—	46	—	μA/MHz
		32 MHz HFRCO	—	53	—	μA/MHz
		26 MHz HFRCO	—	57	—	μA/MHz
		16 MHz HFRCO	—	72	—	μA/MHz
		1 MHz HFRCO	—	663	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode <sup>3</sup>	I <sub>EM1_LPM</sub>	32 MHz HFRCO	—	42	—	μA/MHz
		26 MHz HFRCO	—	43	—	μA/MHz
		16 MHz HFRCO	—	48	—	μA/MHz
		1 MHz HFRCO	—	219	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode <sup>2</sup>	I <sub>EM1_DCM_VS</sub>	19 MHz HFRCO	—	60	—	μA/MHz
		1 MHz HFRCO	—	637	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode <sup>3</sup>	I <sub>EM1_LPM_VS</sub>	19 MHz HFRCO	—	39	—	μA/MHz
		1 MHz HFRCO	—	190	—	μA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode <sup>3</sup>	I <sub>EM2_VS</sub>	Full 512 kB RAM retention and RTCC running from LFXO	—	2.8	—	μA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	3.1	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO <sup>5</sup>	—	2.1	—	μA
Current consumption in EM3 mode, with voltage scaling enabled	I <sub>EM3_VS</sub>	Full 512 kB RAM retention and CRYOTIMER running from ULFR-CO	—	2.4	—	μA

## 4.1.10 Oscillators

### 4.1.10.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.12. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	$f_{\text{LFXO}}$		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	$\text{ESR}_{\text{LFXO}}$		—	—	70	k $\Omega$
Supported range of crystal load capacitance <sup>1</sup>	$C_{\text{LFXO\_CL}}$		6	—	18	pF
On-chip tuning cap range <sup>2</sup>	$C_{\text{LFXO\_T}}$	On each of LFX TAL_N and LFX TAL_P pins	8	—	40	pF
On-chip tuning cap step size	$\text{SS}_{\text{LFXO}}$		—	0.25	—	pF
Current consumption after startup <sup>3</sup>	$I_{\text{LFXO}}$	ESR = 70 k $\Omega$ m, $C_L$ = 7 pF, GAIN <sup>4</sup> = 2, AGC <sup>4</sup> = 1	—	273	—	nA
Start- up time	$t_{\text{LFXO}}$	ESR = 70 k $\Omega$ m, $C_L$ = 7 pF, GAIN <sup>4</sup> = 2	—	308	—	ms

**Note:**

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be  $C_{\text{LFXO\_T}}/2$ . This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU\_PWRCTRL register.
4. In CMU\_LFXOCTRL register.

#### 4.1.21 Pulse Counter (PCNT)

**Table 4.29. Pulse Counter (PCNT)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	$F_{IN}$	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

#### 4.1.22 Analog Port (APORT)

**Table 4.30. Analog Port (APORT)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current <sup>2 1</sup>	$I_{APORT}$	Operation in EM0/EM1	—	7	—	$\mu A$
		Operation in EM2/EM3	—	915	—	nA

**Note:**

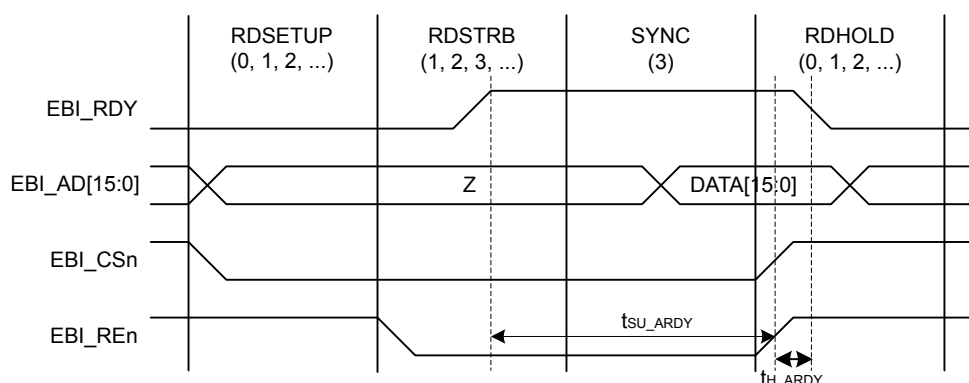
- Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by multiplying the duty cycle of the requests by the specified continuous current number.
- Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

## EBI Ready/Wait Timing Requirements

Timing applies to both EBI\_REn and EBI\_WEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.41. EBI Ready/Wait Timing Requirements**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge	$t_{SU\_ARDY}$	IOVDD $\geq$ 1.62 V	$55 + (3 * t_{HFCOR-ECLK})$	—	—	ns
		IOVDD $\geq$ 3.0 V	$36 + (3 * t_{HFCOR-ECLK})$	—	—	ns
Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid	$t_{H\_ARDY}$	IOVDD $\geq$ 1.62 V	-9	—	—	ns



**Figure 4.8. EBI Ready/Wait Timing Requirements**

## SDIO DDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD\_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO\_CTRL\_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 30 pF on all pins.

**Table 4.49. SDIO DS Mode Timing (Location 0)**

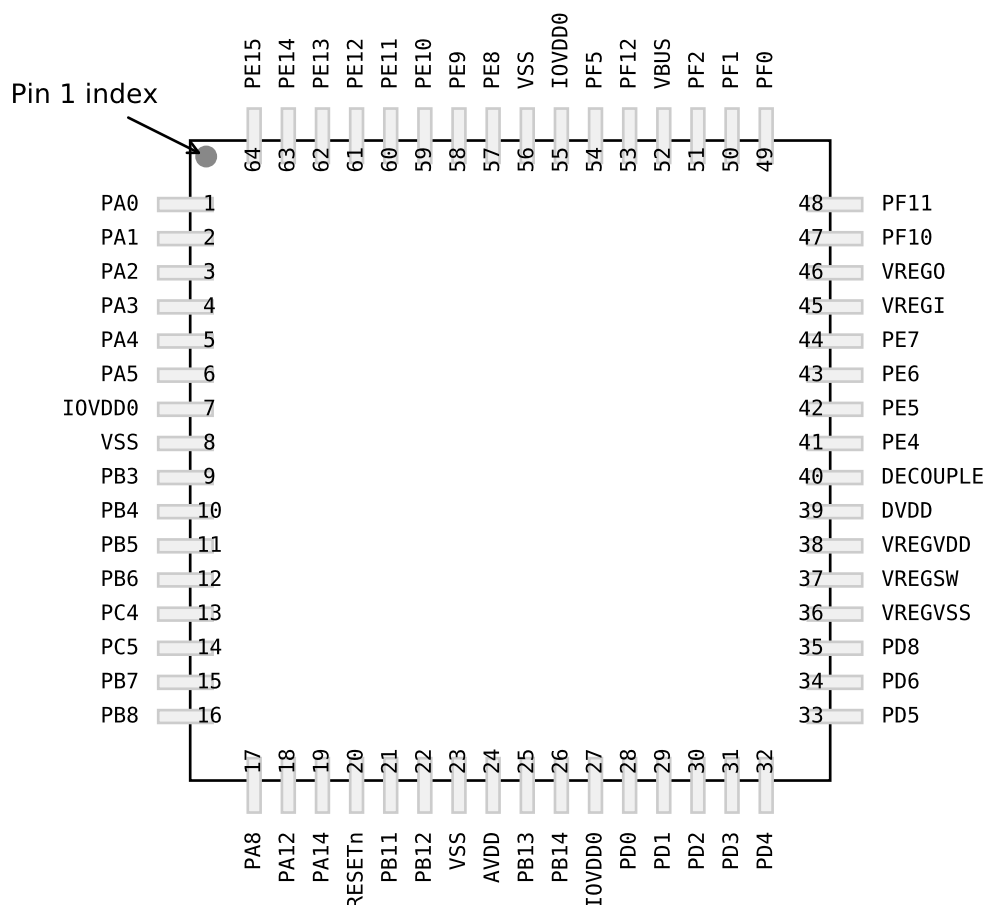
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	$F_{SD\_CLK}$	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	$t_{WL}$	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	$t_{WH}$	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	$t_R$		1.69	6.52	—	ns
Clock fall time	$t_F$		1.42	4.96	—	ns
Input setup time, CMD valid to SD_CLK	$t_{ISU}$		6	—	—	ns
Input hold time, SD_CLK to CMD change	$t_{IH}$		1.8	—	—	ns
Output delay time, SD_CLK to CMD valid	$t_{ODLY}$		0	—	16	ns
Output hold time, SD_CLK to CMD change	$t_{OH}$		0.8	—	—	ns
Input setup time, DAT[0:3] valid to SD_CLK	$t_{ISU2X}$		6	—	—	ns
Input hold time, SD_CLK to DAT[0:3] change	$t_{IH2X}$		1.5	—	—	ns
Output delay time, SD_CLK to DAT[0:3] valid	$t_{ODLY2X}$		0	—	16	ns
Output hold time, SD_CLK to DAT[0:3] change	$t_{OH2X}$		0.8	—	—	ns

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE8	B4	GPIO	PD11	B5	GPIO
PF8	B6	GPIO	PF6	B7	GPIO
VBUS	B8	USB VBUS signal and auxiliary input to 5 V regulator.	PE5	B9	GPIO
VREGI	B10	Input to 5 V regulator.	VREGO	B11	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
PD12	C5	GPIO	PF9	C6	GPIO
VSS	C7 D4 F9 G3 G9 H6 K4 K7 K10 L7	Ground	PF2	C8	GPIO
PE6	C9	GPIO	PC10	C10	GPIO (5V)
PC11	C11	GPIO (5V)	PA3	D1	GPIO
PA2	D2	GPIO	PB15	D3	GPIO (5V)
IOVDD1	D5	Digital IO power supply 1.	PD9	D6	GPIO
IOVDD0	D7 G8 H7 L4	Digital IO power supply 0.	PF1	D8	GPIO (5V)
PE7	D9	GPIO	PC8	D10	GPIO (5V)
PC9	D11	GPIO (5V)	PA6	E1	GPIO
PA5	E2	GPIO	PA4	E3	GPIO
PB0	E4	GPIO	PF0	E8	GPIO (5V)
PE0	E9	GPIO (5V)	PE1	E10	GPIO (5V)
PE3	E11	GPIO	PB1	F1	GPIO
PB2	F2	GPIO	PB3	F3	GPIO
PB4	F4	GPIO	DVDD	F8	Digital power supply.
PE2	F10	GPIO	DECOUPLE	F11	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PB5	G1	GPIO	PB6	G2	GPIO
IOVDD2	G4	Digital IO power supply 2.	PC6	G10	GPIO
PC7	G11	GPIO	PC0	H1	GPIO (5V)
PC2	H2	GPIO (5V)	PD14	H3	GPIO (5V)
PA7	H4	GPIO	PA8	H5	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 58 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB9	37	GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41 45	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	46	GPIO (5V)	PD1	47	GPIO
PD2	48	GPIO (5V)	PD3	49	GPIO
PD4	50	GPIO	PD5	51	GPIO
PD6	52	GPIO	PD7	53	GPIO
PD8	54	GPIO	PC6	55	GPIO
PC7	56	GPIO	DVDD	57	Digital power supply.
DECOUPLE	59	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE0	60	GPIO (5V)
PE1	61	GPIO (5V)	PE2	62	GPIO
PE3	63	GPIO	PE4	64	GPIO
PE5	65	GPIO	PE6	66	GPIO
PE7	67	GPIO	PC8	68	GPIO (5V)
PC9	69	GPIO (5V)	PC10	70	GPIO (5V)
PC11	71	GPIO (5V)	VREGI	72	Input to 5 V regulator.
VREGO	73	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs	PF10	74	GPIO (5V)
PF11	75	GPIO (5V)	PF0	76	GPIO (5V)



## 5.12 EFM32GG11B8xx in QFP64 Device Pinout



**Figure 5.12. EFM32GG11B8xx in QFP64 Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

**Table 5.12. EFM32GG11B8xx in QFP64 Device Pinout**

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

## 5.19 EFM32GG11B1xx in QFN64 Device Pinout

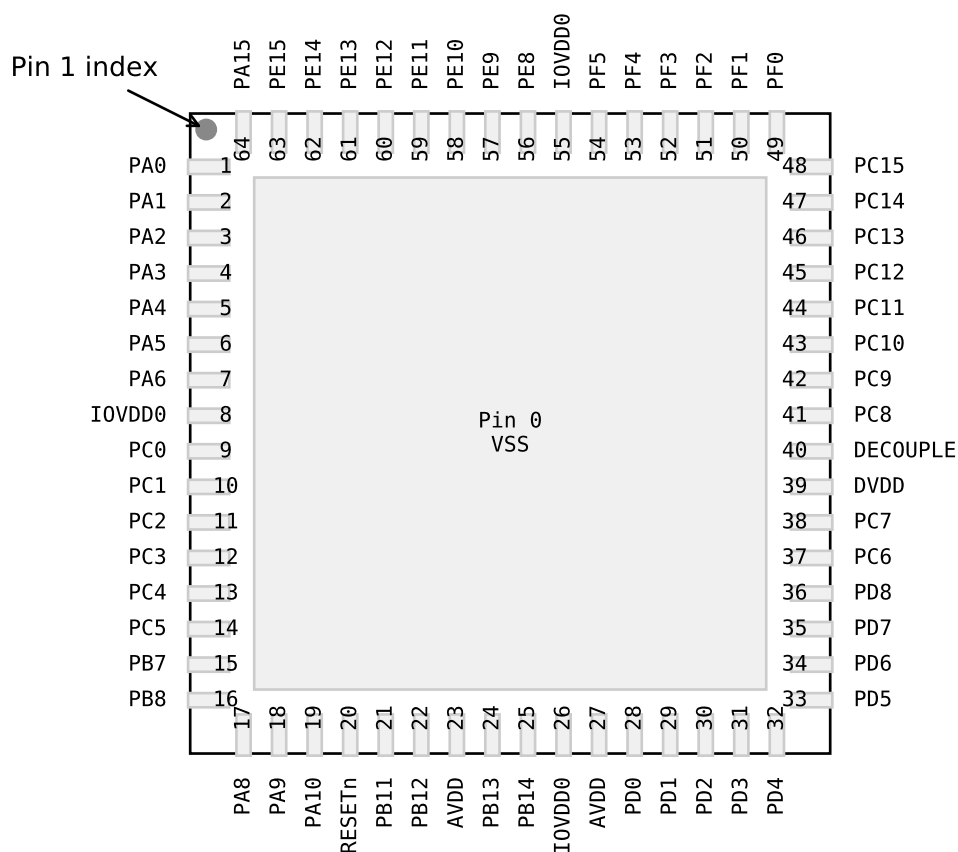


Figure 5.19. EFM32GG11B1xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.19. EFM32GG11B1xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PC0	9	GPIO (5V)
PC1	10	GPIO (5V)	PC2	11	GPIO (5V)

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD15		EBI_NANDREn #1	TIM2_CDTI2 #1 TIM3_CC0 #7 WTIM0_CDTI0 #1 PCNT1_S0IN #2	ETH_TSUEXTCLK #1 CAN0_TX #5 US5_CTS #1 I2C0_SCL #3	
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSACMP1Y BU- SACMP1X	EBI_ARDY #4	TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 TIM5_CC2 #5 WTIM3_CC2 #2 PCNT0_S0IN #0 PCNT2_S1IN #4	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3 U1_RX #0 I2C2_SCL #6	LES_CH13 PRS_CH21 #1 ACMP3_O #3
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSACMP1Y BU- SACMP1X		TIM1_CC3 #0 TIM5_CC1 #5 WTIM3_CC1 #2 PCNT2_S0IN #4	CAN1_RX #4 US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3 U1_TX #0 I2C2_SDA #6	CMU_CLK0 #1 LES_CH12 PRS_CH20 #1
PC11	BUSACMP1Y BU- SACMP1X	EBI_ALE #4 EBI_ALE #5 EBI_A23 #1	TIM5_CC0 #5 WTIM3_CC0 #2	CAN1_TX #4 US0_TX #2 I2C1_SDA #4	LES_CH11 PRS_CH19 #1
PA3	BUSAY BUSBX LCD_SEG16	EBI_AD12 #0 EBI_VSNC #3	TIM0_CDTI0 #0 TIM3_CC0 #5	ETH_RMIREFCLK #0 ETH_MIITXD1 #0 SDIO_DAT3 #1 US3_CS #0 U0_TX #2 QSPI0_DQ1 #1	CMU_CLK2 #1 CMU_CLKI0 #1 CMU_CLK2 #4 LES_ALTEX2 PRS_CH9 #1 ETM_TD1 #3
PG2	BUSACMP2Y BU- SACMP2X	EBI_AD02 #2	TIM6_CC2 #0 TIM2_CDTI2 #3 WTIM0_CC0 #2 LE- TIM1_OUT0 #7	ETH_MIITXD2 #1 US3_CLK #4 QSPI0_DQ1 #2	CMU_CLK0 #3
PG1	BUSACMP2Y BU- SACMP2X	EBI_AD01 #2	TIM6_CC1 #0 TIM2_CDTI1 #3 WTIM0_CDTI2 #1 LETIM1_OUT1 #6	ETH_MIITXD3 #1 US3_RX #4 QSPI0_DQ0 #2	CMU_CLK1 #3
PC10	BUSACMP1Y BU- SACMP1X	EBI_A10 #2 EBI_A22 #1	TIM2_CC2 #2 TIM5_CC2 #4 WTIM3_CC2 #1	CAN1_TX #3 US0_RX #2	LES_CH10 PRS_CH18 #1
PC9	BUSACMP1Y BU- SACMP1X	EBI_A09 #2 EBI_A21 #1 EBI_A27 #3	TIM2_CC1 #2 TIM5_CC1 #4 WTIM3_CC1 #1	CAN1_RX #3 US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2
PC8	BUSACMP1Y BU- SACMP1X	EBI_A08 #2 EBI_A15 #0 EBI_A20 #1 EBI_A26 #3	TIM2_CC0 #2 TIM5_CC0 #4 WTIM3_CC0 #1	US0_CS #2	LES_CH8 PRS_CH4 #0
PA4	BUSBY BUSAX LCD_SEG17	EBI_AD13 #0 EBI_HSNC #3	TIM0_CDTI1 #0 TIM3_CC1 #5	ETH_RMIICRSV #0 ETH_MIITXD0 #0 SDIO_DAT4 #1 US3_CTS #0 U0_RX #2 QSPI0_DQ2 #1	LES_ALTEX3 PRS_CH16 #0 ETM_TD2 #3
PG4	BUSACMP2Y BU- SACMP2X	EBI_AD04 #2	TIM6_CDTI1 #0 WTIM0_CC2 #2	ETH_MIITXD0 #1 US3_CTS #4 QSPI0_DQ3 #2	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_CH11	0: PC11		LESENSE channel 11.
LES_CH12	0: PC12		LESENSE channel 12.
LES_CH13	0: PC13		LESENSE channel 13.
LES_CH14	0: PC14		LESENSE channel 14.
LES_CH15	0: PC15		LESENSE channel 15.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8 7: PB9	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9 7: PB10	Low Energy Timer LETIM0, output channel 1.
LETIM1_OUT0	0: PA7 1: PA11 2: PA12 3: PC2	4: PB5 5: PB2 6: PG0 7: PG2	Low Energy Timer LETIM1, output channel 0.
LETIM1_OUT1	0: PA6 1: PA13 2: PA14 3: PC3	4: PB6 5: PB1 6: PG1 7: PG3	Low Energy Timer LETIM1, output channel 1.
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	0: PC7 1: PA6 2: PD3 3: PB1	4: PB5 5: PH1	LEUART1 Receive input.
LEU1_TX	0: PC6 1: PA5 2: PD2 3: PB0	4: PB4 5: PH0	LEUART1 Transmit output. Also used as receive input in half duplex communication.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.
OPA2_OUT	0: PD5		Operational Amplifier 2 output.
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.
OPA3_N	0: PC7		Operational Amplifier 3 external negative input.
OPA3_OUT	0: PD1		Operational Amplifier 3 output.
OPA3_P	0: PC6		Operational Amplifier 3 external positive input.

## 6.2 BGA192 PCB Land Pattern

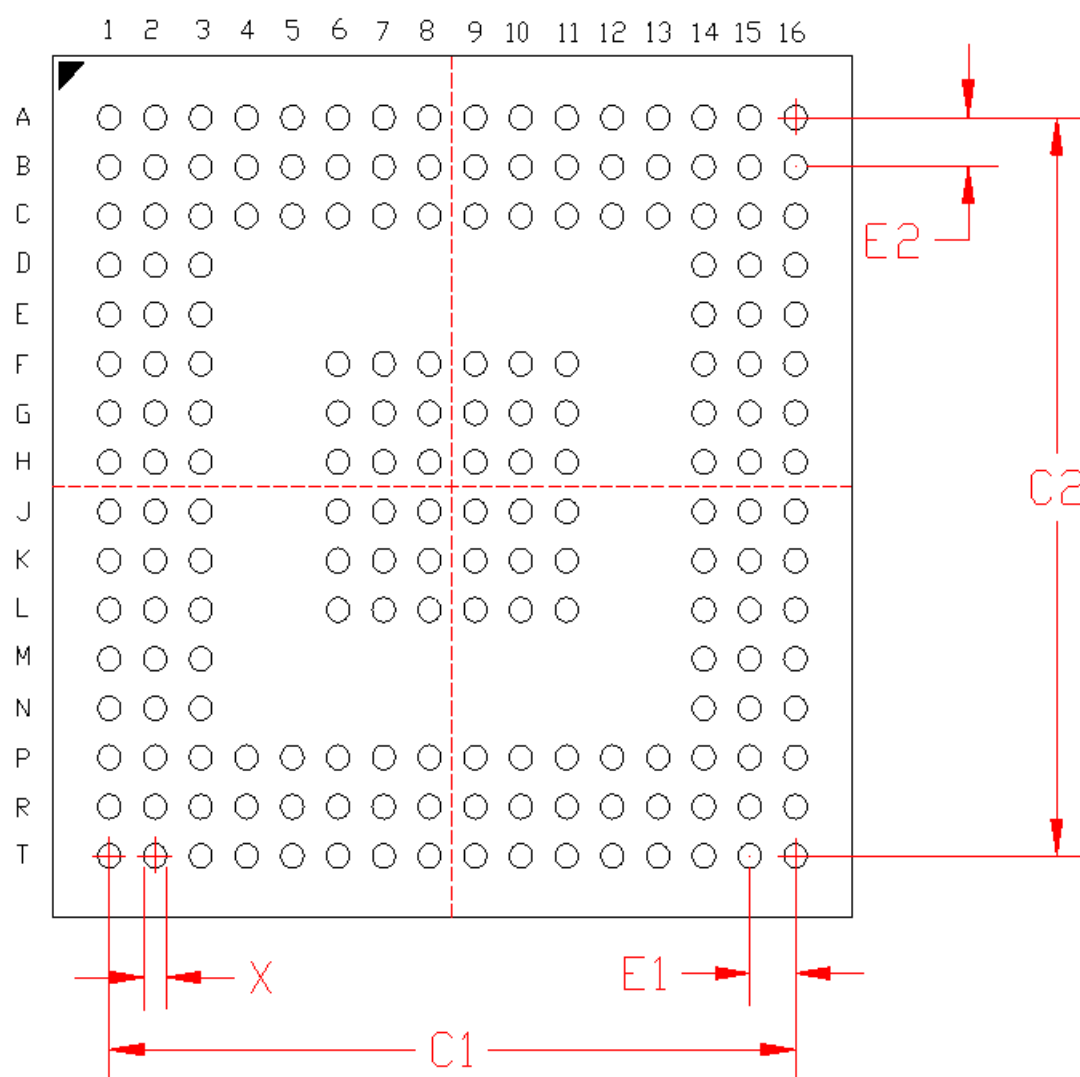


Figure 6.2. BGA192 PCB Land Pattern Drawing

**Table 8.2. BGA120 PCB Land Pattern Dimensions**

Dimension	Min	Nom	Max
X		0.20	
C1		6.00	
C2		6.00	
E1		0.5	
E2		0.5	

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 9. BGA112 Package Specifications

### 9.1 BGA112 Package Dimensions

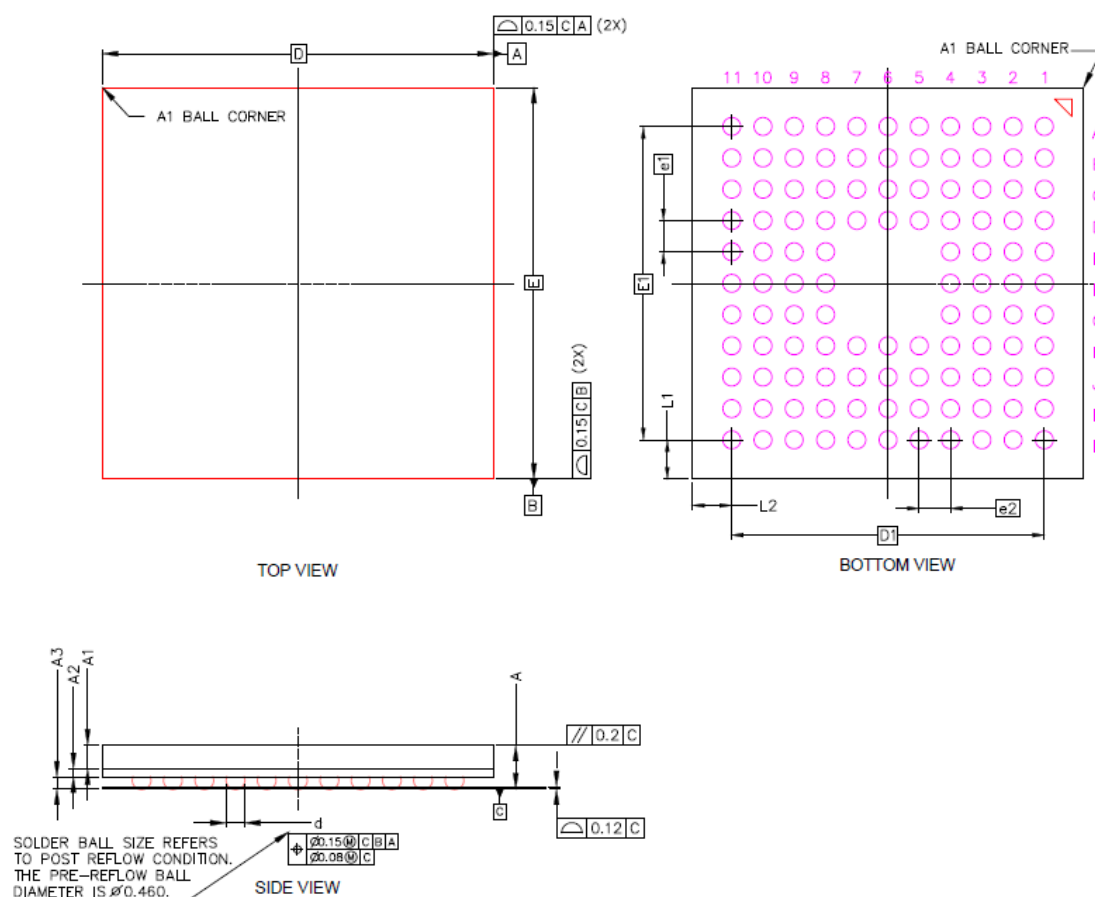


Figure 9.1. BGA112 Package Drawing



## 9.2 BGA112 PCB Land Pattern

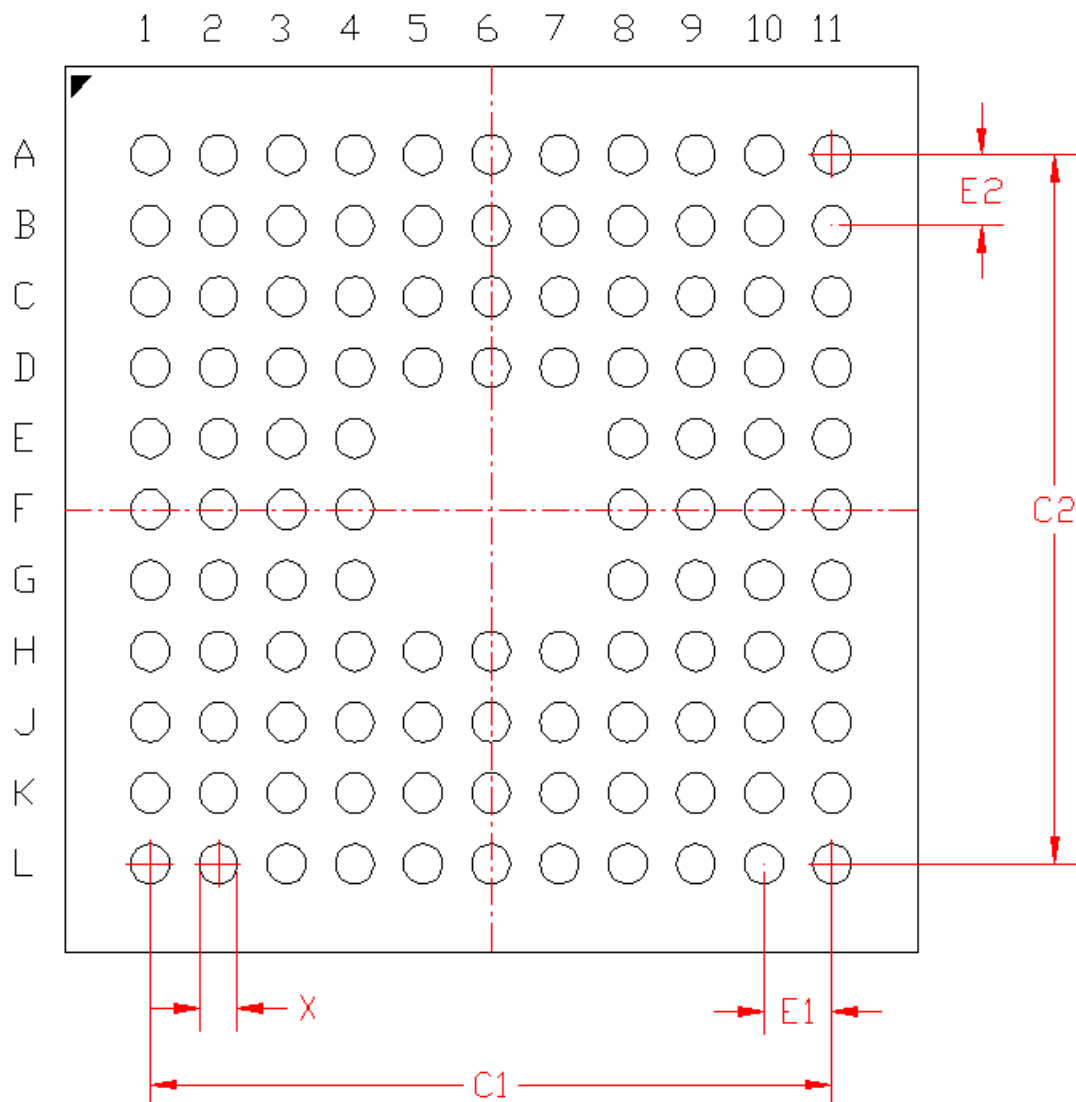


Figure 9.2. BGA112 PCB Land Pattern Drawing

## 10. TQFP100 Package Specifications

### 10.1 TQFP100 Package Dimensions

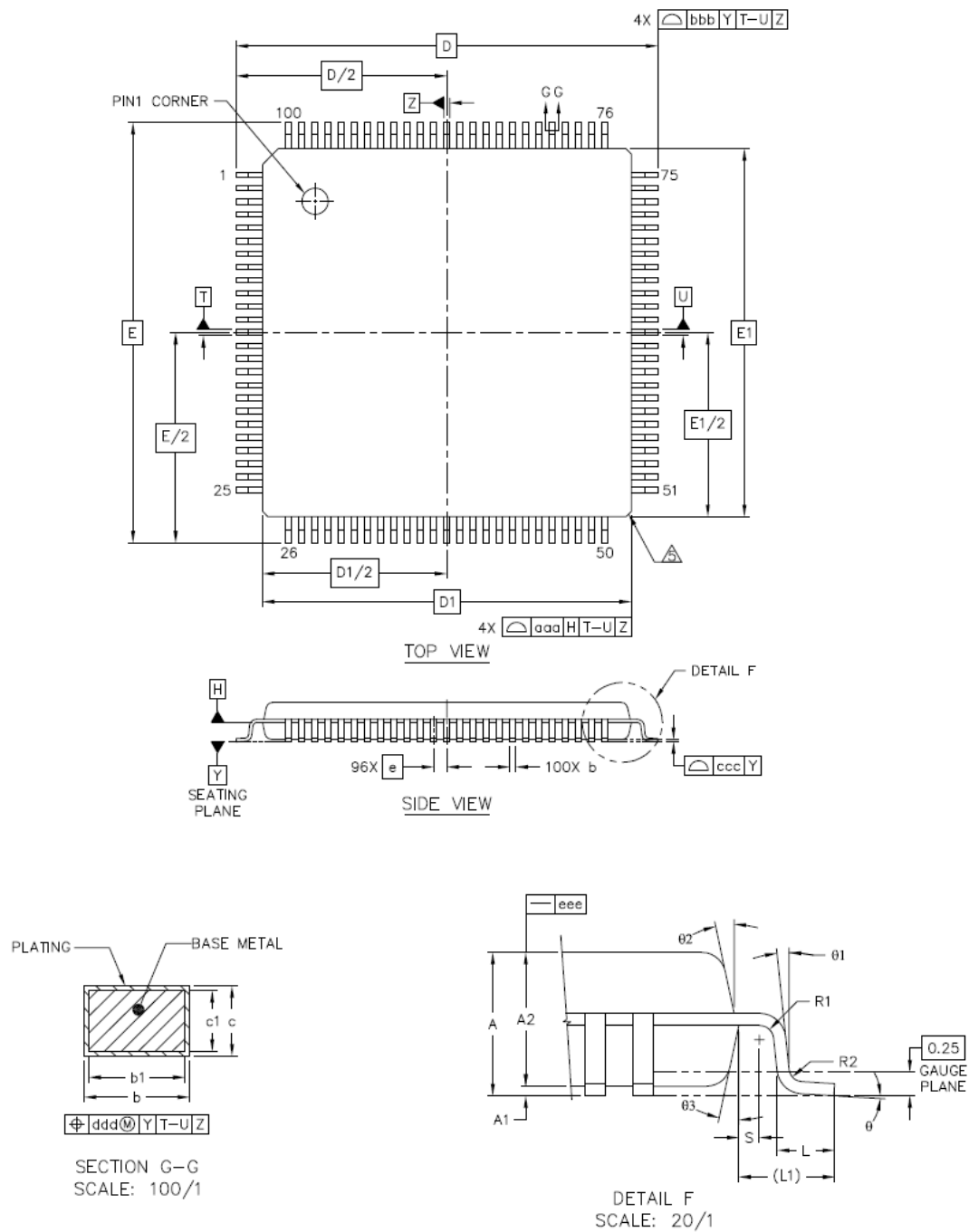


Figure 10.1. TQFP100 Package Drawing

## 12.2 QFN64 PCB Land Pattern

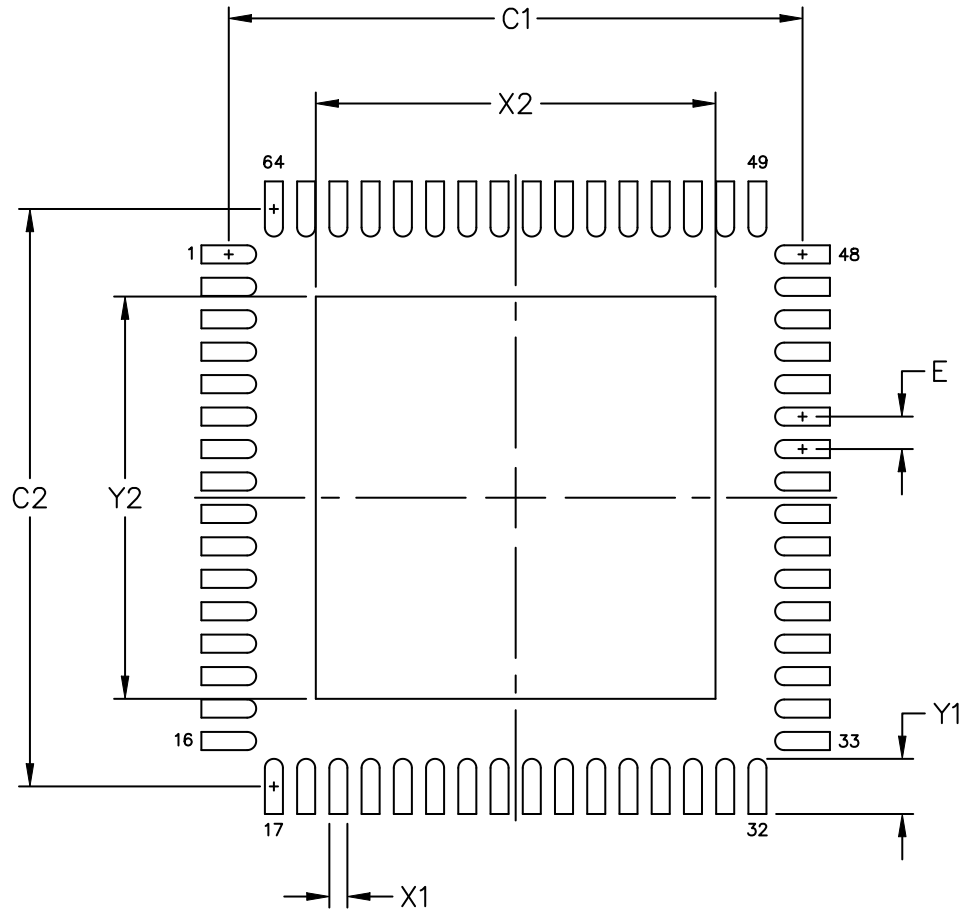


Figure 12.2. QFN64 PCB Land Pattern Drawing

## 13. Revision History

### Revision 0.6

March, 2018

- Removed "Confidential" watermark.
- Updated [4.1 Electrical Characteristics](#) and [4.2 Typical Performance Curves](#) with latest characterization data.

### Revision 0.2

October, 2017

- Updated memory maps to latest formatting and to include all peripherals.
- Updated all electrical specifications tables with latest characterization results.
- **Absolute Maximum Ratings** Table:
  - Removed redundant  $I_{VSSMAX}$  line.
  - Added footnote to clarify  $V_{DIGPIN}$  specification for 5V tolerant GPIO.
- **General Operating Conditions** Table:
  - Removed  $dV_{DD}$  specification and redundant footnote about shorting VREGVDD and AVDD together.
  - Added footnote about IOVDD voltage restriction when CSEN peripheral is used with chopping enabled.
- **Flash Memory Characteristics** Table: Added timing measurement clarification for Device Erase and Mass Erase.
- **Analog to Digital Converter (ADC)** Table:
  - Added header text for general specification conditions.
  - Added footnote for clarification of input voltage limits.
- Minor typographical corrections, including capitalization, mis-spellings and punctuation marks, throughout document.
- Minor formatting and styling updates, including table formats, TOC location, and boilerplate information throughout document.

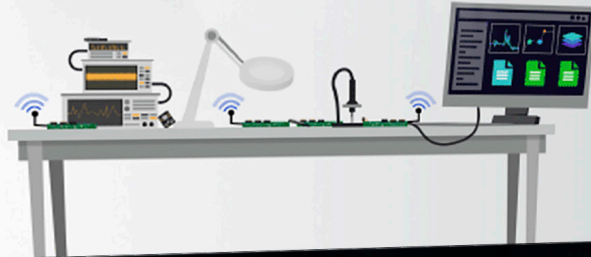
### Revision 0.1

April 27th, 2017

Initial release.

Silicon Labs

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