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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	95
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b820f2048gl120-ar

3. System Overview

3.1 Introduction

The Giant Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Giant Gecko Series 1 Reference Manual.

A block diagram of the Giant Gecko Series 1 family is shown in [Figure 3.1 Detailed EFM32GG11 Block Diagram on page 11](#). The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult [Ordering Information](#).

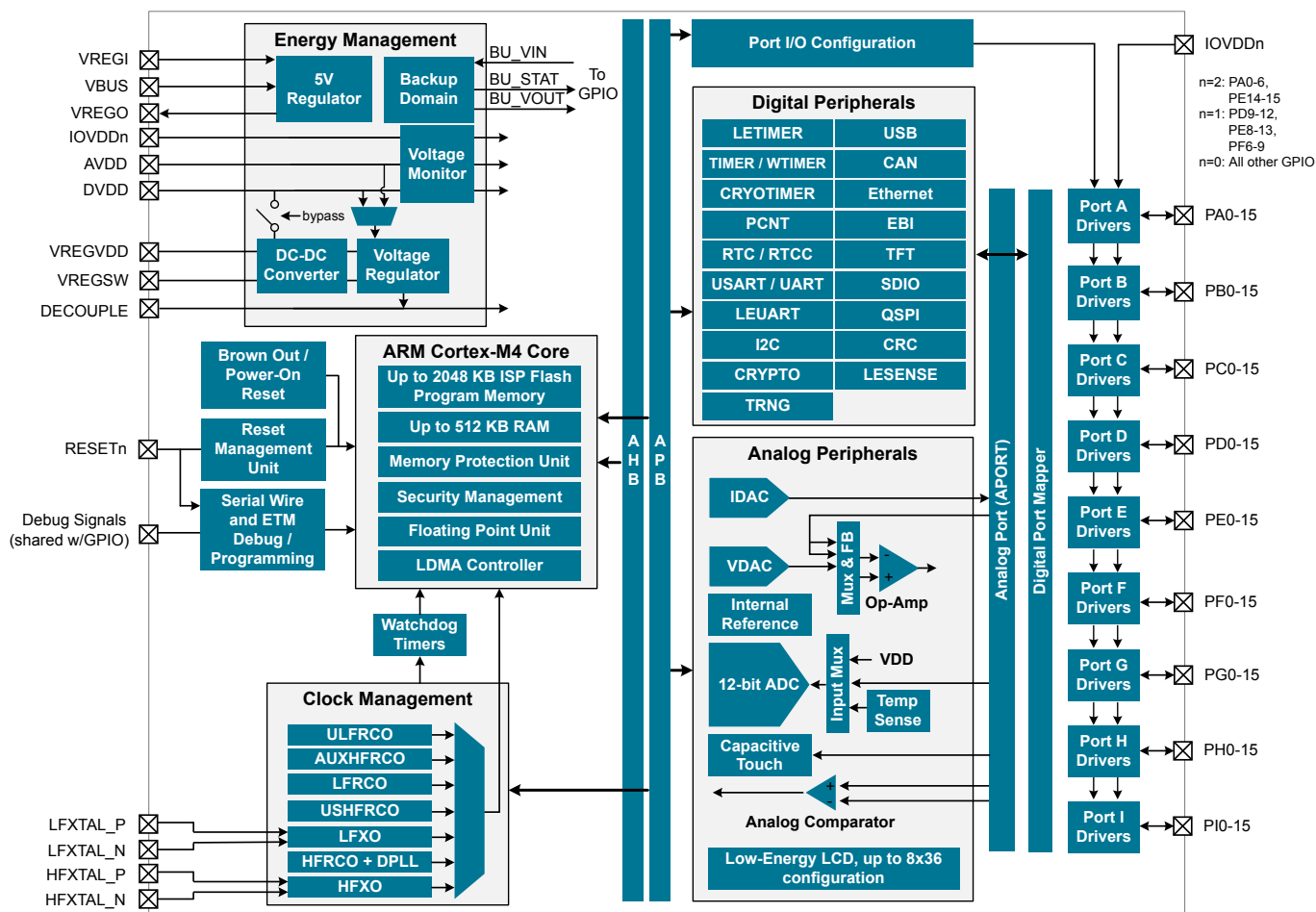


Figure 3.1. Detailed EFM32GG11 Block Diagram

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such as switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μA and 64 μA with several ranges consisting of various step sizes.

3.8.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksp/s, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.8 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x36 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32GG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor with FPU achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 2048 kB flash program memory
 - Dual-bank memory with read-while-write support
- Up to 512 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire or 4-pin JTAG debug interface

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode ³	I _{ACTIVE_LPM}	32 MHz HFRCO, CPU running while loop from flash	—	82	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	83	—	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	88	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	257	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode ¹	I _{ACTIVE_CCM_VS}	19 MHz HFRCO, CPU running while loop from flash	—	117	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1231	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode ³	I _{ACTIVE_LPM_VS}	19 MHz HFRCO, CPU running while loop from flash	—	72	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	219	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode ²	I _{EM1_DCM}	72 MHz HFRCO	—	42	—	μA/MHz
		50 MHz crystal	—	46	—	μA/MHz
		48 MHz HFRCO	—	46	—	μA/MHz
		32 MHz HFRCO	—	53	—	μA/MHz
		26 MHz HFRCO	—	57	—	μA/MHz
		16 MHz HFRCO	—	72	—	μA/MHz
		1 MHz HFRCO	—	663	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode ³	I _{EM1_LPM}	32 MHz HFRCO	—	42	—	μA/MHz
		26 MHz HFRCO	—	43	—	μA/MHz
		16 MHz HFRCO	—	48	—	μA/MHz
		1 MHz HFRCO	—	219	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode ²	I _{EM1_DCM_VS}	19 MHz HFRCO	—	60	—	μA/MHz
		1 MHz HFRCO	—	637	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode ³	I _{EM1_LPM_VS}	19 MHz HFRCO	—	39	—	μA/MHz
		1 MHz HFRCO	—	190	—	μA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode ³	I _{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	2.8	—	μA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	3.1	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO ⁵	—	2.1	—	μA
Current consumption in EM3 mode, with voltage scaling enabled	I _{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFR-CO	—	2.4	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	SNDR _{DAC}	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz	SNDR _{DAC_BAND}	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity ³	DNL _{DAC}		TBD	—	TBD	LSB
Integral non-linearity	INL _{DAC}		TBD	—	TBD	LSB
Offset error ⁵	V _{OFFSET}	T = 25 °C	TBD	—	TBD	mV
		Across operating temperature range	TBD	—	TBD	mV
Gain error ⁵	V _{GAIN}	T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	TBD	—	TBD	%
		Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	TBD	—	TBD	%
External load capacitance, OUTSCALE=0	C _{LOAD}		—	—	75	pF

RMII Receive Timing

Timing is specified with $3.0\text{ V} \leq \text{IOVDD} \leq 3.8\text{ V}$, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.45. Ethernet RMII Receive Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REF_CLK frequency	$F_{\text{REF_CLK}}$	Output slew rate set to 7	—	50	—	MHz
REF_CLK duty cycle	$DC_{\text{REF_CLK}}$		35	—	65	%
Setup time, RXD[1:0], CRS_DV, RX_ER valid to REF_CLK	t_{SU}		4	—	—	ns
Hold time, REF_CLK to RXD[1:0], CRS_DV, RX_ER change	t_{HD}		2	—	—	ns

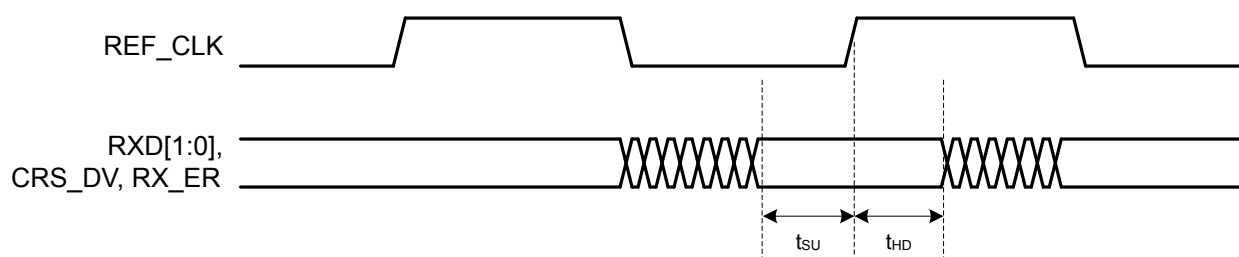


Figure 4.12. Ethernet RMII Receive Timing

4.1.28.2 QSPI DDR Mode

QSPI DDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 35, RX DLL = 70, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.56. QSPI DDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Half SCLK period	T/2	HFXO	$(1/F_{SCLK})^*$ 0.4 - 0.4	—	—	ns
		HFRCO, AUXHFRCO, USHFRCO	$(1/F_{SCLK})^*$ 0.44	—	—	ns
Output valid	t _{OV}		—	—	T/2 - 5.0	ns
Output hold	t _{OH}		T/2 - 39.4	—	—	ns
Input setup	t _{SU}		33.1	—	—	ns
Input hold	t _H		-0.9	—	—	ns

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VBUS	A13	USB VBUS signal and auxiliary input to 5 V regulator.	PF11	A14	GPIO (5V)
PF10	A15	GPIO (5V)	PF0	A16	GPIO (5V)
PA0	B1	GPIO	PD11	B2	GPIO
PD10	B3	GPIO	PD9	B4	GPIO
PF9	B5	GPIO	PF8	B6	GPIO
PF7	B7	GPIO	PF6	B8	GPIO
PI11	B9	GPIO (5V)	PI8	B10	GPIO (5V)
PF5	B11	GPIO	PF13	B12	GPIO (5V)
PF3	B13	GPIO	PF2	B14	GPIO
PF1	B15	GPIO (5V)	VREGO	B16	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PA1	C1	GPIO	PD12	C2	GPIO
PD14	C3	GPIO (5V)	PD13	C4	GPIO (5V)
PI15	C5	GPIO (5V)	PI14	C6	GPIO (5V)
PI13	C7	GPIO (5V)	PI12	C8	GPIO (5V)
PI10	C9	GPIO (5V)	PI7	C10	GPIO (5V)
PF15	C11	GPIO (5V)	PF12	C12	GPIO
PF4	C13	GPIO	PC15	C14	GPIO (5V)
PC14	C15	GPIO (5V)	VREGI	C16	Input to 5 V regulator.
PA2	D1	GPIO	PG0	D2	GPIO (5V)
PD15	D3	GPIO (5V)	PC13	D14	GPIO (5V)
PC12	D15	GPIO (5V)	PC11	D16	GPIO (5V)
PA3	E1	GPIO	PG2	E2	GPIO (5V)
PG1	E3	GPIO (5V)	PC10	E14	GPIO (5V)
PC9	E15	GPIO (5V)	PC8	E16	GPIO (5V)
PA4	F1	GPIO	PG4	F2	GPIO (5V)
PG3	F3	GPIO (5V)	IOVDD2	F6 G6	Digital IO power supply 2.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	M2	GPIO	PB3	M3	GPIO
PC6	M14	GPIO	VREGVSS	M15 N16	Voltage regulator VSS
VREGSW	M16	DCDC regulator switching node	PB4	N1	GPIO
PB5	N2	GPIO	PB6	N3	GPIO
PD5	N14	GPIO	PD4	N15	GPIO
PC0	P1	GPIO (5V)	PC1	P2	GPIO (5V)
PC2	P3	GPIO (5V)	PA8	P4	GPIO
PA11	P5	GPIO	PA13	P6	GPIO (5V)
PB9	P7	GPIO (5V)	PB12	P8	GPIO
PH2	P9	GPIO (5V)	PH5	P10	GPIO
PH8	P11	GPIO (5V)	PH11	P12	GPIO (5V)
PH13	P13	GPIO (5V)	PD0	P14	GPIO (5V)
PD3	P15	GPIO	PD8	P16	GPIO
PB7	R1	GPIO	PC3	R2	GPIO (5V)
PC5	R3	GPIO	PA9	R4	GPIO
BODEN	R5	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	RESETn	R6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB10	R7	GPIO (5V)	PH0	R8	GPIO (5V)
PH3	R9	GPIO (5V)	PH6	R10	GPIO
PH9	R11	GPIO (5V)	PH12	R12	GPIO (5V)
PH14	R13	GPIO (5V)	PH15	R14	GPIO (5V)
PD2	R15	GPIO (5V)	PD7	R16	GPIO
PB8	T1	GPIO	PC4	T2	GPIO
PA7	T3	GPIO	PA10	T4	GPIO
PA12	T5	GPIO (5V)	PA14	T6	GPIO
PB11	T7	GPIO	PH1	T8	GPIO (5V)
PH4	T9	GPIO	PH7	T10	GPIO (5V)
PH10	T11	GPIO (5V)	PB13	T12	GPIO
PB14	T13	GPIO	AVDD	T14	Analog power supply.
PD1	T15	GPIO	PD6	T16	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF3	B9	GPIO
PF1	B10	GPIO (5V)	PF12	B11	GPIO
VBUS	B12	USB VBUS signal and auxiliary input to 5 V regulator.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 K12 L12 L13 M8 M11 N8	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L14	Digital IO power supply 0.
PF0	C10	GPIO (5V)	PE4	C11	GPIO
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PE5	D11	GPIO
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PE6	E11	GPIO
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE7	F11	GPIO
PC8	F12	GPIO (5V)	PC9	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE0	G11	GPIO (5V)
PE1	G12	GPIO (5V)	PE3	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
PC7	H13	GPIO	PD14	J1	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO (5V)
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	VREGI	45	Input to 5 V regulator.
VREGO	46	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs	PF10	47	GPIO (5V)
PF11	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.19 EFM32GG11B1xx in QFN64 Device Pinout

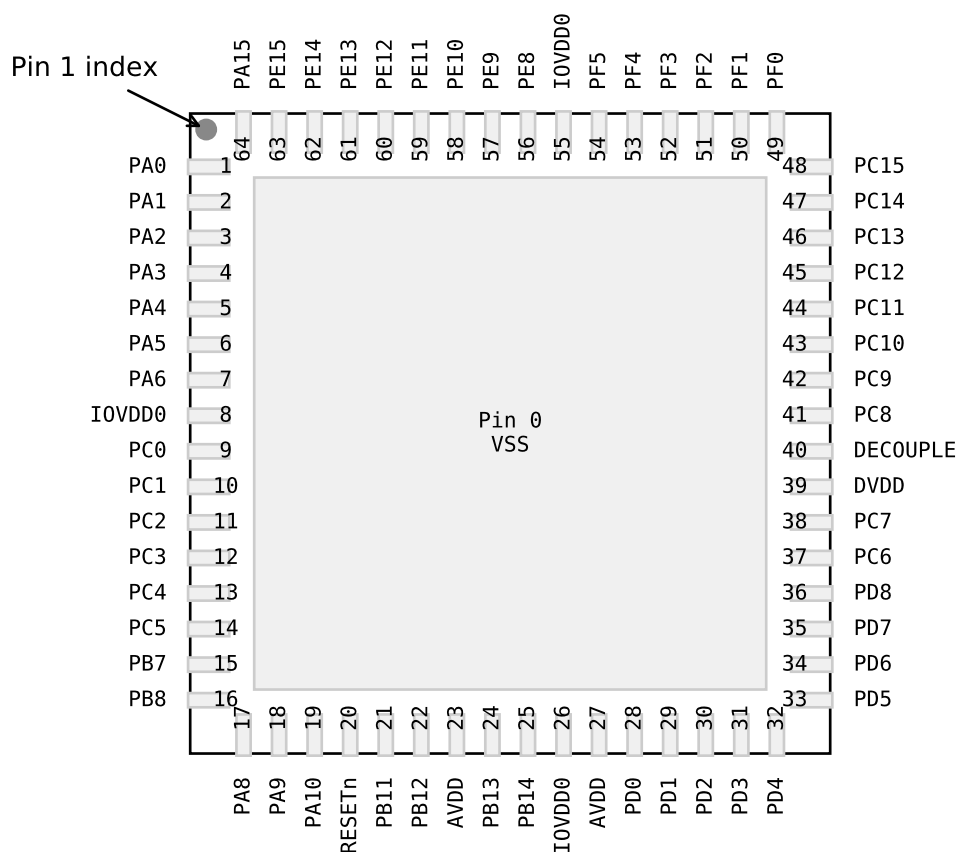


Figure 5.19. EFM32GG11B1xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.19. EFM32GG11B1xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PC0	9	GPIO (5V)
PC1	10	GPIO (5V)	PC2	11	GPIO (5V)

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.
LES_CH0	0: PC0		LESENSE channel 0.
LES_CH1	0: PC1		LESENSE channel 1.
LES_CH2	0: PC2		LESENSE channel 2.
LES_CH3	0: PC3		LESENSE channel 3.
LES_CH4	0: PC4		LESENSE channel 4.
LES_CH5	0: PC5		LESENSE channel 5.
LES_CH6	0: PC6		LESENSE channel 6.
LES_CH7	0: PC7		LESENSE channel 7.
LES_CH8	0: PC8		LESENSE channel 8.
LES_CH9	0: PC9		LESENSE channel 9.
LES_CH10	0: PC10		LESENSE channel 10.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PCNT0_S0IN	0: PC13 1: PE0 2: PC0 3: PD6	4: PA0 5: PB0 6: PB5 7: PB12	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PC14 1: PE1 2: PC1 3: PD7	4: PA1 5: PB1 6: PB6 7: PB11	Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	0: PA5 1: PB3 2: PD15 3: PC4	4: PA7 5: PA12 6: PB11 7: PG14	Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	0: PA6 1: PB4 2: PB0 3: PC5	4: PA8 5: PA13 6: PB12 7: PG15	Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	0: PD0 1: PE8 2: PB13 3: PF10	4: PC12 5: PI2 6: PI0 7: PH14	Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	0: PD1 1: PE9 2: PB14 3: PF11	4: PC13 5: PI1 6: PH15 7: PH13	Pulse Counter PCNT2 input number 1.
PRS_CH0	0: PA0 1: PF3 2: PC14 3: PF2		Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PA1 1: PF4 2: PC15 3: PE12		Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PC0 1: PF5 2: PE10 3: PE13		Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PC1 1: PE8 2: PE11 3: PA0		Peripheral Reflex System PRS, channel 3.
PRS_CH4	0: PC8 1: PB0 2: PF1		Peripheral Reflex System PRS, channel 4.
PRS_CH5	0: PC9 1: PB1 2: PD6		Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA6 1: PB14 2: PE6		Peripheral Reflex System PRS, channel 6.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US1_CTS	0: PB9 1: PD4 2: PF3 3: PC6	4: PC12 5: PB13 6: PH2	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PB10 1: PD5 2: PF4 3: PC7	4: PC13 5: PB14 6: PH3	USART1 Request To Send hardware flow control output.
US1_RX	0: PC1 1: PD1 2: PD6 3: PF7	4: PC2 5: PA0 6: PA2	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PC0 1: PD0 2: PD7 3: PF6	4: PC1 5: PF2 6: PA14	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	0: PC4 1: PB5 2: PA9 3: PA15	4: PF8 5: PF2	USART2 clock input / output.
US2_CS	0: PC5 1: PB6 2: PA10 3: PB11	4: PF9 5: PF5	USART2 chip select input / output.
US2_CTS	0: PC1 1: PB12 2: PA11 3: PB10	4: PC12 5: PD6	USART2 Clear To Send hardware flow control input.
US2_RTS	0: PC0 1: PB15 2: PA12 3: PC14	4: PC13 5: PD8	USART2 Request To Send hardware flow control output.
US2_RX	0: PC3 1: PB4 2: PA8 3: PA14	4: PF7 5: PF1	USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	0: PC2 1: PB3 2: PA7 3: PA13	4: PF6 5: PF0	USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
US3_CLK	0: PA2 1: PD7 2: PD4 3: PG8	4: PG2 5: PI14	USART3 clock input / output.
US3_CS	0: PA3 1: PE4 2: PC14 3: PC0	4: PG3 5: PI15	USART3 chip select input / output.
US3_CTS	0: PA4 1: PE5 2: PD6 3: PG10	4: PG4 5: PG9	USART3 Clear To Send hardware flow control input.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US3_RTS	0: PA5 1: PC1 2: PA14 3: PC15	4: PG5 5: PG11	USART3 Request To Send hardware flow control output.
US3_RX	0: PA1 1: PE7 2: PB7 3: PG7	4: PG1 5: PI13	USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PA0 1: PE6 2: PB3 3: PG6	4: PG0 5: PI12	USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI).
US4_CLK	0: PC4 1: PD11 2: PI2 3: PI8	4: PH6	USART4 clock input / output.
US4_CS	0: PC5 1: PD12 2: PI3 3: PI9	4: PH7	USART4 chip select input / output.
US4_CTS	0: PA7 1: PD13 2: PI4 3: PI10	4: PH8	USART4 Clear To Send hardware flow control input.
US4_RTS	0: PA8 1: PD14 2: PI5 3: PI11	4: PH9	USART4 Request To Send hardware flow control output.
US4_RX	0: PB8 1: PD10 2: PI1 3: PI7	4: PH5	USART4 Asynchronous Receive. USART4 Synchronous mode Master Input / Slave Output (MISO).
US4_TX	0: PB7 1: PD9 2: PI0 3: PI6	4: PH4	USART4 Asynchronous Transmit. Also used as receive input in half duplex communication. USART4 Synchronous mode Master Output / Slave Input (MOSI).
US5_CLK	0: PB11 1: PD13 2: PF13 3: PH12		USART5 clock input / output.
US5_CS	0: PB13 1: PD14 2: PF12 3: PH13		USART5 chip select input / output.
US5_CTS	0: PB14 1: PD15 2: PF11 3: PH14		USART5 Clear To Send hardware flow control input.
US5_RTS	0: PB12 1: PB15 2: PF10 3: PH15		USART5 Request To Send hardware flow control output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US5_RX	0: PE9 1: PA7 2: PB1 3: PH11		USART5 Asynchronous Receive. USART5 Synchronous mode Master Input / Slave Output (MISO).
US5_TX	0: PE8 1: PA6 2: PF15 3: PH10		USART5 Asynchronous Transmit. Also used as receive input in half duplex communication. USART5 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	0: PF10		USB D- pin.
USB_DP	0: PF11		USB D+ pin.
USB_ID	0: PF12		USB ID pin.
USB_VBUSEN	0: PF5		USB 5 V VBUS enable.
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6 2: PG2 3: PG8	4: PC15 5: PB0 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5 1: PD13 2: PG3 3: PG9	4: PF0 5: PB1 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM3_CC2	0: PD11 1: PC10 2: PC13 3: PF11	4: PI5 5: PF6 6: PF12 7: PF15	Wide timer 3 Capture Compare input / output channel 2.

Certain alternate function locations may have non-interference priority. These locations will take precedence over any other functions selected on that pin (i.e. another alternate function enabled to the same pin inadvertently).

Some alternate functions may also have high speed priority on certain locations. These locations ensure the fastest possible paths to the pins for timing-critical signals.

The following table lists the alternate functions and locations with special priority.

Table 5.22. Alternate Functionality Priority

Alternate Functionality	Location	Priority
CMU_CLK2	1: PA3 5: PD10	High Speed High Speed
CMU_CLKI0	1: PA3 5: PD10	High Speed High Speed
ETH_RMIICRSOV	0: PA4 1: PD11	High Speed High Speed
ETH_RMIREFCLK	0: PA3 1: PD10	High Speed High Speed
ETH_RMIIRXD0	0: PA2 1: PD9	High Speed High Speed
ETH_RMIIRXD1	0: PA1 1: PF9	High Speed High Speed
ETH_RMIIRXER	0: PA5 1: PD12	High Speed High Speed
ETH_RMIITXD0	0: PE15 1: PF7	High Speed High Speed
ETH_RMIITXD1	0: PE14 1: PF6	High Speed High Speed
ETH_RMIITXEN	0: PA0 1: PF8	High Speed High Speed
QSPI0_CS0	0: PF7	High Speed
QSPI0_CS1	0: PF8	High Speed
QSPI0_DQ0	0: PD9	High Speed
QSPI0_DQ1	0: PD10	High Speed
QSPI0_DQ2	0: PD11	High Speed
QSPI0_DQ3	0: PD12	High Speed
QSPI0_DQ4	0: PE8	High Speed
QSPI0_DQ5	0: PE9	High Speed
QSPI0_DQ6	0: PE10	High Speed
QSPI0_DQ7	0: PE11	High Speed

Table 11.1. TQFP64 Package Dimensions

Dimension	Min	Typ	Max
A	—	1.15	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
θ	0	3.5	7
Θ1	0	—	0.10
Θ2	11	12	13
Θ3	11	12	13
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. 3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			

Table 12.2. QFN64 PCB Land Pattern Dimensions

Dimension	Typ
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	7.30
Y2	7.30

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch can be used for the center ground pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.