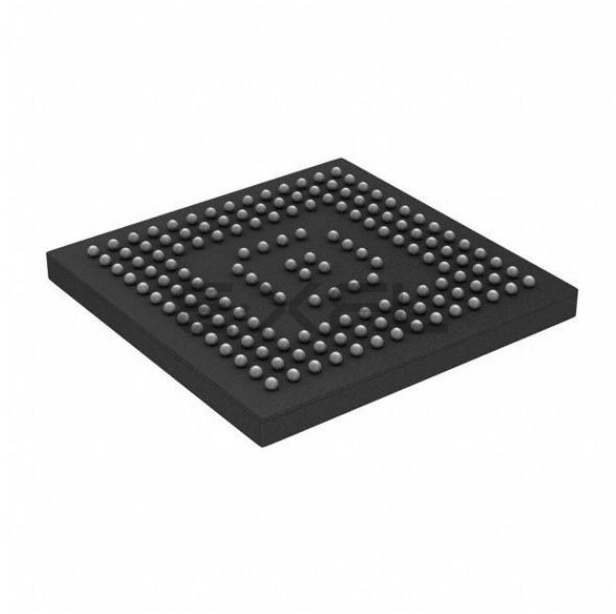

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	152-VFBGA
Supplier Device Package	152-BGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b820f2048gl152-a

4.1.7.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.9. Current Consumption 1.8 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	72 MHz HFRCO, CPU running Prime from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	140	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	122	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	122	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	126	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	131	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	315	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	107	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	259	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	72 MHz HFRCO	—	57	—	µA/MHz
		50 MHz crystal	—	59	—	µA/MHz
		48 MHz HFRCO	—	59	—	µA/MHz
		32 MHz HFRCO	—	61	—	µA/MHz
		26 MHz HFRCO	—	63	—	µA/MHz
		16 MHz HFRCO	—	68	—	µA/MHz
		1 MHz HFRCO	—	252	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	55	—	µA/MHz
		1 MHz HFRCO	—	207	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.7	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	4.0	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.5	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis (V_{CM} = 1.25 V, BIASPROG[4] = 0x10, FULLBIAS[4] = 1)	$V_{ACMPHYST}$	HYSTSEL[5] = HYST0	TBD	0	TBD	mV
		HYSTSEL[5] = HYST1	TBD	18	TBD	mV
		HYSTSEL[5] = HYST2	TBD	33	TBD	mV
		HYSTSEL[5] = HYST3	TBD	46	TBD	mV
		HYSTSEL[5] = HYST4	TBD	57	TBD	mV
		HYSTSEL[5] = HYST5	TBD	68	TBD	mV
		HYSTSEL[5] = HYST6	TBD	79	TBD	mV
		HYSTSEL[5] = HYST7	TBD	90	TBD	mV
		HYSTSEL[5] = HYST8	TBD	0	TBD	mV
		HYSTSEL[5] = HYST9	TBD	-18	TBD	mV
		HYSTSEL[5] = HYST10	TBD	-33	TBD	mV
		HYSTSEL[5] = HYST11	TBD	-45	TBD	mV
		HYSTSEL[5] = HYST12	TBD	-57	TBD	mV
		HYSTSEL[5] = HYST13	TBD	-67	TBD	mV
		HYSTSEL[5] = HYST14	TBD	-78	TBD	mV
		HYSTSEL[5] = HYST15	TBD	-88	TBD	mV
Comparator delay[3]	$t_{ACMPDELAY}$	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	30	—	µs
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	3.7	—	µs
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	360	—	ns
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[4] =0x10, FULLBIAS[4] = 1	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	infinite	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	100	—	kΩ
		CSRESSEL[6] = 6	—	162	—	kΩ
		CSRESSEL[6] = 7	—	235	—	kΩ

SPI Slave Timing

Table 4.35. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		6 * $t_{HFPERCLK}$	—	—	ns
SCLK high time [1] [3] [2]	t_{SCLK_HI}		2.5 * $t_{HFPERCLK}$	—	—	ns
SCLK low time [1] [3] [2]	t_{SCLK_LO}		2.5 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [3]	$t_{CS\_ACT\_MI}$		24	—	69	ns
CS disable to MISO [1] [3]	$t_{CS\_DIS\_MI}$		19	—	175	ns
MOSI setup time [1] [3]	t_{SU_MO}		7	—	—	ns
MOSI hold time [1] [3] [2]	t_{H_MO}		6	—	—	ns
SCLK to MISO [1] [3] [2]	t_{SCLK_MI}		16 + 1.5 * $t_{HFPERCLK}$	—	43 + 2.5 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

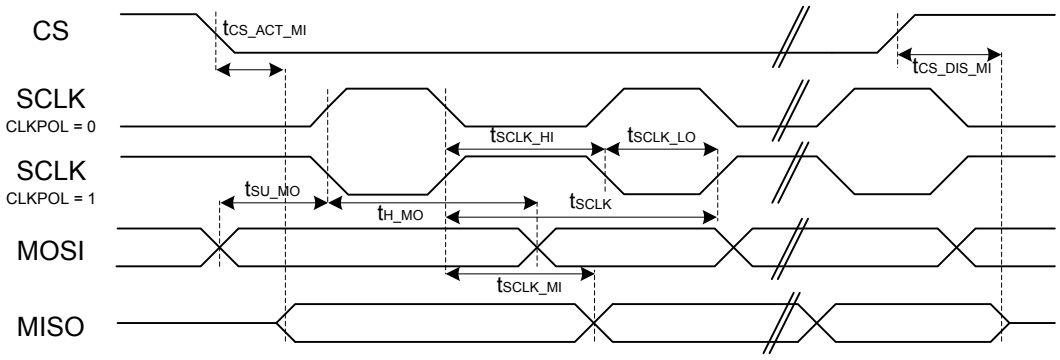

Figure 4.2. SPI Slave Timing Diagram

SDIO SDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.48. SDIO SDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		0.99	4.68	—	ns
Clock fall time	t_F		0.90	3.64	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}		8	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}		1.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}		0	—	35	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}		0.8	—	—	ns

SDIO MMC DDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Table 4.52. SDIO MMC DDR Mode Timing (Location 0, 1.8V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	18	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	25.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	25.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.13	5.21	—	ns
Clock fall time	t_F		1.01	4.10	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		3	—	—	ns
Input setup time, DAT[0:7] valid to SD_CLK	t_{ISU2X}		5.3	—	—	ns
Input hold time, SD_CLK to DAT[0:7] change	t_{IH2X}		2.5	—	—	ns
Output delay time, SD_CLK to DAT[0:7] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:7] change	t_{OH2X}		3	—	—	ns

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

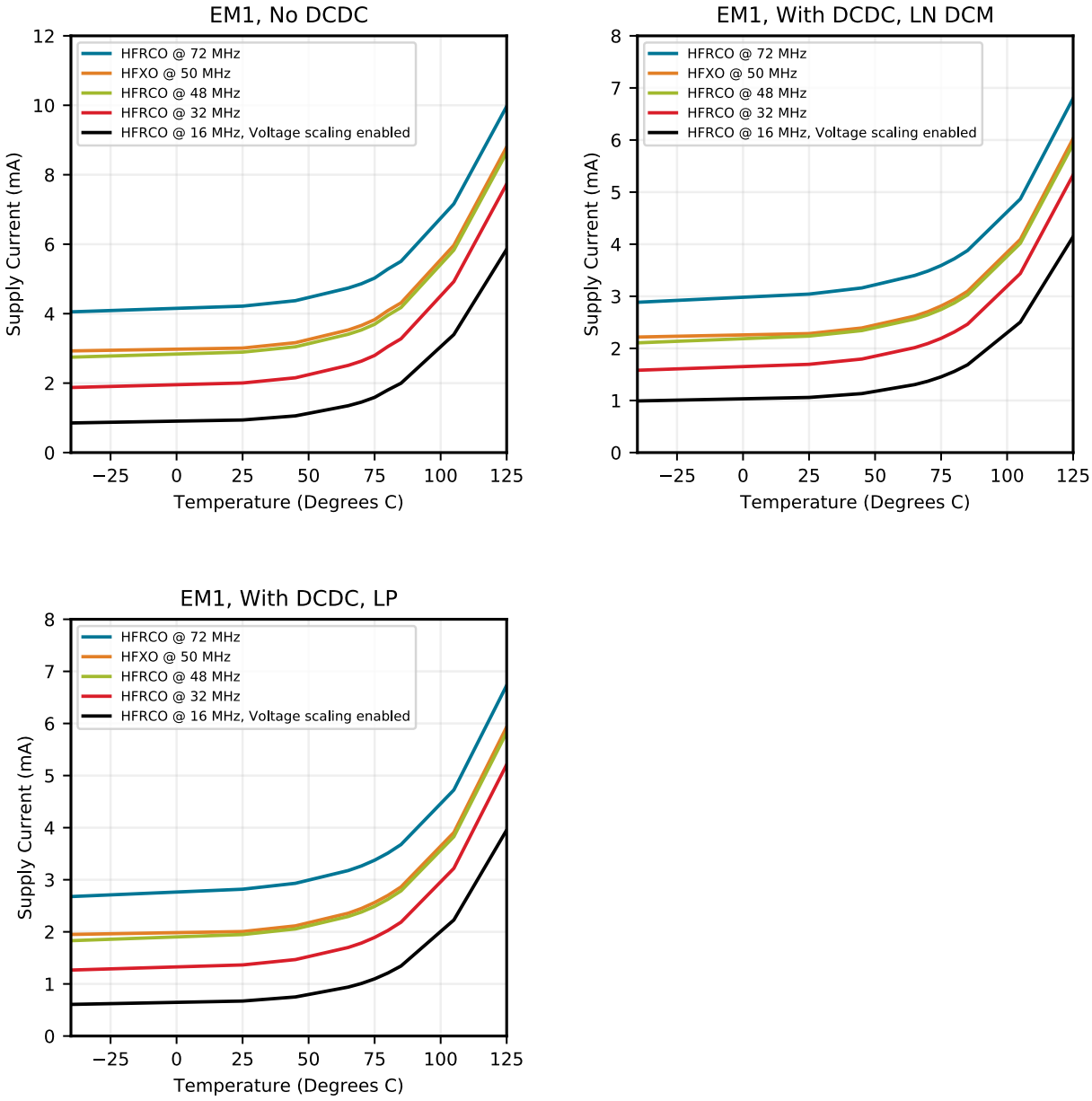

Figure 4.25. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD15	J2	GPIO (5V)	PC6	J12	GPIO
DECOUPLE	J13	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC0	K1	GPIO (5V)
PC1	K2	GPIO (5V)	PD8	K13	GPIO
PC2	L1	GPIO (5V)	PC3	L2	GPIO (5V)
PA7	L3	GPIO	PB9	L15	GPIO (5V)
PB10	L16	GPIO (5V)	PD0	L17	GPIO (5V)
PD1	L18	GPIO	PD4	L19	GPIO
PD7	L20	GPIO	PB7	M1	GPIO
PC4	M2	GPIO	PA8	M3	GPIO
PA10	M4	GPIO	PA13	M5	GPIO (5V)
PA14	M6	GPIO	RESETn	M7	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	M9 M10 N11	Analog power supply.	PD3	M12	GPIO
PD6	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	PB12	N7	GPIO
PB13	N9	GPIO	PB14	N10	GPIO
PD2	N12	GPIO (5V)	PD5	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.11 EFM32GG11B3xx in QFP100 Device Pinout

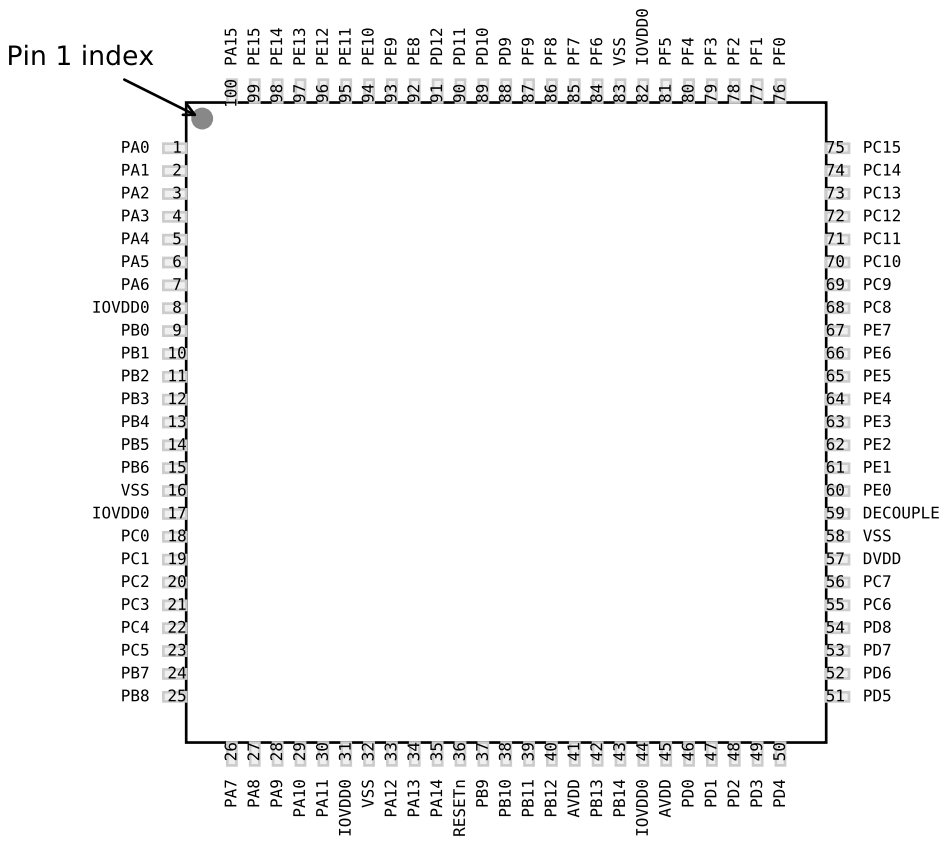

Figure 5.11. EFM32GG11B3xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.11. EFM32GG11B3xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PB0	BUSBY BUSAX LCD_SEG32	EBI_AD00 #1 EBI_CS0 #3 EBI_A16 #0	TIM2_CDTI0 #0 TIM1_CC0 #2 TIM3_CC2 #7 WTIM0_CC0 #5 PCNT0_S0IN #5 PCNT1_S1IN #2	LEU1_TX #3	PRS_CH4 #1 ACMP0_O #5
PE0	BUSDY BUSCX	EBI_A00 #2 EBI_A07 #0	TIM3_CC0 #1 WTIM1_CC1 #3 PCNT0_S0IN #1	CAN0_RX #6 U0_TX #1 I2C1_SDA #2	PRS_CH22 #1 ACMP2_O #1
PC7	BUSACMP0Y BUSACMP0X OPA3_N	EBI_A06 #0 EBI_A13 #1 EBI_A21 #3	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 LEU1_RX #0 I2C0_SCL #2	LES_CH7 PRS_CH15 #1 ETM_TD0 #2
PB1	BUSAY BUSBX LCD_SEG33	EBI_AD01 #1 EBI_CS1 #3 EBI_A17 #0	TIM2_CDTI1 #0 TIM1_CC1 #2 WTIM0_CC1 #5 LE-TIM1_OUT1 #5 PCNT0_S1IN #5	ETH_MIICRS #0 US5_RX #2 LEU1_RX #3	PRS_CH5 #1
PB2	BUSBY BUSAX LCD_SEG34	EBI_AD02 #1 EBI_CS2 #3 EBI_A18 #0	TIM2_CDTI2 #0 TIM1_CC2 #2 WTIM0_CC2 #5 LE-TIM1_OUT0 #5	ETH_MIICOL #0 US1_CS #6	PRS_CH18 #0 ACMP0_O #6
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	EBI_AD03 #1 EBI_CS3 #3 EBI_A19 #0	TIM1_CC3 #2 WTIM0_CC0 #6 PCNT1_S0IN #1	ETH_MIICRS #2 ETH_MDIO #0 SDIO_DAT6 #1 US2_TX #1 US3_TX #2 QSPI0_DQ4 #1	PRS_CH19 #0 ACMP0_O #7
PC6	BUSACMP0Y BUSACMP0X OPA3_P	EBI_A05 #0	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 LEU1_TX #0 I2C0_SDA #2	LES_CH6 PRS_CH14 #1 ETM_TCLK #2
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	EBI_AD04 #1 EBI_ARDY #3 EBI_A20 #0	WTIM0_CC1 #6 PCNT1_S1IN #1	ETH_MIICOL #2 ETH_MDC #0 SDIO_DAT7 #1 US2_RX #1 QSPI0_DQ5 #1 LEU1_TX #4	PRS_CH20 #0
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	EBI_AD05 #1 EBI_ALE #3 EBI_A21 #0	WTIM0_CC2 #6 LE-TIM1_OUT0 #4 PCNT0_S0IN #6	ETH_TSUEXTCLK #0 US0_RTS #4 US2_CLK #1 QSPI0_DQ6 #1 LEU1_RX #4	PRS_CH21 #0
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	EBI_AD06 #1 EBI_WEn #3 EBI_A22 #0	TIM0_CC0 #3 TIM2_CC0 #4 WTIM3_CC0 #6 LE-TIM1_OUT1 #4 PCNT0_S1IN #6	ETH_TSUTMRTOG #0 US0_CTS #4 US2_CS #1 QSPI0_DQ7 #1	PRS_CH12 #1
PD5	BUSADC0Y BUSADC0X OPA2_OUT	EBI_A09 #1 EBI_A18 #3	TIM6_CC1 #7 WTIM0_CDTI1 #4 WTIM1_CC3 #1 WTIM2_CC2 #5	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3	PRS_CH11 #2 ETM_TD3 #0 ETM_TD3 #2

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD4	BUSADC0Y BUSADC0X OPA2_P	EBI_A08 #1 EBI_A17 #3	TIM6_CC0 #7 WTIM0_CDTI0 #4 WTIM1_CC2 #1 WTIM2_CC1 #5	CAN1_TX #2 US1_CTS #1 US3_CLK #2 LEU0_TX #0 I2C1_SDA #3	CMU_CLKI0 #0 PRS_CH10 #2 ETM_TD2 #0 ETM_TD2 #2
PC0	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSACMP0Y BUSACMP0X	EBI_AD07 #1 EBI_CS0 #2 EBI_REn #3 EBI_A23 #0	TIM0_CC1 #3 TIM2_CC1 #4 PCNT0_S0IN #2	ETH_MDIO #2 CAN0_RX #0 US0_TX #5 US1_TX #0 US1_CS #4 US2_RTS #0 US3_CS #3 I2C0_SDA #4	LES_CH0 PRS_CH2 #0
PC1	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSACMP0Y BUSACMP0X	EBI_AD08 #1 EBI_CS1 #2 EBI_BL0 #3 EBI_A24 #0	TIM0_CC2 #3 TIM2_CC2 #4 WTIM0_CC0 #7 PCNT0_S1IN #2	ETH_MDC #2 CAN0_TX #0 US0_RX #5 US1_TX #4 US1_RX #0 US2_CTS #0 US3_RTS #1 I2C0_SCL #4	LES_CH1 PRS_CH3 #0
PC2	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSACMP0Y BUSACMP0X	EBI_AD09 #1 EBI_CS2 #2 EBI_NANDWEn #3 EBI_A25 #0	TIM0_CDTI0 #3 TIM2_CC0 #5 WTIM0_CC1 #7 LETIM1_OUT0 #3	ETH_TSUEXTCLK #2 CAN1_RX #0 US1_RX #4 US2_TX #0	LES_CH2 PRS_CH10 #1
PA8	BUSBY BUSAX LCD_SEG36	EBI_AD14 #1 EBI_A02 #3 EBI_DCLK #0	TIM2_CC0 #0 TIM0_CC0 #6 LETIM0_OUT0 #6 PCNT1_S1IN #4	US2_RX #2 US4_RTS #0	PRS_CH8 #0
PA11	BUSAY BUSBX LCD_SEG39	EBI_CS1 #1 EBI_A05 #3 EBI_HSNC #0	WTIM2_CC2 #0 LETIM1_OUT0 #1	US2_CTS #2	PRS_CH11 #0
PA13	BUSAY BUSBX	EBI_WEn #1 EBI_NANDWEn #2 EBI_A01 #0 EBI_A07 #3	TIM0_CC2 #7 TIM2_CC1 #1 WTIM0_CDTI1 #2 WTIM2_CC1 #1 LETIM1_OUT1 #1 PCNT1_S1IN #5	CAN1_TX #5 US0_CS #5 US2_TX #3	PRS_CH13 #0
PB9	BUSAY BUSBX	EBI_ALE #1 EBI_NANDREn #2 EBI_A00 #1 EBI_A03 #0 EBI_A09 #3	WTIM2_CC0 #2 LETIM0_OUT0 #7	SDIO_WP #3 CAN0_RX #3 US1_CTS #0 U1_TX #2	PRS_CH13 #1 ACMP1_O #5
PB12	BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT	EBI_A03 #1 EBI_A12 #3 EBI_CSTFT #2	TIM1_CC3 #3 WTIM2_CC0 #3 LETIM0_OUT1 #1 PCNT0_S0IN #7 PCNT1_S1IN #6	US2_CTS #1 US5_RTS #0 U1_RTS #2 I2C1_SCL #1	PRS_CH16 #1
PH2	BUSADC1Y BUSADC1X	EBI_VSNC #2	TIM6_CC0 #3	US1_CTS #6	
PH5	BUSADC1Y BUSADC1X	EBI_A17 #2	TIM6_CDTI0 #3 WTIM2_CC1 #6	US4_RX #4	
PH8	BUSACMP3Y BUSACMP3X	EBI_A20 #2	TIM6_CC0 #4 WTIM1_CC0 #6 WTIM2_CC1 #7	US4_CTS #4	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PH11	BUSACMP3Y BUSACMP3X	EBI_A23 #2	TIM5_CC1 #1 WTIM1_CC3 #6	US5_RX #3 U1_TX #5 I2C1_SDA #5	
PH13	BUSACMP3Y BUSACMP3X	EBI_A25 #2	TIM5_CC0 #2 WTIM1_CC1 #7 PCNT2_S1IN #7	US5_CS #3 U1_CTS #5 I2C1_SDA #6	
PD0	VDAC0_OUT0ALT / OPA0_OUTALT #4 OPA2_OUTALT BUSADC0Y BUSADC0X	EBI_A04 #1 EBI_A13 #3	TIM4_CDTI0 TIM6_CC2 #5 WTIM1_CC2 #0 PCNT2_S0IN #0	CAN0_RX #2 US1_TX #1	
PD3	BUSADC0Y BUSADC0X OPA2_N	EBI_A07 #1 EBI_A16 #3	TIM4_CDTI2 TIM0_CC2 #2 TIM6_CC2 #6 WTIM1_CC1 #1 WTIM2_CC0 #5	CAN1_RX #2 US1_CS #1 LEU1_RX #2	ETM_TD1 #0 ETM_TD1 #2
PD8	BU_VIN	EBI_A12 #1	WTIM1_CC2 #2	US2_RTS #5	CMU_CLK1 #1 PRS_CH12 #2 ACMP2_O #0
PB7	LFXTAL_P		TIM0_CDTI0 #4 TIM1_CC0 #3	US0_TX #4 US1_CLK #0 US3_RX #2 US4_TX #0 U0_CTS #4	PRS_CH22 #0
PC3	VDAC0_OUT0ALT / OPA0_OUTALT #3 BUSACMP0Y BUSACMP0X	EBI_AD10 #1 EBI_CS3 #2 EBI_BL1 #3 EBI_NANDREn #0	TIM0_CDTI1 #3 TIM2_CC1 #5 WTIM0_CC2 #7 LETIM1_OUT1 #3	ETH_TSUTMRTOG #2 CAN1_TX #0 US1_CLK #4 US2_RX #0	LES_CH3 PRS_CH11 #1
PC5	BUSACMP0Y BUSACMP0X OPA0_N	EBI_AD12 #1 EBI_WEn #2 EBI_NANDWEn #0 EBI_A00 #3	TIM0_CC1 #5 LETIM0_OUT1 #3 PCNT1_S1IN #3	SDIO_WP #1 US2_CS #0 US4_CS #0 U0_RX #4 U1_RTS #4 I2C1_SCL #0	LES_CH5 PRS_CH19 #2
PA9	BUSAY BUSBX LCD_SEG37	EBI_AD15 #1 EBI_A03 #3 EBI_DTEN #0	TIM2_CC1 #0 TIM0_CC1 #6 WTIM2_CC0 #0 LETIM0_OUT1 #6	US2_CLK #2	PRS_CH9 #0
PB10	BUSBY BUSAX	EBI_BL0 #2 EBI_A01 #1 EBI_A04 #0 EBI_A10 #3	WTIM2_CC1 #2 LETIM0_OUT1 #7	SDIO_CD #3 CAN0_TX #3 US1_RTS #0 US2_CTS #3 U1_RX #2	PRS_CH9 #2 ACMP1_O #6
PH0	BUSADC1Y BUSADC1X	EBI_DCLK #2	WTIM2_CC2 #4	US0_CTS #6 LEU1_TX #5	
PH3	BUSADC1Y BUSADC1X	EBI_HSNC #2	TIM6_CC1 #3	US1_RTS #6	
PH6	BUSADC1Y BUSADC1X	EBI_A18 #2	TIM6_CDTI1 #3 WTIM2_CC2 #6	US4_CLK #4	
PH9	BUSACMP3Y BUSACMP3X	EBI_A21 #2	TIM6_CC1 #4 WTIM1_CC1 #6 WTIM2_CC2 #7	US4_RTS #4	
PH12	BUSACMP3Y BUSACMP3X	EBI_A24 #2	TIM5_CC2 #1 WTIM1_CC0 #7	US5_CLK #3 U1_RX #5 I2C1_SCL #5	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_TSUTMR-TOG	0: PB6 1: PB15 2: PC3 3: PF9		Ethernet IEEE1588 Timer Toggle.
ETM_TCLK	0: PD7 1: PF8 2: PC6 3: PA6	4: PE11 5: PG15	Embedded Trace Module ETM clock .
ETM_TD0	0: PD6 1: PF9 2: PC7 3: PA2	4: PE12 5: PG14	Embedded Trace Module ETM data 0.
ETM_TD1	0: PD3 1: PD13 2: PD3 3: PA3	4: PE13 5: PG13	Embedded Trace Module ETM data 1.
ETM_TD2	0: PD4 1: PB15 2: PD4 3: PA4	4: PE14 5: PG12	Embedded Trace Module ETM data 2.
ETM_TD3	0: PD5 1: PF3 2: PD5 3: PA5	4: PE15 5: PG11	Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PF6		LCD segment line 24.
LCD_SEG25	0: PF7		LCD segment line 25.
LCD_SEG26	0: PF8		LCD segment line 26.
LCD_SEG27	0: PF9		LCD segment line 27.
LCD_SEG28	0: PD9		LCD segment line 28.
LCD_SEG29	0: PD10		LCD segment line 29.
LCD_SEG30	0: PD11		LCD segment line 30.
LCD_SEG31	0: PD12		LCD segment line 31.
LCD_SEG32	0: PB0		LCD segment line 32.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
QSPI0_DQ7	0: PE11 1: PB6 2: PG8		Quad SPI 0 Data 7.
QSPI0_DQS	0: PF9 1: PE15 2: PG11		Quad SPI 0 Data S.
QSPI0_SCLK	0: PF6 1: PE14 2: PG0		Quad SPI 0 Serial Clock.
SDIO_CD	0: PF8 1: PC4 2: PA6 3: PB10		SDIO Card Detect.
SDIO_CLK	0: PE13 1: PE14		SDIO Serial Clock.
SDIO_CMD	0: PE12 1: PE15		SDIO Command.
SDIO_DAT0	0: PE11 1: PA0		SDIO Data 0.
SDIO_DAT1	0: PE10 1: PA1		SDIO Data 1.
SDIO_DAT2	0: PE9 1: PA2		SDIO Data 2.
SDIO_DAT3	0: PE8 1: PA3		SDIO Data 3.
SDIO_DAT4	0: PD12 1: PA4		SDIO Data 4.
SDIO_DAT5	0: PD11 1: PA5		SDIO Data 5.
SDIO_DAT6	0: PD10 1: PB3		SDIO Data 6.

Table 5.31. VDAC0 / OPA Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA0_N																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
OPA0_P																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	

Table 10.2. TQFP100 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
C1		15.4	
C2		15.4	
E		0.50 BSC	
X		0.30	
Y		1.50	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10.3 TQFP100 Package Marking

Figure 10.3. TQFP100 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

11.2 TQFP64 PCB Land Pattern

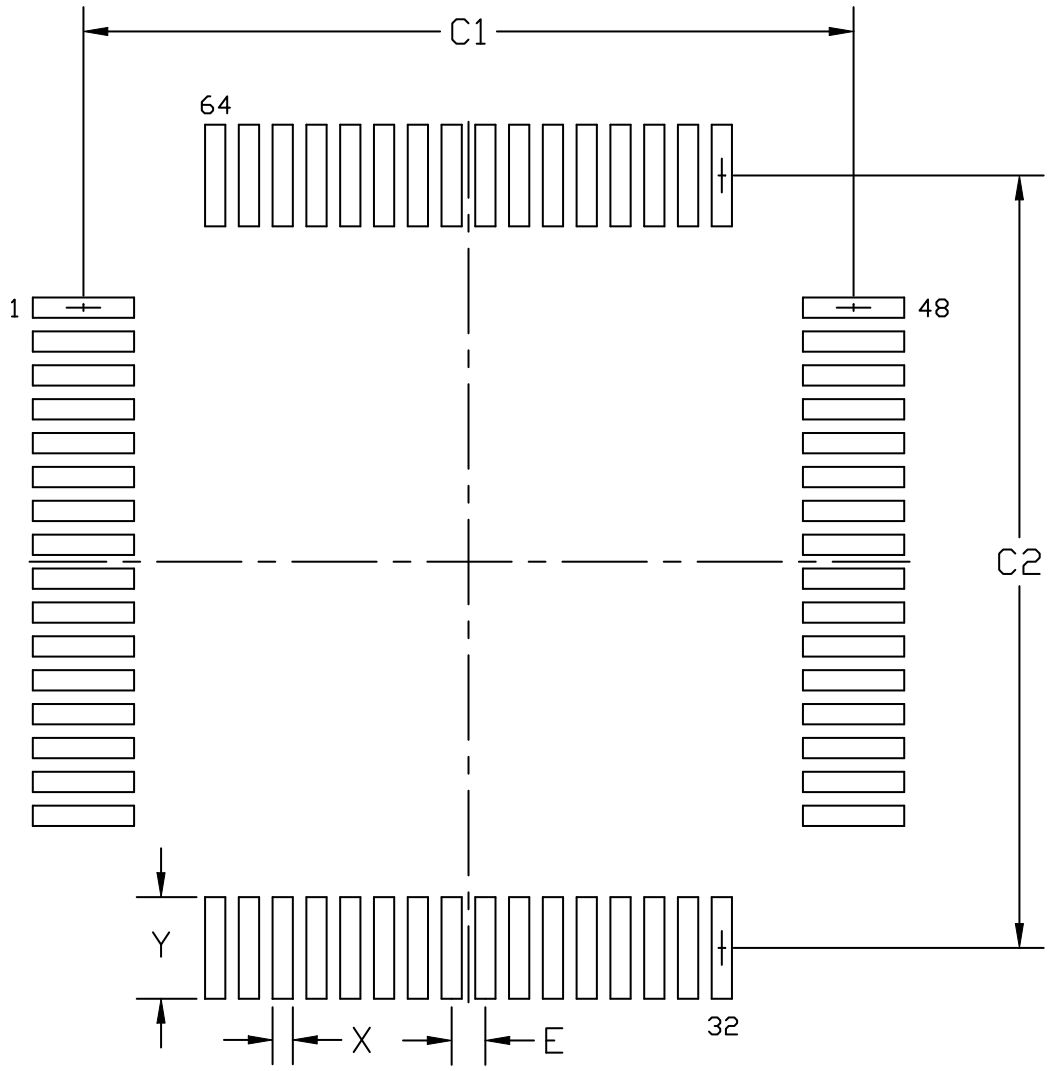

Figure 11.2. TQFP64 PCB Land Pattern Drawing

12.2 QFN64 PCB Land Pattern

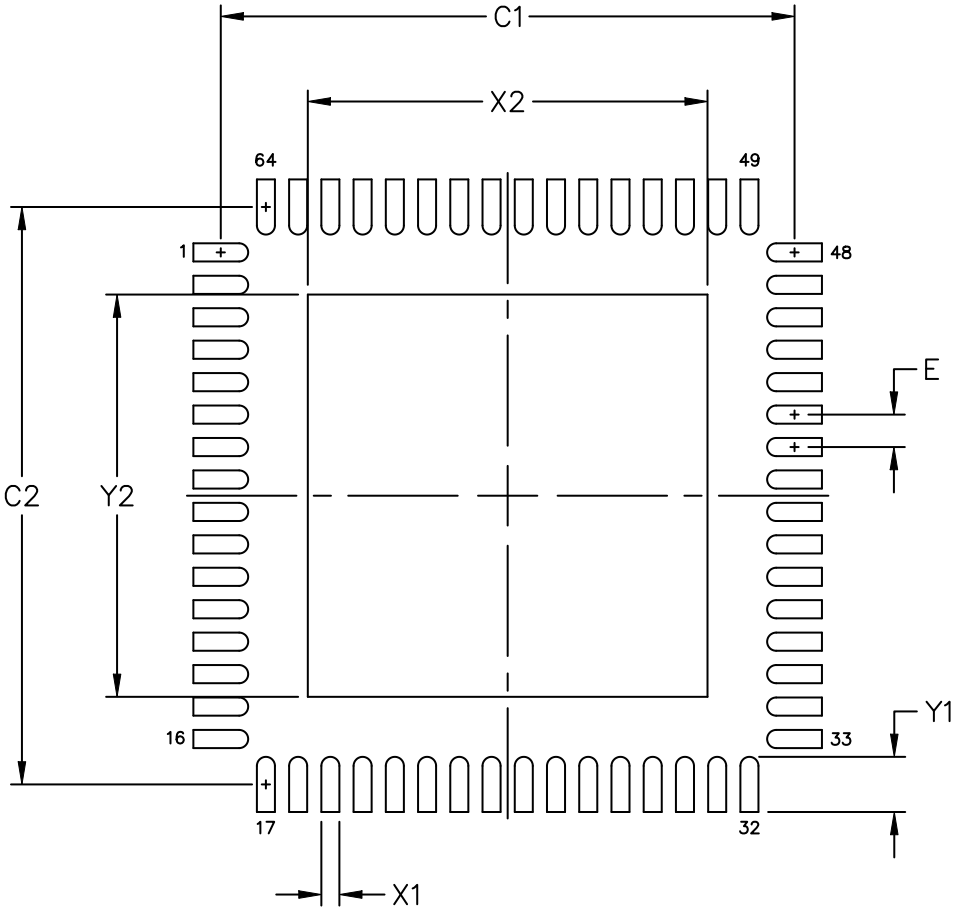

Figure 12.2. QFN64 PCB Land Pattern Drawing

12.3 QFN64 Package Marking

Figure 12.3. QFN64 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.