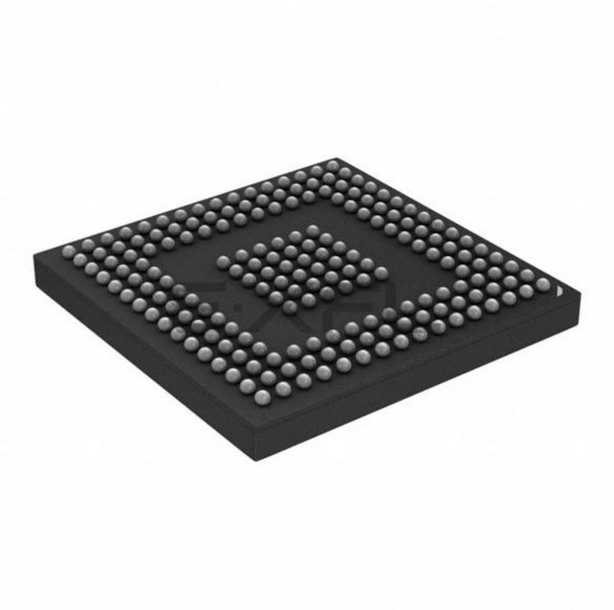

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 144 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.8V |
| Data Converters | A/D 16x12b SAR; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 192-VFBGA |
| Supplier Device Package | 192-BGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b820f2048gl192-ar |

### 3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

#### 3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

#### 3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

#### 3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

#### 4.1.10.3 Low-Frequency RC Oscillator (LFRCO)

**Table 4.14. Low-Frequency RC Oscillator (LFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{LFRCO}$ | ENVREF[2] = 1 | TBD | 32.768 | TBD | kHz |
| | | ENVREF[2] = 1, T > 85 °C | TBD | 32.768 | TBD | kHz |
| | | ENVREF[2] = 0 | TBD | 32.768 | TBD | kHz |
| Startup time | $t_{LFRCO}$ | | — | 500 | — | µs |
| Current consumption [1] | $I_{LFRCO}$ | ENVREF = 1 in CMU_LFRCOCTRL | — | 370 | — | nA |
| | | ENVREF = 0 in CMU_LFRCOCTRL | — | 520 | — | nA |

**Note:**
1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. In CMU_LFRCOCTRL register.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

#### 4.1.18 Capacitive Sense (CSEN)

**Table 4.26. Capacitive Sense (CSEN)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Single conversion time (1x accumulation) | $t_{CNV}$ | 12-bit SAR Conversions | — | 20.2 | — | µs |
| | | 16-bit SAR Conversions | — | 26.4 | — | µs |
| | | Delta Modulation Conversion (single comparison) | — | 1.55 | — | µs |
| Maximum external capacitive load | $C_{EXTMAX}$ | CS0CG=7 (Gain = 1x), including routing parasitics | — | 68 | — | pF |
| | | CS0CG=0 (Gain = 10x), including routing parasitics | — | 680 | — | pF |
| Maximum external series impedance | $R_{EXTMAX}$ | | — | 1 | — | kΩ |
| Supply current, EM2 bonded conversions, WARMUPMODE=NORMAL, WARMUPCNT=0 | $I_{CSEN\_BOND}$ | 12-bit SAR conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1] | — | 326 | — | nA |
| | | Delta Modulation conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1] | — | 226 | — | nA |
| | | 12-bit SAR conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1] | — | 33 | — | nA |
| | | Delta Modulation conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1] | — | 25 | — | nA |
| Supply current, EM2 scan conversions, WARMUPMODE=NORMAL, WARMUPCNT=0 | $I_{CSEN\_EM2}$ | 12-bit SAR conversions, 20 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan[1] | — | 690 | — | nA |
| | | Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan[1] | — | 515 | — | nA |
| | | 12-bit SAR conversions, 200 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan[1] | — | 79 | — | nA |
| | | Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan[1] | — | 57 | — | nA |

#### 4.1.24 USART SPI

**SPI Master Timing**

**Table 4.34. SPI Master Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCLK period [1 3 2] | $t_{SCLK}$ | All USARTs except USART2 | 2 * $t_{HFPERCLK}$ | — | — | ns |
| | | USART2 | 2 * $t_{HFPERBCLK}$ | — | — | ns |
| CS to MOSI [1 3] | $t_{CS\_MO}$ | USART2, location 4, IOVDD = 1.8 V | -3.2 | — | 6.8 | ns |
| | | USART2, location 4, IOVDD = 3.0 V | -2.3 | — | 6.0 | ns |
| | | USART2, location 5, IOVDD = 1.8 V | -8.1 | — | 6.3 | ns |
| | | USART2, location 5, IOVDD = 3.0 V | -7.3 | — | 4.4 | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | -15 | — | 13 | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | -13 | — | 11 | ns |
| SCLK to MOSI [1 3] | $t_{SCLK\_MO}$ | USART2, location 4, IOVDD = 1.8 V | -0.3 | — | 9.2 | ns |
| | | USART2, location 4, IOVDD = 3.0 V | -0.3 | — | 8.6 | ns |
| | | USART2, location 5, IOVDD = 1.8 V | -3.6 | — | 5.0 | ns |
| | | USART2, location 5, IOVDD = 3.0 V | -3.4 | — | 3.2 | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | -10 | — | 11 | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | -9 | — | 11 | ns |
| MISO setup time [1 3] | $t_{SU\_MI}$ | USART2, location 4, IOVDD = 1.8 V | 39.7 | — | — | ns |
| | | USART2, location 4, IOVDD = 3.0 V | 22.4 | — | — | ns |
| | | USART2, location 5, IOVDD = 1.8 V | 49.2 | — | — | ns |
| | | USART2, location 5, IOVDD = 3.0 V | 30.0 | — | — | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | 55 | — | — | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | 36 | — | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MISO hold time [1] [3] | $t_{H\_MI}$ | USART2, location 4, IOVDD = 1.8 V | -11.6 | — | — | ns |
| | | USART2, location 4, IOVDD = 3.0 V | -11.6 | — | — | ns |
| | | USART2, location 5, IOVDD = 1.8 V | -9.1 | — | — | ns |
| | | USART2, location 5, IOVDD = 3.0 V | -9.1 | — | — | ns |
| | | All other USARTs and locations, IOVDD = 1.8 V | -8 | — | — | ns |
| | | All other USARTs and locations, IOVDD = 3.0 V | -8 | — | — | ns |

**Note:**
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$).

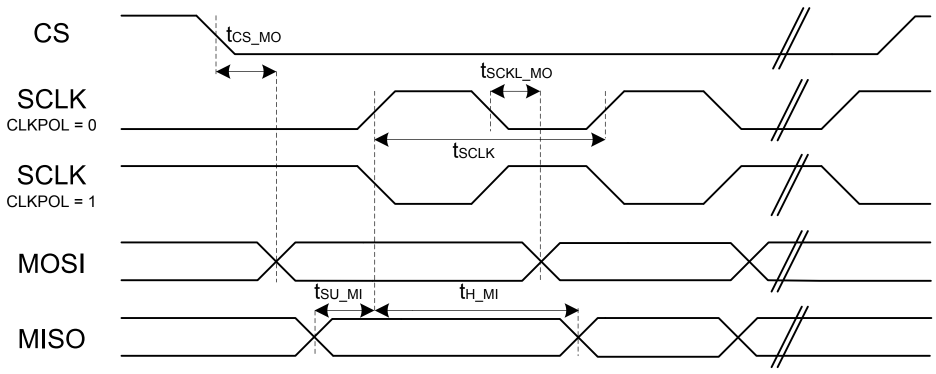


**Figure 4.1. SPI Master Timing Diagram**

### 4.1.25 External Bus Interface (EBI)

**EBI Write Enable Output Timing**

Timing applies to both EBI_WEn and EBI_NANDWEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.36. EBI Write Enable Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output hold time, from trailing EBI_WEn / EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid | $t_{OH\_WEn}$ | IOVDD ≥ 1.62 V | -22 + (WRHOLD * t{}HFCORECLK{}) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -13 + (WRHOLD * $t_{HFCORECLK}$) | — | — | ns |
| Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_WEn / EBI_NANDWEn edge[1] | $t_{OSU\_WEn}$ | IOVDD ≥ 1.62 V | -12 + (WRSETUP * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -10 + (WRSETUP * $t_{HFCORECLK}$) | — | — | ns |
| EBI_WEn / EBI_NANDWEn pulse width[1] | $t_{WIDTH\_WEn}$ | IOVDD ≥ 1.62 V | -6 + (MAX(1, WRSTRB) * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -5 + (MAX(1, WRSTRB) * $t_{HFCORECLK}$) | — | — | ns |

**Note:**

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of $t_{WIDTH\_WEn}$ and increases the length of $t_{OSU\_WEn}$ by 1/2 * $t_{HFCLKNODIV}$.

### EBI Address Latch Enable Output Timing

Timing applies to multiplexed addressing modes D8A24ALE and D16A16ALE for both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.37. EBI Address Latch Enable Output Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output hold time, from trailing EBI_ALE edge to EBI_AD invalid[1 2] | $t_{OH\_ALEn}$ | IOVDD ≥ 1.62 V | -22 + (ADDRHOLD * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -11 + (ADDRHOLD * $t_{HFCORECLK}$) | — | — | ns |
| Output setup time, from EBI_AD valid to leading EBI_ALE edge | $t_{OSU\_ALEn}$ | IOVDD ≥ 1.62 V | -12 | — | — | ns |
| | | IOVDD ≥ 3.0 V | -9 | — | — | ns |
| EBI_ALEn pulse width[1] | $t_{WIDTH\_ALEn}$ | IOVDD ≥ 1.62 V | -4 + ((ADDRSETUP + 1) * t{}HFCORECLK{}) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -3 + ((ADDRSETUP + 1) * t{}HFCORECLK{}) | — | — | ns |

**Note:**

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALEn can be moved to the left by setting HALFALE=1. This decreases the length of $t_{WIDTH\_ALEn}$ and increases the length of $t_{OSU\_ALEn}$ by $t_{HFCORECLK}$ - 1/2 * $t_{HFCLKNODIV}$.
2. The figure shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

**EBI Read Enable Output Timing**

Timing applies to both EBI_REn and EBI_NANDREn for all addressing modes and both polarities. Output timing for EBI_AD applies only to multiplexed addressing modes D8A24ALE and D16A16ALE. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.38. EBI Read Enable Output Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output hold time, from trailing EBI_REn / EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid | $t_{OH\_REn}$ | IOVDD ≥ 1.62 V | -23 + (RDHOLD * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -13 + (RDHOLD * $t_{HFCORECLK}$) | — | — | ns |
| Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_REn / EBI_NANDREn edge [1] | $t_{OSU\_REn}$ | IOVDD ≥ 1.62 V | -12 + (RDSETUP * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -11 + (RDSETUP * $t_{HFCORECLK}$) | — | — | ns |
| EBI_REn pulse width[1] [2] | $t_{WIDTH\_REn}$ | IOVDD ≥ 1.62 V | -6 + (MAX(1, RDSTRB) * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -4 + (MAX(1, RDSTRB) * $t_{HFCORECLK}$) | — | — | ns |

**Note:**

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of $t_{WIDTH\_REn}$ and increases the length of $t_{OSU\_REn}$ by 1/2 * $t_{HFCLKNODIV}$.
2. When page mode is used, RDSTRB is replaced by RDPA for page hits.

**SDIO MMC DDR Mode Timing at 1.8 V**

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

**Table 4.52. SDIO MMC DDR Mode Timing (Location 0, 1.8V I/O)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency during data transfer | $F_{SD\_CLK}$ | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 18 | MHz |
| | | Using HFXO | — | — | TBD | MHz |
| Clock low time | $t_{WL}$ | Using HFRCO, AUXHFRCO, or USHFRCO | 25.1 | — | — | ns |
| | | Using HFXO | TBD | — | — | ns |
| Clock high time | $t_{WH}$ | Using HFRCO, AUXHFRCO, or USHFRCO | 25.1 | — | — | ns |
| | | Using HFXO | TBD | — | — | ns |
| Clock rise time | $t_R$ | | 1.13 | 5.21 | — | ns |
| Clock fall time | $t_F$ | | 1.01 | 4.10 | — | ns |
| Input setup time, CMD valid to SD_CLK | $t_{ISU}$ | | 5.3 | — | — | ns |
| Input hold time, SD_CLK to CMD change | $t_{IH}$ | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD valid | $t_{ODLY}$ | | 0 | — | 16 | ns |
| Output hold time, SD_CLK to CMD change | $t_{OH}$ | | 3 | — | — | ns |
| Input setup time, DAT[0:7] valid to SD_CLK | $t_{ISU2X}$ | | 5.3 | — | — | ns |
| Input hold time, SD_CLK to DAT[0:7] change | $t_{IH2X}$ | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to DAT[0:7] valid | $t_{ODLY2X}$ | | 0 | — | 16 | ns |
| Output hold time, SD_CLK to DAT[0:7] change | $t_{OH2X}$ | | 3 | — | — | ns |

**QSPI DDR Mode Timing (Locations 1, 2)**

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 53, RX DLL = 88, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

**Table 4.57. QSPI DDR Mode Timing (Locations 1, 2)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Half SCLK period | T/2 | HFXO | $(1/F_{SCLK})$ * 0.4 - 0.4 | — | — | ns |
| | | HFRCO, AUXHFRCO, USHFRCO | $(1/F_{SCLK})$ * 0.44 | — | — | ns |
| Output valid | $t_{OV}$ | | — | — | T/2 - 6.6 | ns |
| Output hold | $t_{OH}$ | | T/2 - 52.2 | — | — | ns |
| Input setup | $t_{SU}$ | | 44.8 | — | — | ns |
| Input hold | $t_H$ | | -2.4 | — | — | ns |

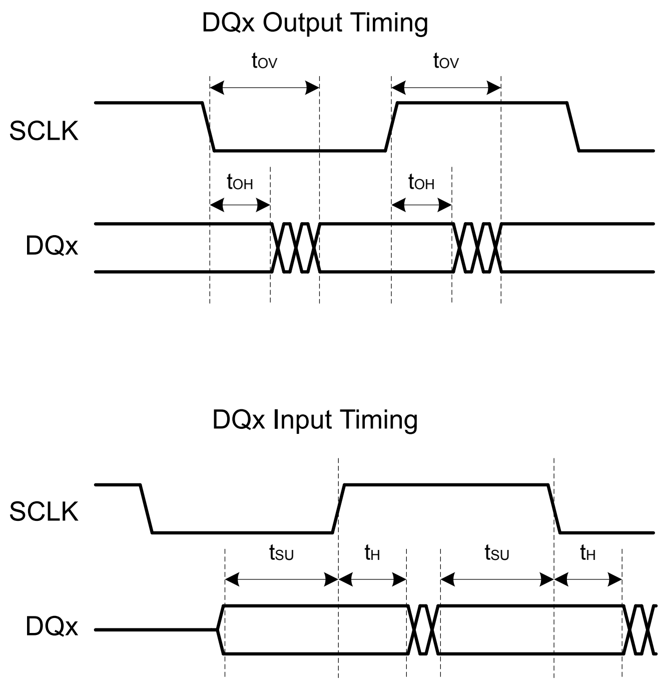


**Figure 4.22. QSPI DDR Timing Diagrams**

**QSPI DDR Flash Timing Example**

This example uses timing values for location 0 (DDR mode) to demonstrate the calculation of allowable flash timing using the QSPI in DDR mode.

- Using a configured SCLK frequency ($F_{SCLK}$) of 8 MHz from the HFXO clock source:
- The resulting minimum half-period, T/2(min) = $(1/F_{SCLK})$ * 0.4 - 0.4 = 49.6 ns.
- Flash will see a minimum setup time of T/2 – $t_{OV}$ = T/2 – (T/2 – 5.0) = 5.0 ns.
- Flash will see a minimum hold time of $t_{OH}$ = T/2 – 39.4 = 49.6 – 39.4 = 10.2 ns.
- Flash can have a maximum output valid time of T/2 – $t_{SU}$ = T/2 – 33.1 = 49.6 – 33.1 = 16.5 ns.
- Flash can have a minimum output hold time of $t_H$ = - 0.9 ns.

# 5. Pin Definitions

## 5.1 EFM32GG11B8xx in BGA192 Device Pinout

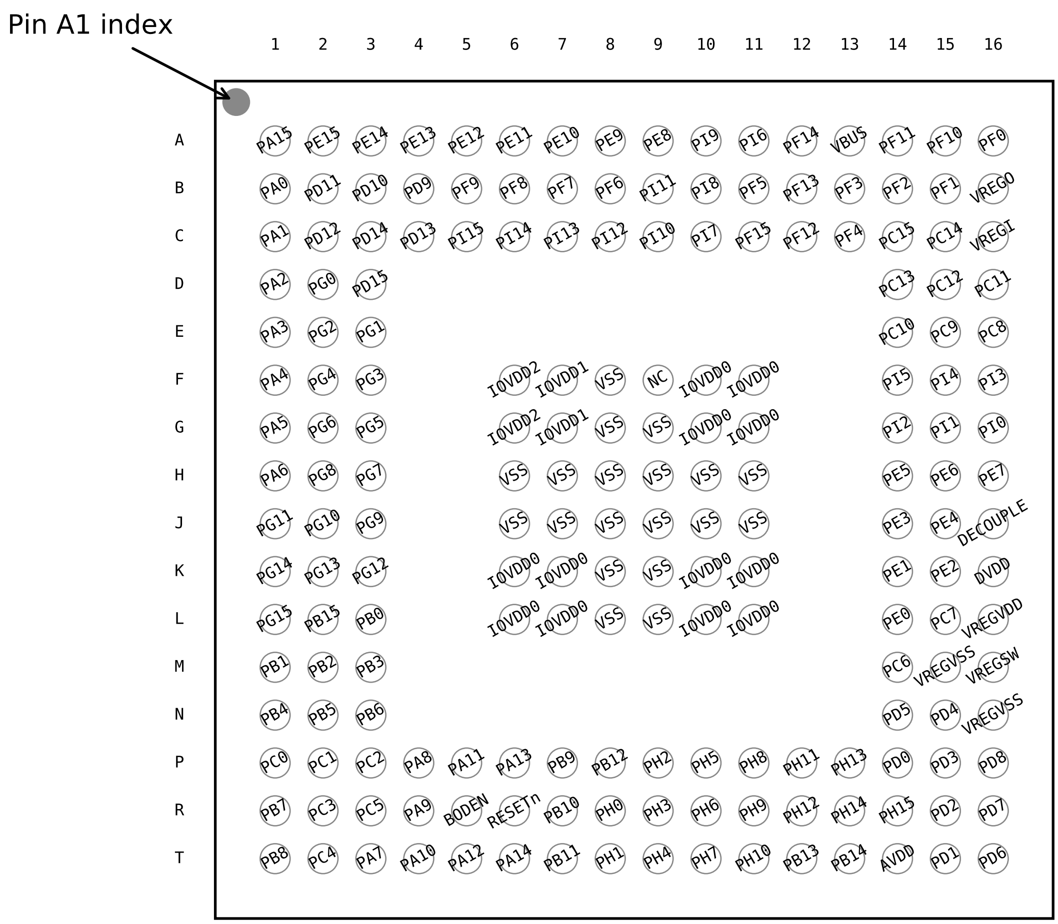

**Figure 5.1. EFM32GG11B8xx in BGA192 Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

**Table 5.1. EFM32GG11B8xx in BGA192 Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PA15 | A1 | GPIO | PE15 | A2 | GPIO |
| PE14 | A3 | GPIO | PE13 | A4 | GPIO |
| PE12 | A5 | GPIO | PE11 | A6 | GPIO |
| PE10 | A7 | GPIO | PE9 | A8 | GPIO |
| PE8 | A9 | GPIO | PI9 | A10 | GPIO (5V) |
| PI6 | A11 | GPIO (5V) | PF14 | A12 | GPIO (5V) |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PB2 | M2 | GPIO | PB3 | M3 | GPIO |
| PC6 | M14 | GPIO | VREGVSS | M15<br>N16 | Voltage regulator VSS |
| VREGSW | M16 | DCDC regulator switching node | PB4 | N1 | GPIO |
| PB5 | N2 | GPIO | PB6 | N3 | GPIO |
| PD5 | N14 | GPIO | PD4 | N15 | GPIO |
| PC0 | P1 | GPIO (5V) | PC1 | P2 | GPIO (5V) |
| PC2 | P3 | GPIO (5V) | PA8 | P4 | GPIO |
| PA11 | P5 | GPIO | PA13 | P6 | GPIO (5V) |
| PB9 | P7 | GPIO (5V) | PB12 | P8 | GPIO |
| PH2 | P9 | GPIO (5V) | PH5 | P10 | GPIO |
| PH8 | P11 | GPIO (5V) | PH11 | P12 | GPIO (5V) |
| PH13 | P13 | GPIO (5V) | PD0 | P14 | GPIO (5V) |
| PD3 | P15 | GPIO | PD8 | P16 | GPIO |
| PB7 | R1 | GPIO | PC3 | R2 | GPIO (5V) |
| PC5 | R3 | GPIO | PA9 | R4 | GPIO |
| BODEN | R5 | Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. | RESETn | R6 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| PB10 | R7 | GPIO (5V) | PH0 | R8 | GPIO (5V) |
| PH3 | R9 | GPIO (5V) | PH6 | R10 | GPIO |
| PH9 | R11 | GPIO (5V) | PH12 | R12 | GPIO (5V) |
| PH14 | R13 | GPIO (5V) | PH15 | R14 | GPIO (5V) |
| PD2 | R15 | GPIO (5V) | PD7 | R16 | GPIO |
| PB8 | T1 | GPIO | PC4 | T2 | GPIO |
| PA7 | T3 | GPIO | PA10 | T4 | GPIO |
| PA12 | T5 | GPIO (5V) | PA14 | T6 | GPIO |
| PB11 | T7 | GPIO | PH1 | T8 | GPIO (5V) |
| PH4 | T9 | GPIO | PH7 | T10 | GPIO (5V) |
| PH10 | T11 | GPIO (5V) | PB13 | T12 | GPIO |
| PB14 | T13 | GPIO | AVDD | T14 | Analog power supply. |
| PD1 | T15 | GPIO | PD6 | T16 | GPIO |

**Note:**
1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PB2 | 11 | GPIO | PB3 | 12 | GPIO |
| PB4 | 13 | GPIO | PB5 | 14 | GPIO |
| PB6 | 15 | GPIO | VSS | 16<br>32<br>58<br>83 | Ground |
| PC0 | 18 | GPIO (5V) | PC1 | 19 | GPIO (5V) |
| PC2 | 20 | GPIO (5V) | PC3 | 21 | GPIO (5V) |
| PC4 | 22 | GPIO | PC5 | 23 | GPIO |
| PB7 | 24 | GPIO | PB8 | 25 | GPIO |
| PA7 | 26 | GPIO | PA8 | 27 | GPIO |
| PA9 | 28 | GPIO | PA10 | 29 | GPIO |
| PA11 | 30 | GPIO | PA12 | 33 | GPIO (5V) |
| PA13 | 34 | GPIO (5V) | PA14 | 35 | GPIO |
| RESETn | 36 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB9 | 37 | GPIO (5V) |
| PB10 | 38 | GPIO (5V) | PB11 | 39 | GPIO |
| PB12 | 40 | GPIO | AVDD | 41<br>45 | Analog power supply. |
| PB13 | 42 | GPIO | PB14 | 43 | GPIO |
| PD0 | 46 | GPIO (5V) | PD1 | 47 | GPIO |
| PD2 | 48 | GPIO (5V) | PD3 | 49 | GPIO |
| PD4 | 50 | GPIO | PD5 | 51 | GPIO |
| PD6 | 52 | GPIO | PD7 | 53 | GPIO |
| PD8 | 54 | GPIO | PC6 | 55 | GPIO |
| PC7 | 56 | GPIO | DVDD | 57 | Digital power supply. |
| DECOUPLE | 59 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. | PE0 | 60 | GPIO (5V) |
| PE1 | 61 | GPIO (5V) | PE2 | 62 | GPIO |
| PE3 | 63 | GPIO | PE4 | 64 | GPIO |
| PE5 | 65 | GPIO | PE6 | 66 | GPIO |
| PE7 | 67 | GPIO | PC8 | 68 | GPIO (5V) |
| PC9 | 69 | GPIO (5V) | PC10 | 70 | GPIO (5V) |
| PC11 | 71 | GPIO (5V) | PC12 | 72 | GPIO (5V) |
| PC13 | 73 | GPIO (5V) | PC14 | 74 | GPIO (5V) |
| PC15 | 75 | GPIO (5V) | PF0 | 76 | GPIO (5V) |
| PF1 | 77 | GPIO (5V) | PF2 | 78 | GPIO |

### 5.12 EFM32GG11B8xx in QFP64 Device Pinout

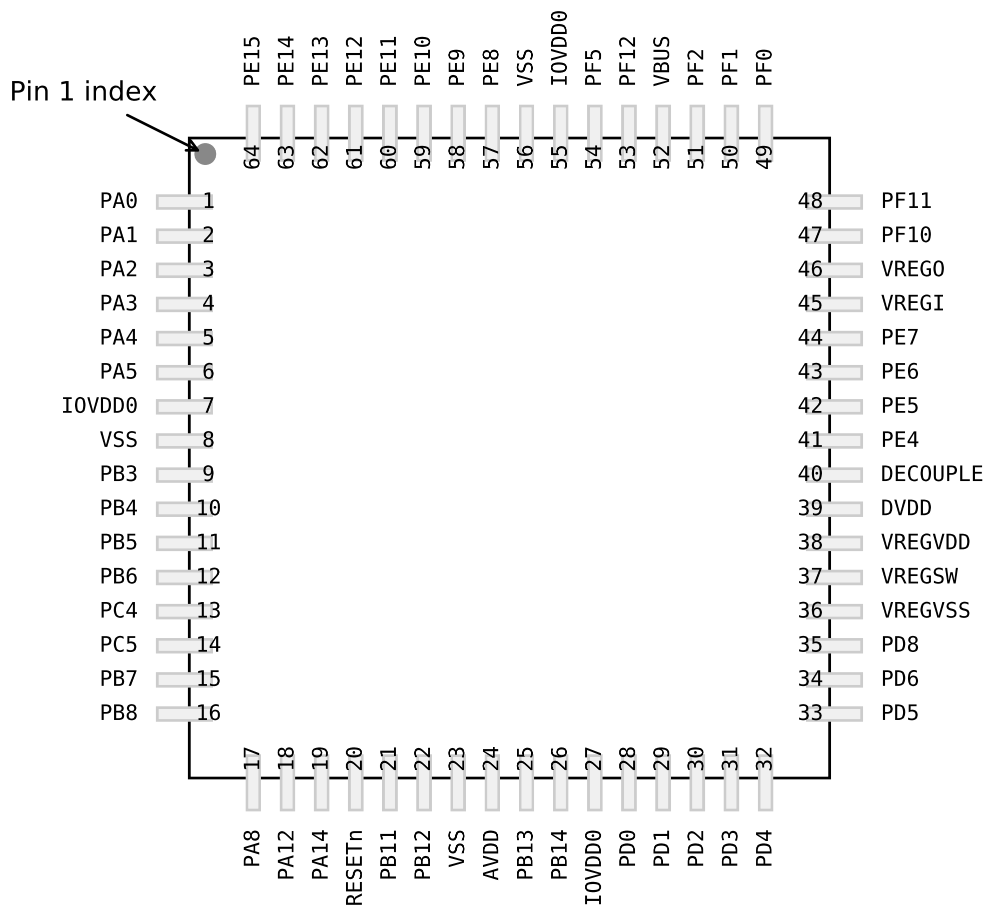


**Figure 5.12. EFM32GG11B8xx in QFP64 Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

**Table 5.12. EFM32GG11B8xx in QFP64 Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PA0 | 1 | GPIO | PA1 | 2 | GPIO |
| PA2 | 3 | GPIO | PA3 | 4 | GPIO |
| PA4 | 5 | GPIO | PA5 | 6 | GPIO |
| IOVDD0 | 7<br>27<br>55 | Digital IO power supply 0. | VSS | 8<br>23<br>56 | Ground |
| PB3 | 9 | GPIO | PB4 | 10 | GPIO |
| PB5 | 11 | GPIO | PB6 | 12 | GPIO |

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | EBI | Timers | Communication | Other |
| PF14 | BUSDY BUSCX | | TIM1_CC1 #6 TIM4_CC1 #1 TIM5_CC2 #7 WTIM3_CC1 #7 | I2C2_SCL #4 | |
| PF11 | BUSCY BUSDX | EBI_NANDWEn #5 | TIM5_CC2 #6 WTIM3_CC2 #3 PCNT2_S1IN #3 | US5_CTS #2 U1_RX #1 I2C2_SCL #2 USB_DP | |
| PF10 | BUSDY BUSCX | EBI_ARDY #5 | TIM5_CC1 #6 WTIM3_CC1 #3 PCNT2_S0IN #3 | US5_RTS #2 U1_TX #1 I2C2_SDA #2 USB_DM | |
| PF0 | BUSDY BUSCX | EBI_A24 #1 | TIM0_CC0 #4 WTIM0_CC1 #4 LE-TIM0_OUT0 #2 | US2_TX #5 CAN0_RX #1 US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | PRS_CH15 #2 ACMP3_O #0 DBG_SWCLKTCK BOOT_TX |
| PA0 | BUSBY BUSAX LCD_SEG13 | EBI_AD09 #0 EBI_CSTFT #3 | TIM0_CC0 #0 TIM0_CC1 #7 TIM3_CC0 #4 PCNT0_S0IN #4 | ETH_RMIITXEN #0 ETH_MIITXCLK #0 SDIO_DAT0 #1 US1_RX #5 US3_TX #0 QSPI0_CS0 #1 LEU0_RX #4 I2C0_SDA #0 | CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0 |
| PD11 | LCD_SEG30 | EBI_CS2 #0 EBI_HSNC #1 | TIM4_CC0 #6 WTIM3_CC2 #0 | ETH_RMIICRSDV #1 SDIO_DAT5 #0 QSPI0_DQ2 #0 ETH_MIIRXD3 #2 US4_CLK #1 | |
| PD10 | LCD_SEG29 | EBI_CS1 #0 EBI_VSNC #1 | TIM4_CC2 #5 WTIM3_CC1 #0 | ETH_RMIIREFCLK #1 SDIO_DAT6 #0 QSPI0_DQ1 #0 ETH_MIIRXD2 #2 US4_RX #1 | CMU_CLK2 #5 CMU_CLKI0 #5 |
| PD9 | LCD_SEG28 | EBI_CS0 #0 EBI_DTEN #1 | TIM4_CC1 #5 WTIM3_CC0 #0 | ETH_RMIIRXD0 #1 SDIO_DAT7 #0 QSPI0_DQ0 #0 ETH_MIIRXD1 #2 US4_TX #1 | |
| PF9 | BUSCY BUSDX LCD_SEG27 | EBI_REn #4 EBI_BL1 #1 | TIM4_CC0 #5 | ETH_RMIIRXD1 #1 US2_CS #4 QSPI0_DQS #0 ETH_MIIRXD0 #2 ETH_TSUTMRTOG #3 SDIO_WP #0 U0_RTS #0 U1_CTS #1 | ETM_TD0 #1 |
| PF8 | BUSDY BUSCX LCD_SEG26 | EBI_WEn #4 EBI_BL0 #1 | TIM0_CC2 #1 TIM4_CC2 #4 | ETH_RMIITXEN #1 US2_CLK #4 QSPI0_CS1 #0 ETH_MIIRXDV #2 ETH_TSUEXTCLK #3 SDIO_CD #0 U0_CTS #0 U1_RTS #1 | ETM_TCLK #1 GPIO_EM4WU8 |

| Alternate | LOCATION | | |
|---|---|---|---|
| **Functionality** | **0 - 3** | **4 - 7** | **Description** |
| LFXTAL_N | 0: PB8 | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | 0: PB7 | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| OPA0_N | 0: PC5 | | Operational Amplifier 0 external negative input. |
| OPA0_P | 0: PC4 | | Operational Amplifier 0 external positive input. |
| OPA1_N | 0: PD7 | | Operational Amplifier 1 external negative input. |
| OPA1_P | 0: PD6 | | Operational Amplifier 1 external positive input. |
| OPA2_N | 0: PD3 | | Operational Amplifier 2 external negative input. |
| OPA2_OUT | 0: PD5 | | Operational Amplifier 2 output. |
| OPA2_OUTALT | 0: PD0 | | Operational Amplifier 2 alternative output. |
| OPA2_P | 0: PD4 | | Operational Amplifier 2 external positive input. |
| OPA3_N | 0: PC7 | | Operational Amplifier 3 external negative input. |
| OPA3_OUT | 0: PD1 | | Operational Amplifier 3 output. |
| OPA3_P | 0: PC6 | | Operational Amplifier 3 external positive input. |

## 11.2 TQFP64 PCB Land Pattern

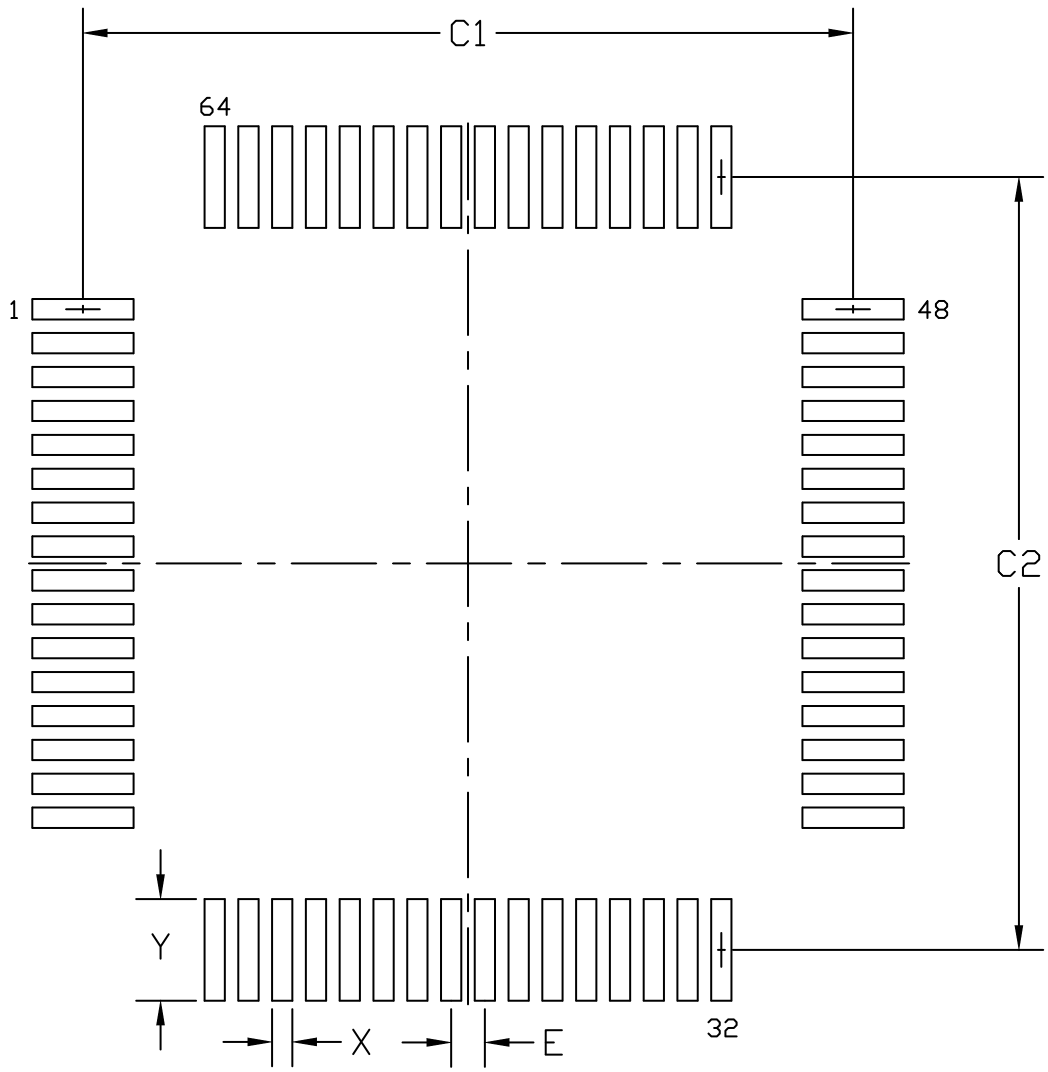


**Figure 11.2. TQFP64 PCB Land Pattern Drawing**

# 13. Revision History

**Revision 0.6**

March, 2018

- Removed "Confindential" watermark.
- Updated 4.1 Electrical Characteristics and 4.2 Typical Performance Curves with latest characterization data.

**Revision 0.2**

October, 2017

- Updated memory maps to latest formatting and to include all peripherals.
- Updated all electrical specifications tables with latest characterization results.
- **Absolute Maximum Ratings** Table:
  - Removed redundant $I_{VSSMAX}$ line.
  - Added footnote to clarify $V_{DIGPIN}$ specification for 5V tolerant GPIO.
- **General Operating Conditions** Table:
  - Removed $dV_{DD}$ specification and redundant footnote about shorting VREGVDD and AVDD together.
  - Added footnote about IOVDD voltage restriction when CSEN peripheral is used with chopping enabled.
- **Flash Memory Characteristics** Table: Added timing measurement clarification for Device Erase and Mass Erase.
- **Analog to Digital Converter (ADC)** Table:
  - Added header text for general specification conditions.
  - Added footnote for clarification of input voltage limits.
- Minor typographical corrections, including capitalization, mis-spellings and punctuation marks, throughout document.
- Minor formatting and styling updates, including table formats, TOC location, and boilerplate information throughout document.

**Revision 0.1**

April 27th, 2017

Initial release.