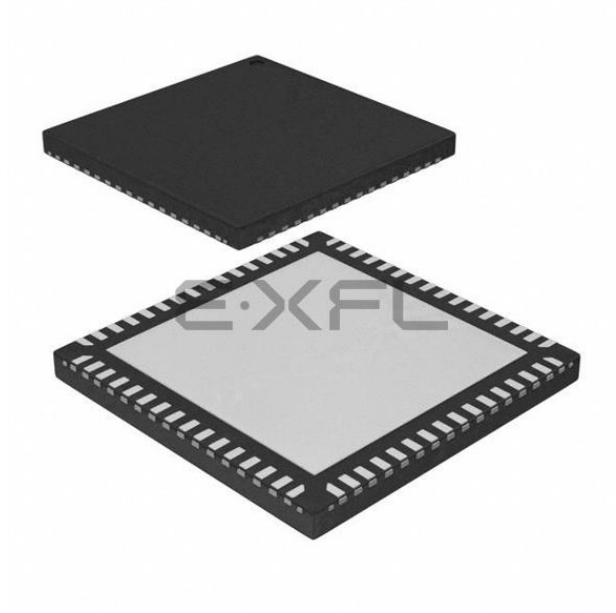
Silicon Labs - EFM32GG11B820F2048GM64-A Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b820f2048gm64-a

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to 4.1.2.1 General Operating Conditions for more details about operational supply and temperature limits.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.9	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	4.3	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.8	TBD	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFRCO	—	3.6	TBD	µA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.08	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.69	—	µA
		128 byte RAM retention, no RTCC	—	0.69	TBD	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.16	TBD	µA
Current consumption of peripheral power domain 1, with voltage scaling enabled	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[1]	—	0.68	—	µA
Current consumption of peripheral power domain 2, with voltage scaling enabled	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[1]	—	0.28	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency limits	f_{HFRCO_BAND}	FREQRANGE = 0, FINETUNINGEN = 0	1	—	10	MHz
		FREQRANGE = 3, FINETUNINGEN = 0	2	—	17	MHz
		FREQRANGE = 6, FINETUNINGEN = 0	4	—	30	MHz
		FREQRANGE = 7, FINETUNINGEN = 0	5	—	34	MHz
		FREQRANGE = 8, FINETUNINGEN = 0	7	—	42	MHz
		FREQRANGE = 10, FINETUNINGEN = 0	12	—	58	MHz
		FREQRANGE = 11, FINETUNINGEN = 0	15	—	68	MHz
		FREQRANGE = 12, FINETUNINGEN = 0	18	—	83	MHz
		FREQRANGE = 13, FINETUNINGEN = 0	24	—	100	MHz
		FREQRANGE = 14, FINETUNINGEN = 0	28	—	119	MHz
		FREQRANGE = 15, FINETUNINGEN = 0	33	—	138	MHz
		FREQRANGE = 16, FINETUNINGEN = 0	43	—	163	MHz

Note:

1. Maximum DPLL lock time ~= 6 x (M+1) x t_{REF}, where t_{REF} is the reference clock period.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
3. ± 100 mV differential drive.
4. In ACMPn_CTRL register.
5. In ACMPn_HYSTERESIS registers.
6. In ACMPn_INPUTSEL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew rate[5]	SR	DRIVESTRENGTH = 3, INCBW=1[3]	—	4.7	—	V/µs
		DRIVESTRENGTH = 3, INCBW=0	—	1.5	—	V/µs
		DRIVESTRENGTH = 2, INCBW=1[3]	—	1.27	—	V/µs
		DRIVESTRENGTH = 2, INCBW=0	—	0.42	—	V/µs
		DRIVESTRENGTH = 1, INCBW=1[3]	—	0.17	—	V/µs
		DRIVESTRENGTH = 1, INCBW=0	—	0.058	—	V/µs
		DRIVESTRENGTH = 0, INCBW=1[3]	—	0.044	—	V/µs
		DRIVESTRENGTH = 0, INCBW=0	—	0.015	—	V/µs
Startup time[6]	T_{START}	DRIVESTRENGTH = 2	—	—	12	µs
Input offset voltage	V_{OSI}	DRIVESTRENGTH = 2 or 3, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	TBD	—	TBD	mV
DC power supply rejection ratio[9]	$PSRR_{DC}$	Input referred	—	70	—	dB
DC common-mode rejection ratio[9]	$CMRR_{DC}$	Input referred	—	70	—	dB
Total harmonic distortion	THD_{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 4.7 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

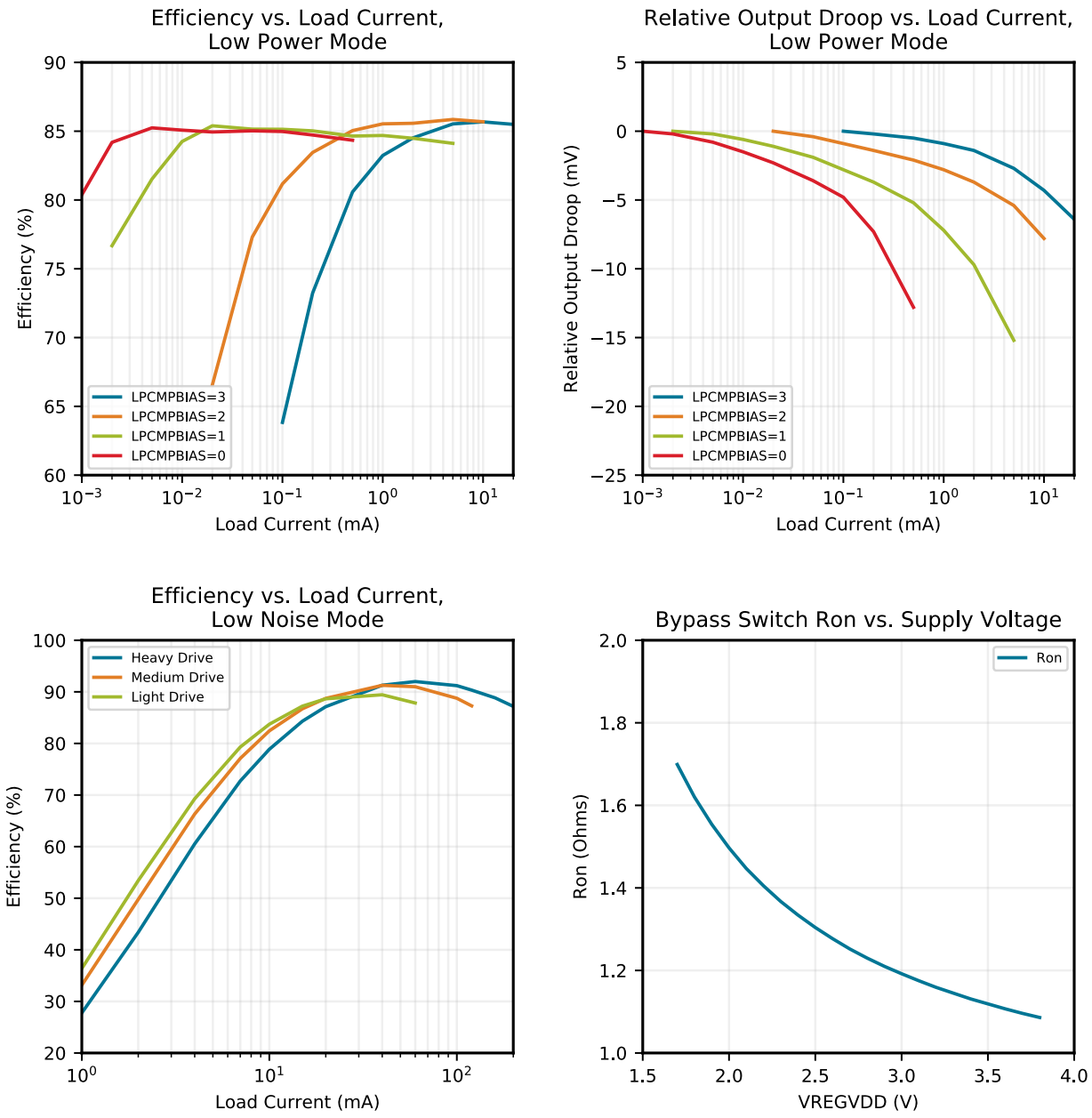


Figure 4.29. DC-DC Converter Typical Performance Characteristics

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVDD	J13	Voltage regulator VDD input	PC0	K1	GPIO (5V)
PC1	K2	GPIO (5V)	PE0	K12	GPIO (5V)
VREGSW	K13	DCDC regulator switching node	PC2	L1	GPIO (5V)
PC3	L2	GPIO (5V)	PA7	L3	GPIO
PB9	L13	GPIO (5V)	PB10	L14	GPIO (5V)
PD1	L17	GPIO	PC6	L18	GPIO
PC7	L19	GPIO	VREGVSS	L20	Voltage regulator VSS
PB7	M1	GPIO	PC4	M2	GPIO
PA8	M3	GPIO	PA10	M4	GPIO
PA13	M5	GPIO (5V)	PA14	M6	GPIO
RESETn	M7	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB12	M8	GPIO
PD0	M9	GPIO (5V)	PD2	M10	GPIO (5V)
PD3	M11	GPIO	PD4	M12	GPIO
PD8	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	BODEN	N7	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.
PB13	N8	GPIO	PB14	N9	GPIO
AVDD	N10	Analog power supply.	PD5	N11	GPIO
PD6	N12	GPIO	PD7	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.5 EFM32GG11B4xx in BGA120 Device Pinout

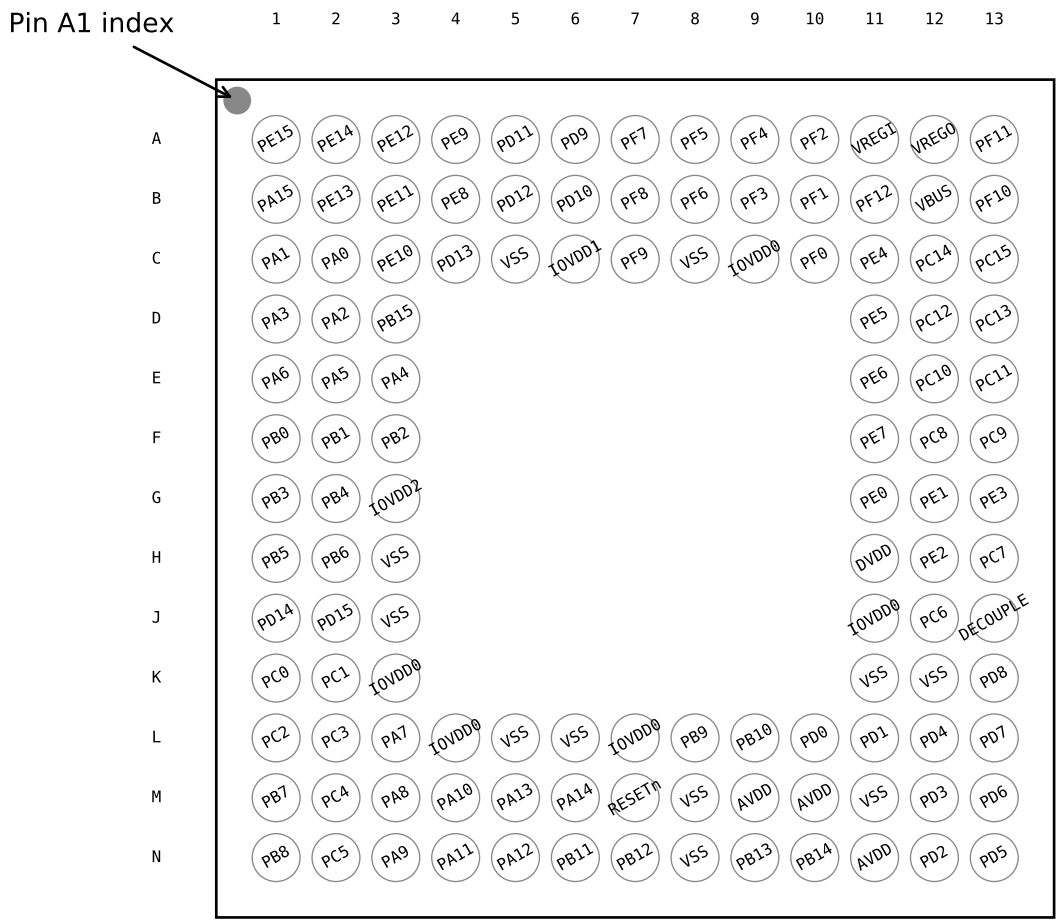


Figure 5.5. EFM32GG11B4xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.5. EFM32GG11B4xx in BGA120 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF4	A9	GPIO	PF2	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF3	B9	GPIO
PF1	B10	GPIO (5V)	PF12	B11	GPIO
VBUS	B12	USB VBUS signal and auxiliary input to 5 V regulator.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 K12 L12 L13 M8 M11 N8	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L14	Digital IO power supply 0.
PF0	C10	GPIO (5V)	PE4	C11	GPIO
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PE5	D11	GPIO
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PE6	E11	GPIO
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE7	F11	GPIO
PC8	F12	GPIO (5V)	PC9	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE0	G11	GPIO (5V)
PE1	G12	GPIO (5V)	PE3	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
PC7	H13	GPIO	PD14	J1	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE8	B4	GPIO	PD11	B5	GPIO
PF8	B6	GPIO	PF6	B7	GPIO
PF3	B8	GPIO	PE5	B9	GPIO
PC12	B10	GPIO (5V)	PC13	B11	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
PD12	C5	GPIO	PF9	C6	GPIO
VSS	C7 D4 F9 G3 G9 H6 K4 K7 K10 L7	Ground	PF2	C8	GPIO
PE6	C9	GPIO	PC10	C10	GPIO (5V)
PC11	C11	GPIO (5V)	PA3	D1	GPIO
PA2	D2	GPIO	PB15	D3	GPIO (5V)
IOVDD1	D5	Digital IO power supply 1.	PD9	D6	GPIO
IOVDD0	D7 G8 H7 L4	Digital IO power supply 0.	PF1	D8	GPIO (5V)
PE7	D9	GPIO	PC8	D10	GPIO (5V)
PC9	D11	GPIO (5V)	PA6	E1	GPIO
PA5	E2	GPIO	PA4	E3	GPIO
PB0	E4	GPIO	PF0	E8	GPIO (5V)
PE0	E9	GPIO (5V)	PE1	E10	GPIO (5V)
PE3	E11	GPIO	PB1	F1	GPIO
PB2	F2	GPIO	PB3	F3	GPIO
PB4	F4	GPIO	DVDD	F8	Digital power supply.
PE2	F10	GPIO	DECOUPLE	F11	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PB5	G1	GPIO	PB6	G2	GPIO
IOVDD2	G4	Digital IO power supply 2.	PC6	G10	GPIO
PC7	G11	GPIO	PC0	H1	GPIO (5V)
PC2	H2	GPIO (5V)	PD14	H3	GPIO (5V)
PA7	H4	GPIO	PA8	H5	GPIO
PD8	H8	GPIO	PD5	H9	GPIO
PD6	H10	GPIO	PD7	H11	GPIO

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_BEXT	0: PA14		LCD external supply bypass in step down or charge pump mode. If using the LCD in step-down or charge pump mode, a 1 uF (minimum) capacitor between this pin and VSS is required. To reduce supply ripple, a larger capcitor of approximately 1000 times the total LCD segment capacitance may be used. If using the LCD with the internal supply source, this pin may be left unconnected or used as a GPIO.
LCD_COM0	0: PE4		LCD driver common line number 0.
LCD_COM1	0: PE5		LCD driver common line number 1.
LCD_COM2	0: PE6		LCD driver common line number 2.
LCD_COM3	0: PE7		LCD driver common line number 3.
LCD_SEG0	0: PF2		LCD segment line 0.
LCD_SEG1	0: PF3		LCD segment line 1.
LCD_SEG2	0: PF4		LCD segment line 2.
LCD_SEG3	0: PF5		LCD segment line 3.
LCD_SEG4	0: PE8		LCD segment line 4.
LCD_SEG5	0: PE9		LCD segment line 5.
LCD_SEG6	0: PE10		LCD segment line 6.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.
OPA2_OUT	0: PD5		Operational Amplifier 2 output.
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.
OPA3_N	0: PC7		Operational Amplifier 3 external negative input.
OPA3_OUT	0: PD1		Operational Amplifier 3 output.
OPA3_P	0: PC6		Operational Amplifier 3 external positive input.

Table 5.24. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP1X																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT0Y	BUSACMP1Y																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.29. CSEN Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
CEXT																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
CEXT_SENSE																																	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.30. IDAC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT1Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	

Table 5.31. VDAC0 / OPA Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA0_N																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
OPA0_P																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	

Table 6.2. BGA192 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.20	
C1		6.00	
C2		6.00	
E1		0.4	
E2		0.4	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Table 7.1. BGA152 Package Dimensions

Dimension	Min	Typ	Max
A	0.78	0.84	0.90
A1	0.13	0.18	0.23
A3	0.16	0.20	0.24
A2		0.45 REF	
D		8.00 BSC	
e		0.50 BSC	
E		8.00 BSC	
D1		6.50 BSC	
E1		6.50 BSC	
b	0.20	0.25	0.30
aaa		0.10	
bbb		0.10	
ddd		0.08	
eee		0.15	
fff		0.05	

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Table 9.2. BGA112 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.45	
C1		8.00	
C2		8.00	
E1		0.8	
E2		0.8	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. TQFP100 Package Specifications

10.1 TQFP100 Package Dimensions

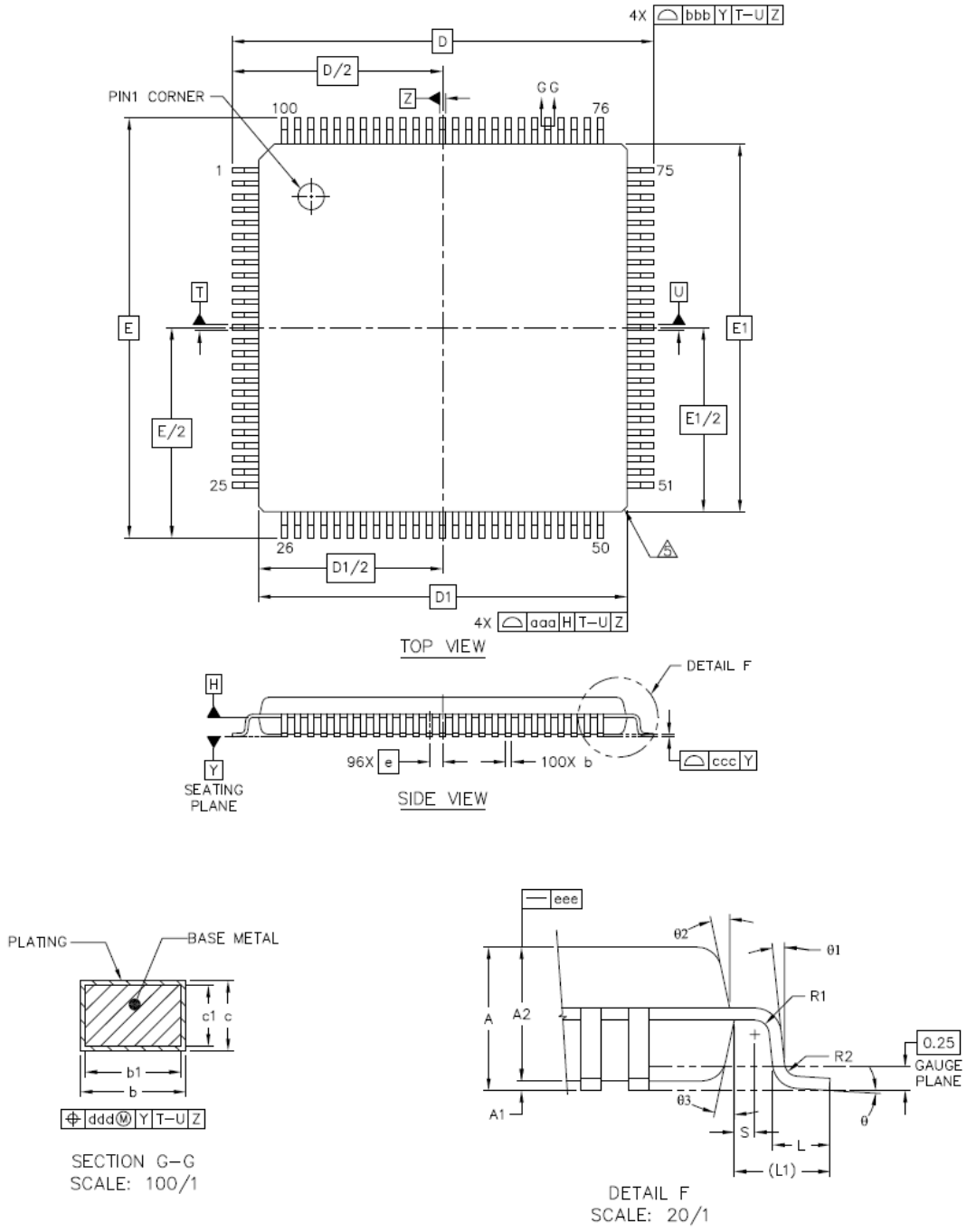


Figure 10.1. TQFP100 Package Drawing

Table 11.1. TQFP64 Package Dimensions

Dimension	Min	Typ	Max
A	—	1.15	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	—	0.20
c1	0.09	—	0.16
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
θ	0	3.5	7
Θ1	0	—	0.10
Θ2	11	12	13
Θ3	11	12	13

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.