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##### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	95
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b820f2048il120-br">https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b820f2048il120-br</a>

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**4.1.5 5V Regulator**

$V_{VREGI} = 5\text{ V}$ ,  $V_{VREGO} = 3.3\text{ V}$ ,  $C_{VREGI} = 10\text{ }\mu\text{F}$ ,  $C_{VREGO} = 4.7\text{ }\mu\text{F}$ , unless otherwise specified.

**Table 4.5. 5V Regulator**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VREGI or VBUS input voltage range	$V_{VREGI}$	Regulating output	2.7	—	5.5	V
		Bypass mode enabled	2.7	—	3.8	V
VREGO output voltage	$V_{VREGO}$	Regulating output, 3.3 V setting	3.1	3.3	3.5	V
		EM4S open-loop output, $I_{OUT} < 100\text{ }\mu\text{A}$	1.8	—	3.8	V
Voltage output step size	$V_{VREGO\_SS}$		—	0.1	—	V
Resistance in Bypass Mode	$R_{BYP}$	Bypass mode enabled	—	1.2	TBD	$\Omega$
Output current	$I_{OUT}$	EM0 or EM1, $V_{VREGI} > V_{VREGO} + 0.6\text{ V}$	—	—	200	mA
		EM0 or EM1, $V_{VREGI} > V_{VREGO} + 0.3\text{ V}$	—	—	100	mA
		EM2, EM3, or EM4H, $V_{VREGI} > V_{VREGO} + 0.6\text{ V}$	—	—	2	mA
		EM2, EM3, or EM4H, $V_{VREGI} > V_{VREGO} + 0.3\text{ V}$	—	—	0.5	mA
		EM4S	—	—	20	$\mu\text{A}$
Load regulation	$L_{R_{VREGO}}$	EM0 or EM1	—	0.10	—	$\text{mV/mA}$
		EM2, EM3, or EM4H	—	2.5	—	$\text{mV/mA}$
DC power supply rejection	$PSR_{DC}$		—	40	—	dB
VREGI or VBUS bypass capacitance	$C_{VREGI}$		—	10	—	$\mu\text{F}$
VREGO bypass capacitance	$C_{VREGO}$		1	4.7	10	$\mu\text{F}$
Supply current consumption	$I_{VREGI}$	EM0 or EM1, No load	—	29	—	$\mu\text{A}$
		EM2, EM3, or EM4H, No load	—	270	—	nA
		EM4S, No load	—	70	—	nA
VREGI and VBUS detection high threshold	$V_{DET\_H}$		TBD	1.18	—	V
VREGI and VBUS detection low threshold	$V_{DET\_L}$		—	1.12	TBD	V
Current monitor transfer ratio	$IMON_{XF}$	Translation of current through VREGO path to voltage at ADC input	—	0.35	—	$\text{mA/mV}$

**4.1.7.2 Current Consumption 3.3 V using DC-DC Converter**

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

**Table 4.8. Current Consumption 3.3 V using DC-DC Converter**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode <sup>2</sup>	IACTIVE_DCM	72 MHz HFRCO, CPU running Prime from flash	—	80	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	80	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	92	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	84	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	84	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	90	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	94	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	109	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	698	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode <sup>1</sup>	IACTIVE_CCM	72 MHz HFRCO, CPU running Prime from flash	—	84	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	84	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	95	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	91	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	92	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	104	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	113	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	142	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1264	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode <sup>3</sup>	I <sub>ACTIVE_LPM</sub>	32 MHz HFRCO, CPU running while loop from flash	—	82	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	83	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	88	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	257	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode <sup>1</sup>	I <sub>ACTIVE_CCM_VS</sub>	19 MHz HFRCO, CPU running while loop from flash	—	117	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1231	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode <sup>3</sup>	I <sub>ACTIVE_LPM_VS</sub>	19 MHz HFRCO, CPU running while loop from flash	—	72	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	219	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode <sup>2</sup>	I <sub>EM1_DCM</sub>	72 MHz HFRCO	—	42	—	µA/MHz
		50 MHz crystal	—	46	—	µA/MHz
		48 MHz HFRCO	—	46	—	µA/MHz
		32 MHz HFRCO	—	53	—	µA/MHz
		26 MHz HFRCO	—	57	—	µA/MHz
		16 MHz HFRCO	—	72	—	µA/MHz
		1 MHz HFRCO	—	663	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode <sup>3</sup>	I <sub>EM1_LPM</sub>	32 MHz HFRCO	—	42	—	µA/MHz
		26 MHz HFRCO	—	43	—	µA/MHz
		16 MHz HFRCO	—	48	—	µA/MHz
		1 MHz HFRCO	—	219	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode <sup>2</sup>	I <sub>EM1_DCM_VS</sub>	19 MHz HFRCO	—	60	—	µA/MHz
		1 MHz HFRCO	—	637	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode <sup>3</sup>	I <sub>EM1_LPM_VS</sub>	19 MHz HFRCO	—	39	—	µA/MHz
		1 MHz HFRCO	—	190	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode <sup>3</sup>	I <sub>EM2_VS</sub>	Full 512 kB RAM retention and RTCC running from LFXO	—	2.8	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	3.1	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO <sup>5</sup>	—	2.1	—	µA
Current consumption in EM3 mode, with voltage scaling enabled	I <sub>EM3_VS</sub>	Full 512 kB RAM retention and CRYOTIMER running from ULFR-CO	—	2.4	—	µA

## 4.1.10.4 High-Frequency RC Oscillator (HFRCO)

Table 4.15. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{HFRCO\_ACC}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	$t_{HFRCO}$	$f_{HFRCO} \geq 19 \text{ MHz}$	—	300	—	ns
		$4 < f_{HFRCO} < 19 \text{ MHz}$	—	1	—	$\mu\text{s}$
		$f_{HFRCO} \leq 4 \text{ MHz}$	—	2.5	—	$\mu\text{s}$
Maximum DPLL lock time <sup>1</sup>	$t_{DPLL\_LOCK}$	$f_{REF} = 32.768 \text{ kHz}$ , $f_{HFRCO} = 39.98 \text{ MHz}$ , $N = 1219$ , $M = 0$	—	183	—	$\mu\text{s}$
Current consumption on all supplies	$I_{HFRCO}$	$f_{HFRCO} = 72 \text{ MHz}$	—	608	TBD	$\mu\text{A}$
		$f_{HFRCO} = 64 \text{ MHz}$	—	545	TBD	$\mu\text{A}$
		$f_{HFRCO} = 56 \text{ MHz}$	—	478	TBD	$\mu\text{A}$
		$f_{HFRCO} = 48 \text{ MHz}$	—	413	TBD	$\mu\text{A}$
		$f_{HFRCO} = 38 \text{ MHz}$	—	341	TBD	$\mu\text{A}$
		$f_{HFRCO} = 32 \text{ MHz}$	—	286	TBD	$\mu\text{A}$
		$f_{HFRCO} = 26 \text{ MHz}$	—	240	TBD	$\mu\text{A}$
		$f_{HFRCO} = 19 \text{ MHz}$	—	191	TBD	$\mu\text{A}$
		$f_{HFRCO} = 16 \text{ MHz}$	—	164	TBD	$\mu\text{A}$
		$f_{HFRCO} = 13 \text{ MHz}$	—	143	TBD	$\mu\text{A}$
		$f_{HFRCO} = 7 \text{ MHz}$	—	103	TBD	$\mu\text{A}$
		$f_{HFRCO} = 4 \text{ MHz}$	—	42	TBD	$\mu\text{A}$
		$f_{HFRCO} = 2 \text{ MHz}$	—	33	TBD	$\mu\text{A}$
		$f_{HFRCO} = 1 \text{ MHz}$	—	28	TBD	$\mu\text{A}$
		$f_{HFRCO} = 72 \text{ MHz}$ , DPLL enabled	—	927	TBD	$\mu\text{A}$
		$f_{HFRCO} = 40 \text{ MHz}$ , DPLL enabled	—	526	TBD	$\mu\text{A}$
		$f_{HFRCO} = 32 \text{ MHz}$ , DPLL enabled	—	419	TBD	$\mu\text{A}$
		$f_{HFRCO} = 16 \text{ MHz}$ , DPLL enabled	—	233	TBD	$\mu\text{A}$
		$f_{HFRCO} = 4 \text{ MHz}$ , DPLL enabled	—	59	TBD	$\mu\text{A}$
		$f_{HFRCO} = 1 \text{ MHz}$ , DPLL enabled	—	36	TBD	$\mu\text{A}$
Coarse trim step size (% of period)	$SS_{HFRCO\_COARSE}$		—	0.8	—	%
Fine trim step size (% of period)	$SS_{HFRCO\_FINE}$		—	0.1	—	%
Period jitter	$PJ_{HFRCO}$		—	0.2	—	% RMS

4.1.23.2 I2C Fast-mode (Fm)<sup>1</sup>Table 4.32. I2C Fast-mode (Fm)<sup>1</sup>

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency <sup>2</sup>	f <sub>SCL</sub>		0	—	400	kHz
SCL clock low time	t <sub>LOW</sub>		1.3	—	—	μs
SCL clock high time	t <sub>HIGH</sub>		0.6	—	—	μs
SDA set-up time	t <sub>SU_DAT</sub>		100	—	—	ns
SDA hold time <sup>3</sup>	t <sub>HD_DAT</sub>		100	—	900	ns
Repeated START condition set-up time	t <sub>SU_STA</sub>		0.6	—	—	μs
(Repeated) START condition hold time	t <sub>HD_STA</sub>		0.6	—	—	μs
STOP condition set-up time	t <sub>SU_STO</sub>		0.6	—	—	μs
Bus free time between a STOP and START condition	t <sub>BUF</sub>		1.3	—	—	μs

**Note:**

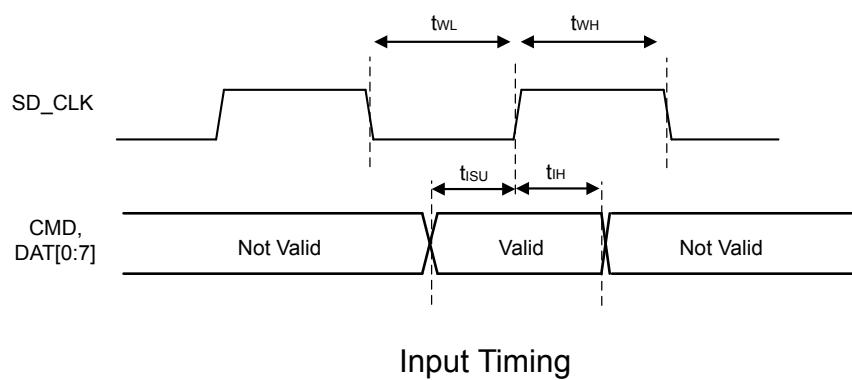
1. For CLHR set to 1 in the I2Cn\_CTRL register.
2. For the minimum HFFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t<sub>HD,DAT</sub>) needs to be met only when the device does not stretch the low time of SCL (t<sub>LOW</sub>).

## 4.1.24 USART SPI

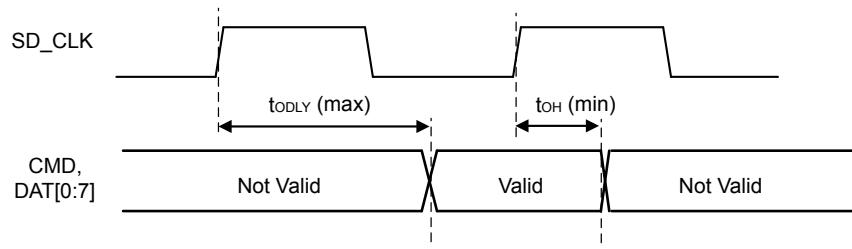
## SPI Master Timing

Table 4.34. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period <sup>1 3 2</sup>	t <sub>SCLK</sub>	All USARTs except USART2	2 * t <sub>HFFPERCLK</sub>	—	—	ns
		USART2	2 * t <sub>HFFPERBCLK</sub>	—	—	ns
CS to MOSI <sup>1 3</sup>	t <sub>CS_MO</sub>	USART2, location 4, IOVDD = 1.8 V	-3.2	—	6.8	ns
		USART2, location 4, IOVDD = 3.0 V	-2.3	—	6.0	ns
		USART2, location 5, IOVDD = 1.8 V	-8.1	—	6.3	ns
		USART2, location 5, IOVDD = 3.0 V	-7.3	—	4.4	ns
		All other USARTs and locations, IOVDD = 1.8 V	-15	—	13	ns
		All other USARTs and locations, IOVDD = 3.0 V	-13	—	11	ns
SCLK to MOSI <sup>1 3</sup>	t <sub>SCLK_MO</sub>	USART2, location 4, IOVDD = 1.8 V	-0.3	—	9.2	ns
		USART2, location 4, IOVDD = 3.0 V	-0.3	—	8.6	ns
		USART2, location 5, IOVDD = 1.8 V	-3.6	—	5.0	ns
		USART2, location 5, IOVDD = 3.0 V	-3.4	—	3.2	ns
		All other USARTs and locations, IOVDD = 1.8 V	-10	—	11	ns
		All other USARTs and locations, IOVDD = 3.0 V	-9	—	11	ns
MISO setup time <sup>1 3</sup>	t <sub>SU_MI</sub>	USART2, location 4, IOVDD = 1.8 V	39.7	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	22.4	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	49.2	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	30.0	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	55	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	36	—	—	ns



Input Timing



Output Timing

Figure 4.15. SDIO SDR Mode Timing

**SDIO MMC SDR Mode Timing at 1.8 V**

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD\_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO\_CTRL\_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

**Table 4.50. SDIO MMC SDR Mode Timing (Location 0, 1.8V I/O)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	FSD_CLK	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	25	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	tWL	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	tWH	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	tR		1.96	8.27	—	ns
Clock fall time	tF		1.67	6.90	—	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	tISU		5.3	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:7] change	tIH		2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	tODLY		0	—	16	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	tOH		3	—	—	ns

#### 4.1.28.2 QSPI DDR Mode

##### QSPI DDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 35, RX DLL = 70, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

**Table 4.56. QSPI DDR Mode Timing (Location 0)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Half SCLK period	T/2	HFXO	(1/F <sub>SCLK</sub> ) * 0.4 - 0.4	—	—	ns
		HFRCO, AUXHFRCO, USHFRCO	(1/F <sub>SCLK</sub> ) * 0.44	—	—	ns
Output valid	t <sub>ov</sub>		—	—	T/2 - 5.0	ns
Output hold	t <sub>OH</sub>		T/2 - 39.4	—	—	ns
Input setup	t <sub>SU</sub>		33.1	—	—	ns
Input hold	t <sub>H</sub>		-0.9	—	—	ns

## 5.2 EFM32GG11B8xx in BGA152 Device Pinout

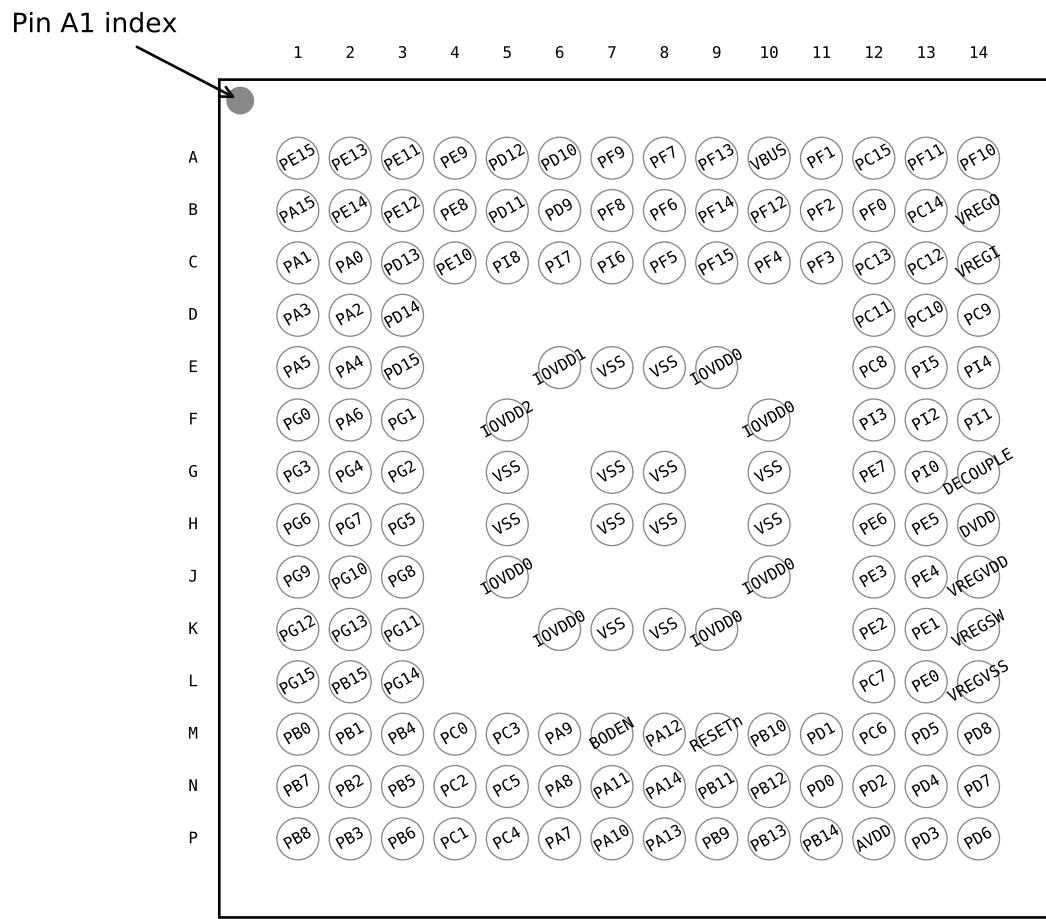


Figure 5.2. EFM32GG11B8xx in BGA152 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.2. EFM32GG11B8xx in BGA152 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE13	A2	GPIO
PE11	A3	GPIO	PE9	A4	GPIO
PD12	A5	GPIO	PD10	A6	GPIO
PF9	A7	GPIO	PF7	A8	GPIO
PF13	A9	GPIO (5V)	VBUS	A10	USB VBUS signal and auxiliary input to 5 V regulator.
PF1	A11	GPIO (5V)	PC15	A12	GPIO (5V)
PF11	A13	GPIO (5V)	PF10	A14	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF13	B9	GPIO (5V)
PF4	B10	GPIO	PF3	B11	GPIO
NC	B12	No Connect.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 L12 L15	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L16	Digital IO power supply 0.
PF2	C10	GPIO	PF1	C11	GPIO (5V)
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PF0	D11	GPIO (5V)
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PC9	E11	GPIO (5V)
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE6	F11	GPIO
PE7	F12	GPIO	PC8	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE3	G11	GPIO
PE4	G12	GPIO	PE5	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
DECOPPLE	H13	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PD14	J1	GPIO (5V)
PD15	J2	GPIO (5V)	PE1	J12	GPIO (5V)
VREGVDD	J13	Voltage regulator VDD input	PC0	K1	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE8	B4	GPIO	PD11	B5	GPIO
PF8	B6	GPIO	PF6	B7	GPIO
PF3	B8	GPIO	PE5	B9	GPIO
PC12	B10	GPIO (5V)	PC13	B11	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
PD12	C5	GPIO	PF9	C6	GPIO
VSS	C7 D4 F9 G3 G9 H6 K4 K7 K10 L7	Ground	PF2	C8	GPIO
PE6	C9	GPIO	PC10	C10	GPIO (5V)
PC11	C11	GPIO (5V)	PA3	D1	GPIO
PA2	D2	GPIO	PB15	D3	GPIO (5V)
IOVDD1	D5	Digital IO power supply 1.	PD9	D6	GPIO
IOVDD0	D7 G8 H7 L4	Digital IO power supply 0.	PF1	D8	GPIO (5V)
PE7	D9	GPIO	PC8	D10	GPIO (5V)
PC9	D11	GPIO (5V)	PA6	E1	GPIO
PA5	E2	GPIO	PA4	E3	GPIO
PB0	E4	GPIO	PF0	E8	GPIO (5V)
PE0	E9	GPIO (5V)	PE1	E10	GPIO (5V)
PE3	E11	GPIO	PB1	F1	GPIO
PB2	F2	GPIO	PB3	F3	GPIO
PB4	F4	GPIO	DVDD	F8	Digital power supply.
PE2	F10	GPIO	DECOPPLE	F11	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PB5	G1	GPIO	PB6	G2	GPIO
IOVDD2	G4	Digital IO power supply 2.	PC6	G10	GPIO
PC7	G11	GPIO	PC0	H1	GPIO (5V)
PC2	H2	GPIO (5V)	PD14	H3	GPIO (5V)
PA7	H4	GPIO	PA8	H5	GPIO
PD8	H8	GPIO	PD5	H9	GPIO
PD6	H10	GPIO	PD7	H11	GPIO

## 5.8 EFM32GG11B8xx in QFP100 Device Pinout

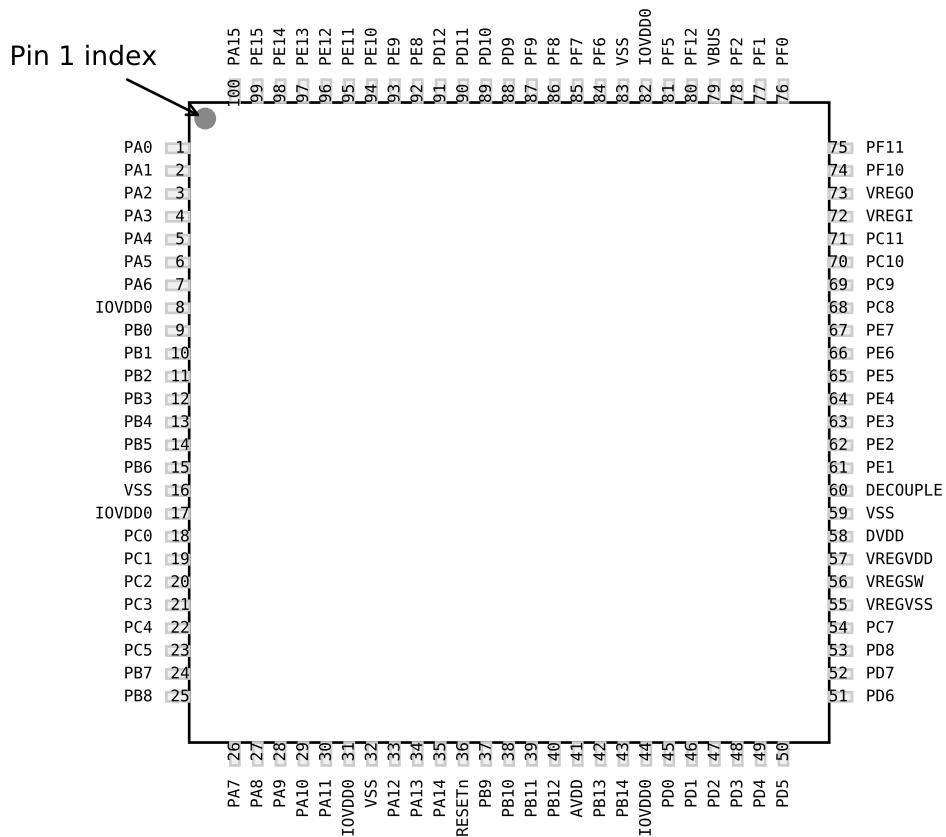


Figure 5.8. EFM32GG11B8xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.8. EFM32GG11B8xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

## 5.14 EFM32GG11B4xx in QFP64 Device Pinout

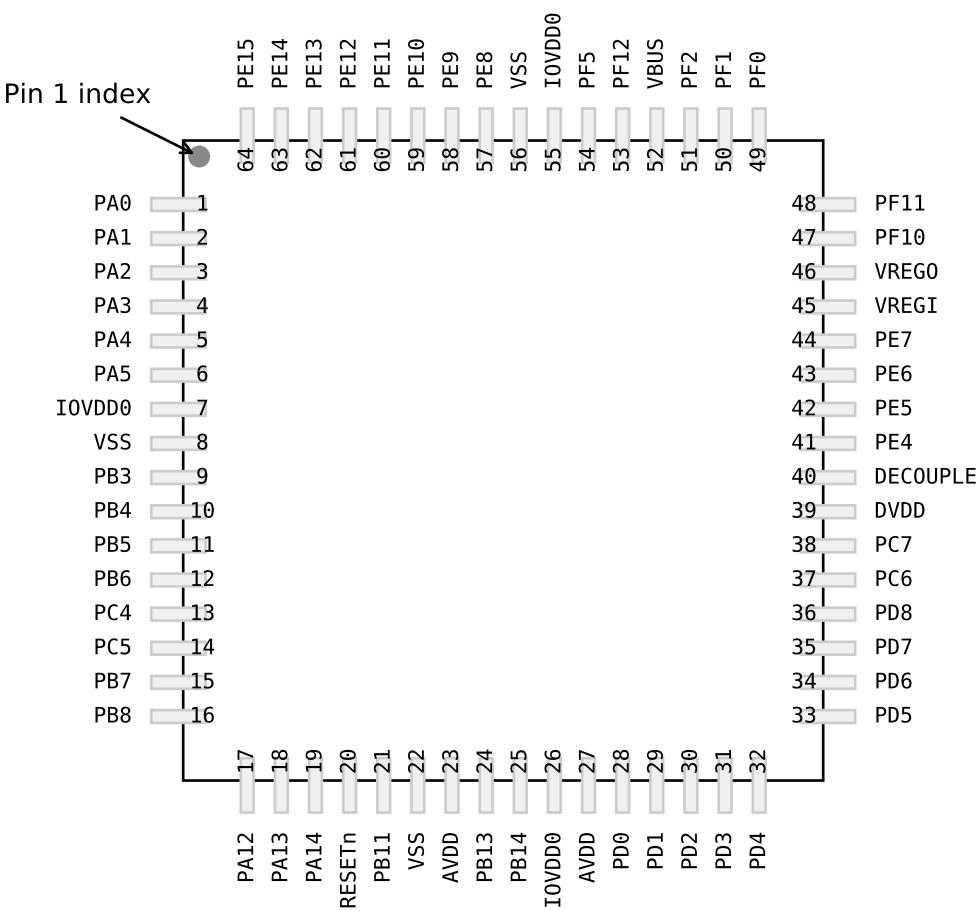


Figure 5.14. EFM32GG11B4xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.14. EFM32GG11B4xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PH11	BUSACMP3Y BU-SACMP3X	EBI_A23 #2	TIM5_CC1 #1 WTIM1_CC3 #6	US5_RX #3 U1_TX #5 I2C1_SDA #5	
PH13	BUSACMP3Y BU-SACMP3X	EBI_A25 #2	TIM5_CC0 #2 WTIM1_CC1 #7 PCNT2_S1IN #7	US5_CS #3 U1_CTS #5 I2C1_SDA #6	
PD0	VDAC0_OUT0ALT / OPA0_OUTALT #4 OPA2_OUTALT BU-SADC0Y BUSADC0X	EBI_A04 #1 EBI_A13 #3	TIM4_CDTI0 TIM6_CC2 #5 WTIM1_CC2 #0 PCNT2_S0IN #0	CAN0_RX #2 US1_TX #1	
PD3	BUSADC0Y BU-SADC0X OPA2_N	EBI_A07 #1 EBI_A16 #3	TIM4_CDTI2 TIM0_CC2 #2 TIM6_CC2 #6 WTIM1_CC1 #1 WTIM2_CC0 #5	CAN1_RX #2 US1_CS #1 LEU1_RX #2	ETM_TD1 #0 ETM_TD1 #2
PD8	BU_VIN	EBI_A12 #1	WTIM1_CC2 #2	US2_RTS #5	CMU_CLK1 #1 PRS_CH12 #2 ACMP2_O #0
PB7	LFXTAL_P		TIM0_CDTI0 #4 TIM1_CC0 #3	US0_TX #4 US1_CLK #0 US3_RX #2 US4_TX #0 U0_CTS #4	PRS_CH22 #0
PC3	VDAC0_OUT0ALT / OPA0_OUTALT #3 BUSACMP0Y BU-SACMP0X	EBI_AD10 #1 EBI_CS3 #2 EBI_BL1 #3 EBI_NANDREn #0	TIM0_CDTI1 #3 TIM2_CC1 #5 WTIM0_CC2 #7 LE-TIM1_OUT1 #3	ETH_TSUTMRTOG #2 CAN1_TX #0 US1_CLK #4 US2_RX #0	LES_CH3 PRS_CH11 #1
PC5	BUSACMP0Y BU-SACMP0X OPA0_N	EBI_AD12 #1 EBI_WEn #2 EBI_NANDWEn #0 EBI_A00 #3	TIM0_CC1 #5 LE-TIM0_OUT1 #3 PCNT1_S1IN #3	SDIO_WP #1 US2_CS #0 US4_CS #0 U0_RX #4 U1_RTS #4 I2C1_SCL #0	LES_CH5 PRS_CH19 #2
PA9	BUSAY BUSBX LCD_SEG37	EBI_AD15 #1 EBI_A03 #3 EBI_DTen #0	TIM2_CC1 #0 TIM0_CC1 #6 WTIM2_CC0 #0 LE-TIM0_OUT1 #6	US2_CLK #2	PRS_CH9 #0
PB10	BUSBY BUSAX	EBI_BL0 #2 EBI_A01 #1 EBI_A04 #0 EBI_A10 #3	WTIM2_CC1 #2 LE-TIM0_OUT1 #7	SDIO_CD #3 CAN0_TX #3 US1_RTS #0 US2_CTS #3 U1_RX #2	PRS_CH9 #2 ACMP1_O #6
PH0	BUSADC1Y BU-SADC1X	EBI_DCLK #2	WTIM2_CC2 #4	US0_CTS #6 LEU1_TX #5	
PH3	BUSADC1Y BU-SADC1X	EBI_HSNC #2	TIM6_CC1 #3	US1_RTS #6	
PH6	BUSADC1Y BU-SADC1X	EBI_A18 #2	TIM6_CDTI1 #3 WTIM2_CC2 #6	US4_CLK #4	
PH9	BUSACMP3Y BU-SACMP3X	EBI_A21 #2	TIM6_CC1 #4 WTIM1_CC1 #6 WTIM2_CC2 #7	US4_RTS #4	
PH12	BUSACMP3Y BU-SACMP3X	EBI_A24 #2	TIM5_CC2 #1 WTIM1_CC0 #7	US5_CLK #3 U1_RX #5 I2C1_SCL #5	

Table 5.24. ACMP1 Bus and Pin Mapping

	APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP1Y	BUSACMP1X	BUS	CH31
PF15	PF15			PB15		PB15					CH30
PF14		PF14		PB14			PB14				CH29
PF12		PF12		PB12		PB13	PB13				CH28
PF10		PF11	PF13	PB10	PB11	PB11	PB12				CH27
PF8		PF9	PF9	PB9	PB9	PB9	PB10				CH26
PF6		PF7	PF7	PB6	PB6	PB6	PB6				CH25
PF4		PF5	PF5	PB4	PB4	PB5	PB5	PB4			CH24
PF2		PF3	PF3	PB2	PB2	PB3	PB3	PB2			CH23
PF0		PF1	PF1	PB0	PB0	PB1	PB1	PB0			CH22
PE14		PE15	PE15	PA14	PA14	PA15	PA15	PA14			CH20
PE12		PE13	PE13	PA12	PA12	PA13	PA13	PA12			CH19
PE10		PE11	PE11	PA10	PA10	PA11	PA11	PA10			CH18
PE8		PE9	PE9	PA8	PA8	PA9	PA9	PA8			CH17
PE6		PE7	PE7	PA6	PA6	PA5	PA5	PA6	PC14	PC14	CH16
PE4		PE5	PE5	PA4	PA4	PA3	PA3	PA4	PC13	PC13	CH15
				PA2		PA2		PA2	PC12	PC12	CH14
		PE1	PE1	PA1	PA1	PA1	PA1	PA0	PC11	PC11	CH13
PE0			PE0	PA0					PC10	PC10	CH12
									PC9	PC9	CH11
									PC8	PC8	CH10

Table 5.31. VDAC0 / OPA Bus and Pin Mapping

											Port
<b>OPA0_N</b>											<b>Bus</b>
APORT4X	APORT3X	APORT2X	APORT1X	APORT4Y	APORT3Y	APORT2Y	APORT1Y				
BUSDX	BUSCX	BUSBX	BUSAX	BUSDY	BUSCY	BUSBY	BUSAY				
PF15		PB15		PF15				PB15			CH31
PF14	PF13	PB13		PF14		PB14					CH30
PF12	PF11	PB11		PF12		PB12					CH29
PF10	PF9	PB10		PF10		PB10					CH28
PF8	PF7		PB9	PF9		PB9					CH27
PF6	PF5	PF6	PB6	PF6		PB6					CH26
PF4	PF3	PF4	PB4	PF4		PB4					CH25
PF2	PF1	PF2	PB2	PF2		PB2					CH24
PE15	PE14	PE15	PE13	PE14	PE14	PE14	PE14				CH23
PE13	PE12	PE14	PA13	PE13	PE13	PE13	PA13				CH22
PE11	PE10	PE12	PA12	PE12	PE12	PA12					CH21
PE9	PE8	PE10	PA10	PE10	PE10	PA10					CH20
PE7	PE6	PE9	PA9	PE9	PE9	PA9					CH19
PE5	PE4	PE8	PA8	PE8	PE8	PA8					CH18
PE3	PE2	PE5	PA5	PE7	PE7	PA7					CH17
PE1	PE0	PE3	PA3	PE6	PE6	PA6					CH16
		PE0	PA0	PE5	PE5	PA5					CH15
				PE4	PE4	PA4					CH14
				PA3	PA3	PA3					CH13
				PA2	PA2	PA2					CH12
				PA1	PA1	PA1					CH11
				PA0	PA0	PA0					CH10
											CH9
											CH8
											CH7
											CH6
											CH5
											CH4
											CH3
											CH2
											CH1
											CH0

**Table 6.1. BGA192 Package Dimensions**

<b>Dimension</b>	<b>Min</b>	<b>Typ</b>	<b>Max</b>
A	0.77	0.83	0.89
A1	0.13	0.18	0.23
A3	0.16	0.20	0.24
A2		0.45 REF	
D		7.00 BSC	
e		0.40 BSC	
E		7.00 BSC	
D1		6.00 BSC	
E1		6.00 BSC	
b	0.20	0.25	0.30
aaa		0.10	
bbb		0.10	
ddd		0.08	
eee		0.15	
fff		0.05	
<b>Note:</b>			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.			