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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	152-VFBGA
Supplier Device Package	152-BGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b820f2048il152-a

1. Feature List

The EFM32GG11 highlighted features are listed below.

- **ARM Cortex-M4 CPU platform**
 - High performance 32-bit processor @ up to 72 MHz
 - DSP instruction support and Floating Point Unit
 - Memory Protection Unit
 - Wake-up Interrupt Controller
- **Flexible Energy Management System**
 - 80 μ A/MHz in Active Mode (EM0)
 - 2.1 μ A EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Up to 2048 kB flash program memory**
 - Dual-bank with read-while-write support
- **Up to 512 kB RAM data memory**
 - 256 kB with ECC (SEC-DED)
- **Octal/Quad-SPI Flash Memory Interface**
 - Supports 3 V and 1.8 V memories
 - 1/2/4/8-bit data bus
 - Quad-SPI Execute In Place (XIP)
- **Communication Interfaces**
 - Low-energy Universal Serial Bus (USB) with Device and Host support
 - Fully USB 2.0 compliant
 - On-chip PHY and embedded 5V to 3.3V regulator
 - Crystal-free Device mode operation
 - Patent-pending Low-Energy Mode (LEM)
 - SD/MMC/SDIO Host Controller
 - SD v3.01, SDIO v3.0 and MMC v4.51
 - 1/4/8-bit bus width
 - 10/100 Ethernet MAC with MII/RMII interface
 - IEEE1588-2008 precision time stamping
 - Energy Efficient Ethernet (802.3az)
 - Up to 2 $\times$ CAN Bus Controller
 - Version 2.0A and 2.0B up to 1 Mbps
 - 6 $\times$ Universal Synchronous/Asynchronous Receiver/ Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
 - Triple buffered full/half-duplex operation with flow control
 - Ultra high speed (36 MHz) operation on one instance
 - 2 $\times$ Universal Asynchronous Receiver/ Transmitter
 - 2 $\times$ Low Energy UART
 - Autonomous operation with DMA in Deep Sleep Mode
 - 3 $\times$ I²C Interface with SMBus support
 - Address recognition in EM3 Stop Mode
- **Up to 144 General Purpose I/O Pins**
 - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - 5 V tolerance on select pins
 - Asynchronous external interrupts
 - Output state retention and wake-up from Shutoff Mode
- **Up to 24 Channel DMA Controller**
- **Up to 24 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **External Bus Interface for up to 4x256 MB of external memory mapped space**
 - TFT Controller with Direct Drive
 - Per-pixel alpha-blending engine
- **Hardware Cryptography**
 - AES 128/256-bit keys
 - ECC B/K163, B/K233, P192, P224, P256
 - SHA-1 and SHA-2 (SHA-224 and SHA-256)
 - True Random Number Generator (TRNG)
- **Hardware CRC engine**
 - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
 - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8 $\times$ 36 segments**
 - Voltage boost, contrast and autonomous animation
 - Patented low-energy LCD driver
- **Backup Power Domain**
 - RTCC and retention registers in a separate power domain, available down to energy mode EM4H
 - Operation from backup battery when main power absent/ insufficient
- **Ultra Low-Power Precision Analog Peripherals**
 - 2 $\times$ 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
 - On-chip temperature sensor
 - 2 $\times$ 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
 - Digital to Analog Current Converter (IDAC)
 - Up to 4 $\times$ Analog Comparator (ACMP)
 - Up to 4 $\times$ Operational Amplifier (OPAMP)
 - Robust current-based capacitive sensing with up to 64 inputs and wake-on-touch (CSEN)
 - Up to 108 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
 - Supply Voltage Monitor

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4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on $T_{AMB}=25\text{ }^{\circ}\text{C}$ and $V_{DD}=3.3\text{ V}$, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to [4.1.2.1 General Operating Conditions](#) for more details about operational supply and temperature limits.

4.1.7.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.9. Current Consumption 1.8 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I _{ACTIVE}	72 MHz HFRCO, CPU running Prime from flash	—	120	—	μA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	120	—	μA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	140	—	μA/MHz
		50 MHz crystal, CPU running while loop from flash	—	122	—	μA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	122	—	μA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	124	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	126	—	μA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	131	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	315	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I _{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	107	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	259	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled	I _{EM1}	72 MHz HFRCO	—	57	—	μA/MHz
		50 MHz crystal	—	59	—	μA/MHz
		48 MHz HFRCO	—	59	—	μA/MHz
		32 MHz HFRCO	—	61	—	μA/MHz
		26 MHz HFRCO	—	63	—	μA/MHz
		16 MHz HFRCO	—	68	—	μA/MHz
		1 MHz HFRCO	—	252	—	μA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I _{EM1_VS}	19 MHz HFRCO	—	55	—	μA/MHz
		1 MHz HFRCO	—	207	—	μA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I _{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.7	—	μA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	4.0	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO ²	—	2.5	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD. 2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$. 3. ± 100 mV differential drive. 4. In ACMPn_CTRL register. 5. In ACMPn_HYSTERESIS registers. 6. In ACMPn_INPUTSEL register.						

SPI Slave Timing

Table 4.35. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 3 2}	t_{SCLK}		6 * t_{HFERCLK}	—	—	ns
SCLK high time ^{1 3 2}	$t_{\text{SCLK_HI}}$		2.5 * t_{HFERCLK}	—	—	ns
SCLK low time ^{1 3 2}	$t_{\text{SCLK_LO}}$		2.5 * t_{HFERCLK}	—	—	ns
CS active to MISO ^{1 3}	$t_{\text{CS_ACT_MI}}$		24	—	69	ns
CS disable to MISO ^{1 3}	$t_{\text{CS_DIS_MI}}$		19	—	175	ns
MOSI setup time ^{1 3}	$t_{\text{SU_MO}}$		7	—	—	ns
MOSI hold time ^{1 3 2}	$t_{\text{H_MO}}$		6	—	—	ns
SCLK to MISO ^{1 3 2}	$t_{\text{SCLK_MI}}$		16 + 1.5 * t_{HFERCLK}	—	43 + 2.5 * t_{HFERCLK}	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. t_{HFERCLK} is one period of the selected HFERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

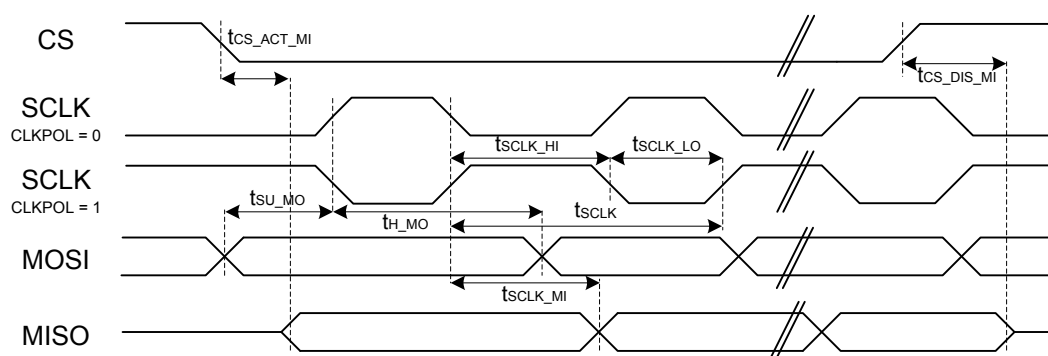


Figure 4.2. SPI Slave Timing Diagram

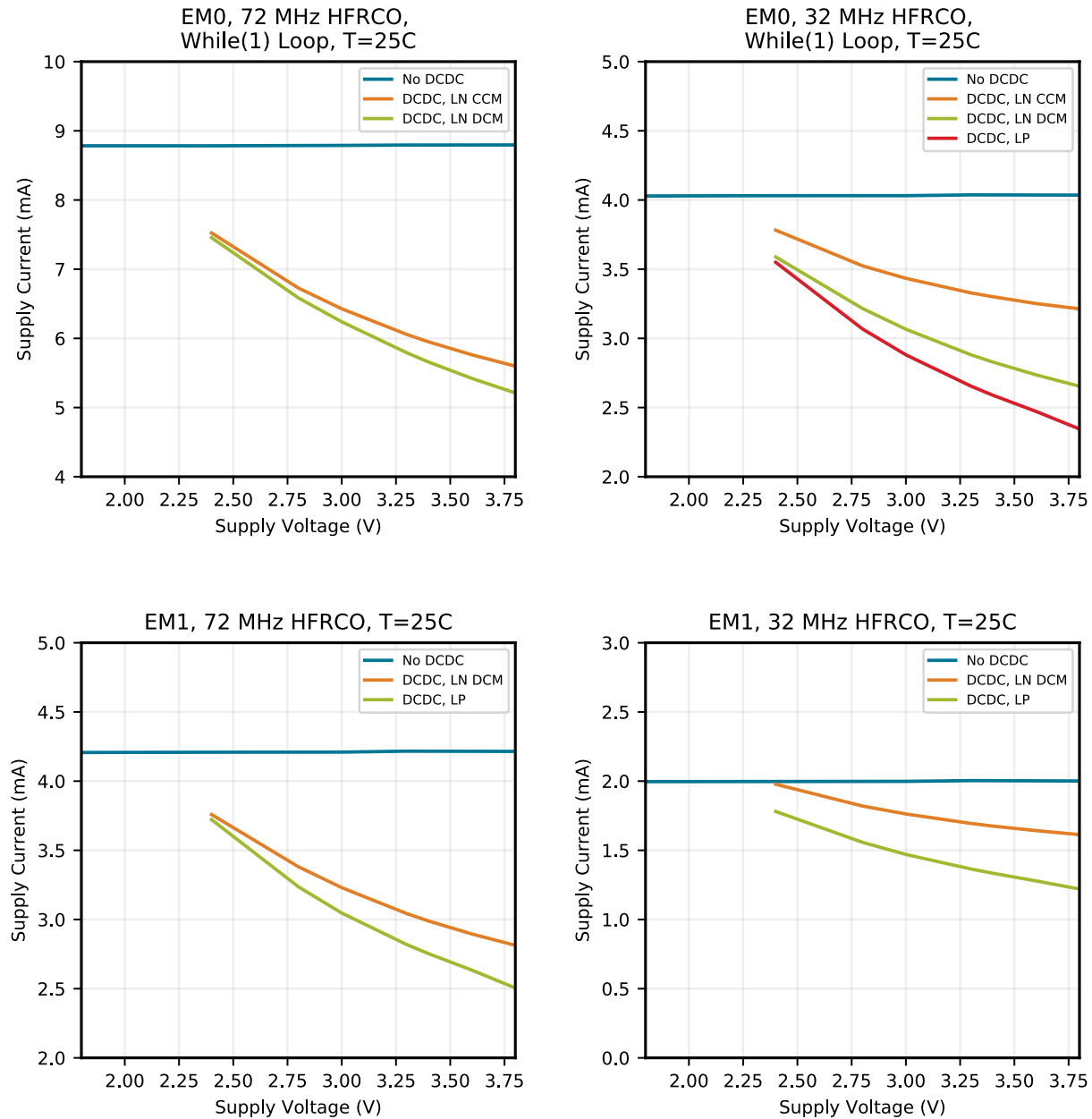


Figure 4.27. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
IOVDD1	F7 G7	Digital IO power supply 1.	VSS	F8 G8 G9 H6 H7 H8 H9 H10 H11 J6 J7 J8 J9 J10 J11 K8 K9 L8 L9	Ground
NC	F9	No Connect.	IOVDD0	F10 F11 G10 G11 K6 K7 K10 K11 L6 L7 L10 L11	Digital IO power supply 0.
PI5	F14	GPIO (5V)	PI4	F15	GPIO (5V)
PI3	F16	GPIO (5V)	PA5	G1	GPIO
PG6	G2	GPIO (5V)	PG5	G3	GPIO (5V)
PI2	G14	GPIO (5V)	PI1	G15	GPIO (5V)
PI0	G16	GPIO (5V)	PA6	H1	GPIO
PG8	H2	GPIO (5V)	PG7	H3	GPIO (5V)
PE5	H14	GPIO	PE6	H15	GPIO
PE7	H16	GPIO	PG11	J1	GPIO (5V)
PG10	J2	GPIO (5V)	PG9	J3	GPIO (5V)
PE3	J14	GPIO	PE4	J15	GPIO
DECOUPLE	J16	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PG14	K1	GPIO
PG13	K2	GPIO	PG12	K3	GPIO
PE1	K14	GPIO (5V)	PE2	K15	GPIO
DVDD	K16	Digital power supply.	PG15	L1	GPIO (5V)
PB15	L2	GPIO (5V)	PB0	L3	GPIO
PE0	L14	GPIO (5V)	PC7	L15	GPIO
VREGVDD	L16	Voltage regulator VDD input	PB1	M1	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVDD	J13	Voltage regulator VDD input	PC0	K1	GPIO (5V)
PC1	K2	GPIO (5V)	PE0	K12	GPIO (5V)
VREGSW	K13	DCDC regulator switching node	PC2	L1	GPIO (5V)
PC3	L2	GPIO (5V)	PA7	L3	GPIO
PB9	L13	GPIO (5V)	PB10	L14	GPIO (5V)
PD1	L17	GPIO	PC6	L18	GPIO
PC7	L19	GPIO	VREGVSS	L20	Voltage regulator VSS
PB7	M1	GPIO	PC4	M2	GPIO
PA8	M3	GPIO	PA10	M4	GPIO
PA13	M5	GPIO (5V)	PA14	M6	GPIO
RESETn	M7	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB12	M8	GPIO
PD0	M9	GPIO (5V)	PD2	M10	GPIO (5V)
PD3	M11	GPIO	PD4	M12	GPIO
PD8	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	BODEN	N7	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.
PB13	N8	GPIO	PB14	N9	GPIO
AVDD	N10	Analog power supply.	PD5	N11	GPIO
PD6	N12	GPIO	PD7	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA12	18	GPIO (5V)	PA13	19	GPIO (5V)
PA14	20	GPIO	RESETn	21	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	22	GPIO	PB12	23	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD7	35	GPIO	PD8	36	GPIO
PC7	37	GPIO	VREGVSS	38	Voltage regulator VSS
VREGSW	39	DCDC regulator switching node	VREGVDD	40	Voltage regulator VDD input
DVDD	41	Digital power supply.	DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	43	GPIO	PE5	44	GPIO
PE6	45	GPIO	PE7	46	GPIO
PC12	47	GPIO (5V)	PC13	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	PF3	52	GPIO
PF4	53	GPIO	PF5	54	GPIO
PE8	56	GPIO	PE9	57	GPIO
PE10	58	GPIO	PE11	59	GPIO
PE12	60	GPIO	PE13	61	GPIO
PE14	62	GPIO	PE15	63	GPIO
PA15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.18 EFM32GG11B4xx in QFN64 Device Pinout

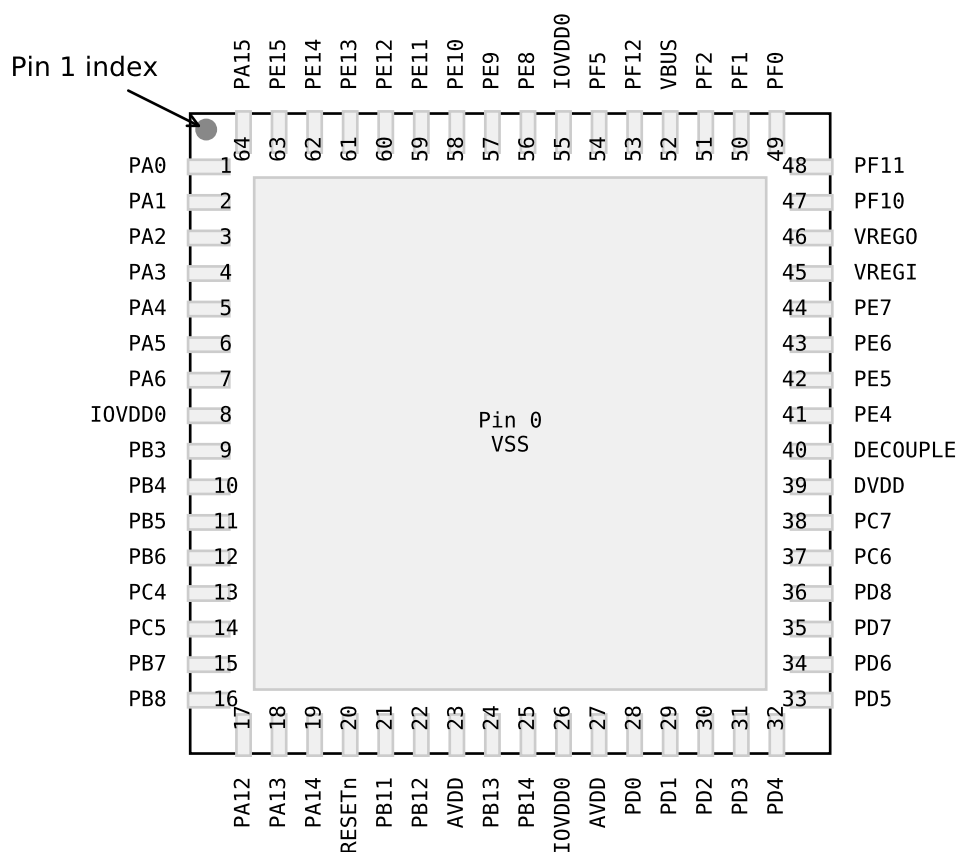


Figure 5.18. EFM32GG11B4xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.18. EFM32GG11B4xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO (5V)
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	VREGI	45	Input to 5 V regulator.
VREGO	46	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs	PF10	47	GPIO (5V)
PF11	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO (5V)
PC9	42	GPIO (5V)	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF14	BUSDY BUSCX		TIM1_CC1 #6 TIM4_CC1 #1 TIM5_CC2 #7 WTIM3_CC1 #7	I2C2_SCL #4	
PF11	BUSCY BUSDX	EBI_NANDWE _n #5	TIM5_CC2 #6 WTIM3_CC2 #3 PCNT2_S1IN #3	US5_CTS #2 U1_RX #1 I2C2_SCL #2 USB_DP	
PF10	BUSDY BUSCX	EBI_ARDY #5	TIM5_CC1 #6 WTIM3_CC1 #3 PCNT2_S0IN #3	US5_RTS #2 U1_TX #1 I2C2_SDA #2 USB_DM	
PF0	BUSDY BUSCX	EBI_A24 #1	TIM0_CC0 #4 WTIM0_CC1 #4 LE- TIM0_OUT0 #2	US2_TX #5 CAN0_RX #1 US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	PRS_CH15 #2 ACMP3_O #0 DBG_SWCLKTCK BOOT_TX
PA0	BUSBY BUSAX LCD_SEG13	EBI_AD09 #0 EBI_CSTFT #3	TIM0_CC0 #0 TIM0_CC1 #7 TIM3_CC0 #4 PCNT0_S0IN #4	ETH_RMIITXEN #0 ETH_MII_TXCLK #0 SDIO_DAT0 #1 US1_RX #5 US3_TX #0 QSPI0_CS0 #1 LEU0_RX #4 I2C0_SDA #0	CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
PD11	LCD_SEG30	EBI_CS2 #0 EBI_HSNC #1	TIM4_CC0 #6 WTIM3_CC2 #0	ETH_RMIICRS _{SDV} #1 SDIO_DAT5 #0 QSPI0_DQ2 #0 ETH_MII_RXD3 #2 US4_CLK #1	
PD10	LCD_SEG29	EBI_CS1 #0 EBI_VSNC #1	TIM4_CC2 #5 WTIM3_CC1 #0	ETH_RMIIREFCLK #1 SDIO_DAT6 #0 QSPI0_DQ1 #0 ETH_MII_RXD2 #2 US4_RX #1	CMU_CLK2 #5 CMU_CLKI0 #5
PD9	LCD_SEG28	EBI_CS0 #0 EBI_DTEN #1	TIM4_CC1 #5 WTIM3_CC0 #0	ETH_RMIIRXD0 #1 SDIO_DAT7 #0 QSPI0_DQ0 #0 ETH_MII_RXD1 #2 US4_TX #1	
PF9	BUSCY BUSDX LCD_SEG27	EBI_RE _n #4 EBI_BL1 #1	TIM4_CC0 #5	ETH_RMIIRXD1 #1 US2_CS #4 QSPI0_DQS #0 ETH_MII_RXD0 #2 ETH_TSUTMRTOG #3 SDIO_WP #0 U0_RTS #0 U1_CTS #1	ETM_TD0 #1
PF8	BUSDY BUSCX LCD_SEG26	EBI_WE _n #4 EBI_BL0 #1	TIM0_CC2 #1 TIM4_CC2 #4	ETH_RMIITXEN #1 US2_CLK #4 QSPI0_CS1 #0 ETH_MII_RXDV #2 ETH_TSUEXTCLK #3 SDIO_CD #0 U0_CTS #0 U1_RTS #1	ETM_TCLK #1 GPIO_EM4WU8

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD13		EBI_ARDY #1	TIM2_CDTI0 #1 TIM3_CC1 #6 WTIM0_CC1 #1	ETH_MDIO #1 US4_CTS #1 US5_CLK #1	ETM_TD1 #1
PI15				CAN1_TX #7 US3_CS #5	
PI14				CAN1_RX #7 US3_CLK #5	
PI13				CAN0_TX #7 US3_RX #5	
PI12				CAN0_RX #7 US3_TX #5	
PI10		EBI_A15 #2	TIM4_CC2 #3	US4_CTS #3	
PI7		EBI_A12 #2	TIM1_CC1 #7 TIM4_CC2 #2 WTIM3_CC1 #5	US4_RX #3	
PF15	BUSCY BUSDX		TIM1_CC2 #6 TIM4_CC2 #1 WTIM3_CC2 #7	US5_TX #2 I2C2_SDA #5	
PF12	BUSDY BUSCX	EBI_NANDREn #5	TIM4_CC2 #0 TIM1_CC3 #5 TIM5_CC0 #7 WTIM3_CC2 #6	US5_CS #2 I2C2_SCL #3 USB_ID	
PF4	BUSDY BUSCX LCD_SEG2	EBI_WEn #0 EBI_WEn #5	TIM4_CC1 #0 TIM0_CDTI1 #2 TIM1_CC2 #5 WTIM3_CC1 #6	US1_RTS #2 I2C2_SDA #3	PRS_CH1 #1
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BUSACMP1Y BU- SACMP1X	EBI_NANDREn #4	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LE- TIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 U1_RTS #0 LEU0_RX #5 I2C2_SCL #1	LES_CH15 PRS_CH1 #2 ACMP3_O #1 DBG_SWO #1
PC14	VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSACMP1Y BU- SACMP1X	EBI_NANDWEn #4	TIM0_CDTI1 #1 TIM1_CC1 #0 TIM1_CC3 #4 TIM5_CC0 #6 WTIM3_CC0 #3 LE- TIM0_OUT0 #5 PCNT0_S1IN #0	US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 U1_CTS #0 LEU0_TX #5 I2C2_SDA #1	LES_CH14 PRS_CH0 #2 ACMP3_O #2
PA2	BUSBY BUSAX LCD_SEG15	EBI_AD11 #0 EBI_DTEN #3	TIM0_CC2 #0 TIM3_CC2 #4	ETH_RMIIRXD0 #0 ETH_MIITXD2 #0 SDIO_DAT2 #1 US1_RX #6 US3_CLK #0 QSPIO_DQ0 #1	CMU_CLK0 #0 PRS_CH8 #1 ETM_TD0 #3
PG0	BUSACMP2Y BU- SACMP2X	EBI_AD00 #2	TIM6_CC0 #0 TIM2_CDTI0 #3 WTIM0_CDTI1 #1 LETIM1_OUT0 #6	ETH_MIITXCLK #1 US3_TX #4 QSPIO_SCLK #2	CMU_CLK2 #3

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_AD08	0: PA15 1: PC1 2: PG8		External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	0: PA0 1: PC2 2: PG9		External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	0: PA1 1: PC3 2: PG10		External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	0: PA2 1: PC4 2: PG11		External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	0: PA3 1: PC5 2: PG12		External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	0: PA4 1: PA7 2: PG13		External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	0: PA5 1: PA8 2: PG14		External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	0: PA6 1: PA9 2: PG15		External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	0: PF3 1: PB9 2: PC4 3: PB5	4: PC11 5: PC11	External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	0: PF2 1: PD13 2: PB15 3: PB4	4: PC13 5: PF10	External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	0: PF6 1: PF8 2: PB10 3: PC1	4: PF6 5: PF6	External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	0: PF7 1: PF9 2: PB11 3: PC3	4: PF7 5: PF7	External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	0: PD9 1: PA10 2: PC0 3: PB0	4: PE8	External Bus Interface (EBI) Chip Select output 0.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
GPIO_EM4WU7	0: PB11		Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PF8		Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PE10		Pin can be used to wake the system up from EM4
HFX TAL_N	0: PB14		High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	0: PB13		High Frequency Crystal positive pin.
I2C0_SCL	0: PA1 1: PD7 2: PC7 3: PD15	4: PC1 5: PF1 6: PE13 7: PE5	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PD6 2: PC6 3: PD14	4: PC0 5: PF0 6: PE12 7: PE4	I2C0 Serial Data input / output.
I2C1_SCL	0: PC5 1: PB12 2: PE1 3: PD5	4: PF2 5: PH12 6: PH14 7: PI3	I2C1 Serial Clock Line input / output.
I2C1_SDA	0: PC4 1: PB11 2: PE0 3: PD4	4: PC11 5: PH11 6: PH13 7: PI2	I2C1 Serial Data input / output.
I2C2_SCL	0: PF5 1: PC15 2: PF11 3: PF12	4: PF14 5: PF3 6: PC13 7: PI5	I2C2 Serial Clock Line input / output.
I2C2_SDA	0: PE8 1: PC14 2: PF10 3: PF4	4: PF13 5: PF15 6: PC12 7: PI4	I2C2 Serial Data input / output.
IDAC0_OUT	0: PB11		IDAC0 output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PRS_CH20	0: PB4 1: PC12 2: PE2		Peripheral Reflex System PRS, channel 20.
PRS_CH21	0: PB5 1: PC13 2: PB11		Peripheral Reflex System PRS, channel 21.
PRS_CH22	0: PB7 1: PE0 2: PF6		Peripheral Reflex System PRS, channel 22.
PRS_CH23	0: PB8 1: PE1 2: PF7		Peripheral Reflex System PRS, channel 23.
QSPI0_CS0	0: PF7 1: PA0 2: PG9		Quad SPI 0 Chip Select 0.
QSPI0_CS1	0: PF8 1: PA1 2: PG10		Quad SPI 0 Chip Select 1.
QSPI0_DQ0	0: PD9 1: PA2 2: PG1		Quad SPI 0 Data 0.
QSPI0_DQ1	0: PD10 1: PA3 2: PG2		Quad SPI 0 Data 1.
QSPI0_DQ2	0: PD11 1: PA4 2: PG3		Quad SPI 0 Data 2.
QSPI0_DQ3	0: PD12 1: PA5 2: PG4		Quad SPI 0 Data 3.
QSPI0_DQ4	0: PE8 1: PB3 2: PG5		Quad SPI 0 Data 4.
QSPI0_DQ5	0: PE9 1: PB4 2: PG6		Quad SPI 0 Data 5.
QSPI0_DQ6	0: PE10 1: PB5 2: PG7		Quad SPI 0 Data 6.

10.2 TQFP100 PCB Land Pattern

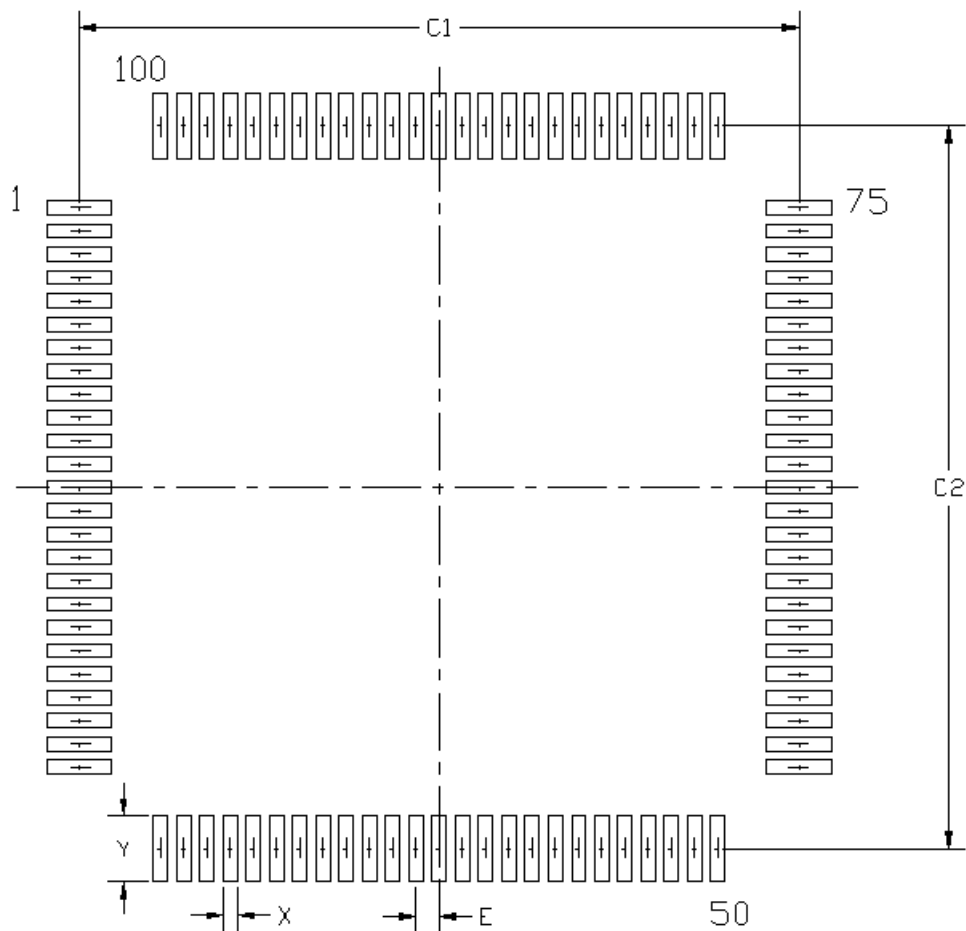


Figure 10.2. TQFP100 PCB Land Pattern Drawing

Table 10.2. TQFP100 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
C1		15.4	
C2		15.4	
E		0.50 BSC	
X		0.30	
Y		1.50	

- Note:**
- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
 - 2. This Land Pattern Design is based on the IPC-7351 guidelines.
 - 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
 - 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
 - 5. The stencil thickness should be 0.125 mm (5 mils).
 - 6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
 - 7. A No-Clean, Type-3 solder paste is recommended.
 - 8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10.3 TQFP100 Package Marking



Figure 10.3. TQFP100 Package Marking

- The package marking consists of:
- P – The part number designation.
 - T – A trace or manufacturing code. The first letter is the device revision.
 - Y – The last 2 digits of the assembly year.
 - W – The 2-digit workweek when the device was assembled.