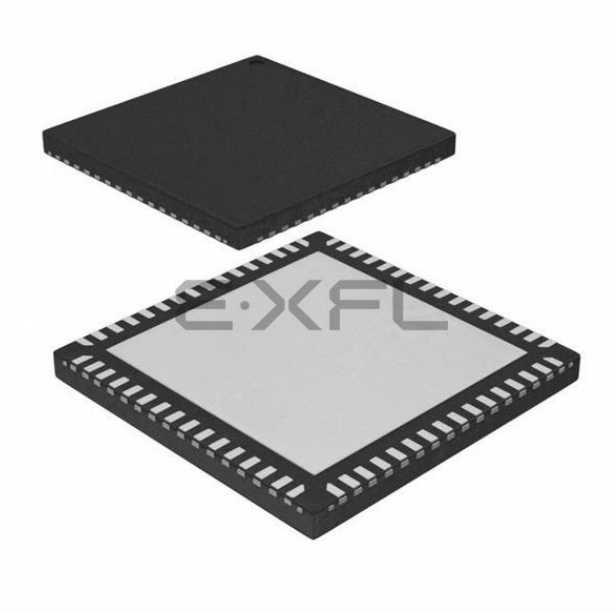

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b820f2048im64-b

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	USB	Ethernet	QSPI	SDIO	LCD	GPIO	Package	Temp Range
EFM32GG11B820F2048GL192-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85°C
EFM32GG11B840F1024GL192-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85°C
EFM32GG11B820F2048GL152-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +85°C
EFM32GG11B820F2048IL152-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +125°C
EFM32GG11B840F1024GL152-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +85°C
EFM32GG11B840F1024IL152-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +125°C
EFM32GG11B820F2048GL120-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +85°C
EFM32GG11B820F2048IL120-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +125°C
EFM32GG11B840F1024GL120-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +85°C
EFM32GG11B840F1024IL120-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +125°C
EFM32GG11B820F2048GQ100-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85°C
EFM32GG11B820F2048IQ100-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +125°C
EFM32GG11B840F1024GQ100-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85°C
EFM32GG11B840F1024IQ100-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +125°C
EFM32GG11B820F2048GQ64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +85°C
EFM32GG11B820F2048GM64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +85°C
EFM32GG11B820F2048IQ64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +125°C
EFM32GG11B820F2048IM64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +125°C
EFM32GG11B840F1024GQ64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +85°C
EFM32GG11B840F1024GM64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +85°C
EFM32GG11B840F1024IQ64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +125°C
EFM32GG11B840F1024IM64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +125°C
EFM32GG11B520F2048GL120-A	2048	512	Yes	No	No	No	No	Yes	95	BGA120	-40 to +85°C
EFM32GG11B510F2048GL120-A	2048	384	Yes	No	No	No	No	Yes	95	BGA120	-40 to +85°C
EFM32GG11B520F2048IL120-A	2048	512	Yes	No	No	No	No	Yes	95	BGA120	-40 to +125°C
EFM32GG11B510F2048IL120-A	2048	384	Yes	No	No	No	No	Yes	95	BGA120	-40 to +125°C
EFM32GG11B520F2048GQ100-A	2048	512	Yes	No	No	No	No	Yes	83	QFP100	-40 to +85°C
EFM32GG11B510F2048GQ100-A	2048	384	Yes	No	No	No	No	Yes	83	QFP100	-40 to +85°C
EFM32GG11B520F2048IQ100-A	2048	512	Yes	No	No	No	No	Yes	83	QFP100	-40 to +125°C
EFM32GG11B510F2048IQ100-A	2048	384	Yes	No	No	No	No	Yes	83	QFP100	-40 to +125°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency limits	f_{HFRCO_BAND}	FREQRANGE = 0, FINETUNINGEN = 0	1	—	10	MHz
		FREQRANGE = 3, FINETUNINGEN = 0	2	—	17	MHz
		FREQRANGE = 6, FINETUNINGEN = 0	4	—	30	MHz
		FREQRANGE = 7, FINETUNINGEN = 0	5	—	34	MHz
		FREQRANGE = 8, FINETUNINGEN = 0	7	—	42	MHz
		FREQRANGE = 10, FINETUNINGEN = 0	12	—	58	MHz
		FREQRANGE = 11, FINETUNINGEN = 0	15	—	68	MHz
		FREQRANGE = 12, FINETUNINGEN = 0	18	—	83	MHz
		FREQRANGE = 13, FINETUNINGEN = 0	24	—	100	MHz
		FREQRANGE = 14, FINETUNINGEN = 0	28	—	119	MHz
		FREQRANGE = 15, FINETUNINGEN = 0	33	—	138	MHz
		FREQRANGE = 16, FINETUNINGEN = 0	43	—	163	MHz

Note:

1. Maximum DPLL lock time ~= 6 x (M+1) x t_{REF}, where t_{REF} is the reference clock period.

4.1.10.6 USB High-Frequency RC Oscillator (USHFRCO)

Table 4.17. USB High-Frequency RC Oscillator (USHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{USHFRCO\_ACC}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
		USB clock recovery enabled, Active connection as device, FINETUNINGEN[1] = 1	-0.25	—	0.25	%
Start-up time	$t_{USHFRCO}$		—	300	—	ns
Current consumption on all supplies	$I_{USHFRCO}$	$f_{USHFRCO}$ = 48 MHz, FINETUNINGEN[1] = 1	—	340	TBD	µA
		$f_{USHFRCO}$ = 50 MHz, FINETUNINGEN[1] = 0	—	342	TBD	µA
		$f_{USHFRCO}$ = 48 MHz, FINETUNINGEN[1] = 0	—	292	TBD	µA
		$f_{USHFRCO}$ = 32 MHz, FINETUNINGEN[1] = 0	—	223	TBD	µA
		$f_{USHFRCO}$ = 16 MHz, FINETUNINGEN[1] = 0	—	132	TBD	µA
Period jitter	$PJ_{USHFRCO}$		—	0.2	—	% RMS

Note:
1. In the CMU_USHFRCOCTRL register.

4.1.10.7 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.18. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		TBD	1	TBD	kHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[1]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[4] = NORMAL	—	—	5	µs
		WARMUPMODE[4] = KEEPIN-STANDBY	—	—	2	µs
		WARMUPMODE[4] = KEEPINSLO-WACC	—	—	1	µs
SNDR at 1Msps and f_{IN} = 10kHz	$SNDR_{ADC}$	Internal reference[7], differential measurement	TBD	67	—	dB
		External reference[6], differential measurement	—	68	—	dB
Spurious-free dynamic range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing co-des	TBD	—	TBD	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	TBD	—	TBD	LSB
Offset error	$V_{ADCOFFSETERR}$		TBD	0	TBD	LSB
Gain error in ADC	$V_{ADCGAIN}$	Using internal reference	—	-0.2	TBD	%
		Using external reference	—	-1	—	%
Temperature sensor slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Note:

1. Derived from ADCCLK.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_BIASPROG register.
4. In ADCn_CNTL register.
5. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
6. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is ± 1.25 V.
7. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is ± 1.25 V. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis (V_{CM} = 1.25 V, BIASPROG[4] = 0x10, FULLBIAS[4] = 1)	$V_{ACMPHYST}$	HYSTSEL[5] = HYST0	TBD	0	TBD	mV
		HYSTSEL[5] = HYST1	TBD	18	TBD	mV
		HYSTSEL[5] = HYST2	TBD	33	TBD	mV
		HYSTSEL[5] = HYST3	TBD	46	TBD	mV
		HYSTSEL[5] = HYST4	TBD	57	TBD	mV
		HYSTSEL[5] = HYST5	TBD	68	TBD	mV
		HYSTSEL[5] = HYST6	TBD	79	TBD	mV
		HYSTSEL[5] = HYST7	TBD	90	TBD	mV
		HYSTSEL[5] = HYST8	TBD	0	TBD	mV
		HYSTSEL[5] = HYST9	TBD	-18	TBD	mV
		HYSTSEL[5] = HYST10	TBD	-33	TBD	mV
		HYSTSEL[5] = HYST11	TBD	-45	TBD	mV
		HYSTSEL[5] = HYST12	TBD	-57	TBD	mV
		HYSTSEL[5] = HYST13	TBD	-67	TBD	mV
		HYSTSEL[5] = HYST14	TBD	-78	TBD	mV
		HYSTSEL[5] = HYST15	TBD	-88	TBD	mV
Comparator delay[3]	$t_{ACMPDELAY}$	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	30	—	µs
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	3.7	—	µs
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	360	—	ns
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[4] =0x10, FULLBIAS[4] = 1	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	infinite	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	100	—	kΩ
		CSRESSEL[6] = 6	—	162	—	kΩ
		CSRESSEL[6] = 7	—	235	—	kΩ

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	µs
Settling time, (output settled within 1% of steady state value),	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	µs
		Step value is changed	—	1	—	µs
Current consumption[2]	I_{IDAC}	EM0 or EM1 Source mode, excluding output current, Across operating temperature range	—	11	TBD	µA
		EM0 or EM1 Sink mode, excluding output current, Across operating temperature range	—	13	TBD	µA
		EM2 or EM3 Source mode, excluding output current, T = 25 °C	—	0.05	—	µA
		EM2 or EM3 Sink mode, excluding output current, T = 25 °C	—	0.07	—	µA
		EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C	—	11	—	µA
		EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C	—	13	—	µA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.11	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.06	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.04	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.03	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.29	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.27	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.12	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.03	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.23.2 I2C Fast-mode (Fm)[1]

Table 4.32. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

EBI Ready/Wait Timing Requirements

Timing applies to both EBI_REn and EBI_WEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.41. EBI Ready/Wait Timing Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge	t_{SU_ARDY}	IOVDD ≥ 1.62 V	55 + (3 * $t_{HFCOR-ECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	36 + (3 * $t_{HFCOR-ECLK}$)	—	—	ns
Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid	t_{H_ARDY}	IOVDD ≥ 1.62 V	-9	—	—	ns

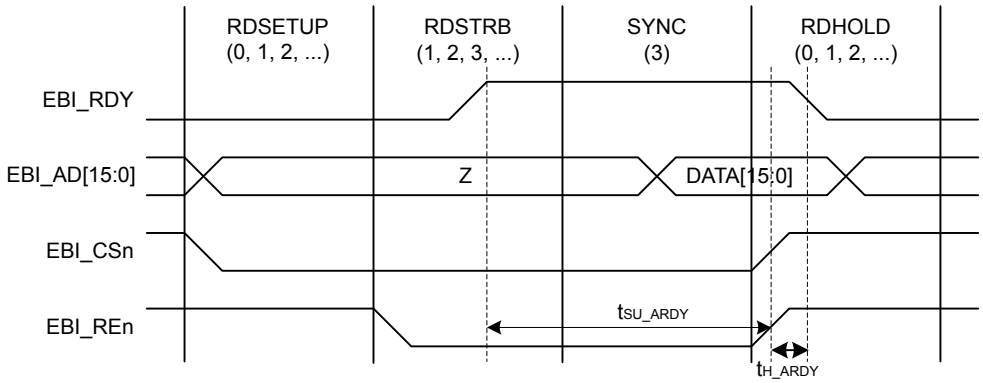


Figure 4.8. EBI Ready/Wait Timing Requirements

SDIO SDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.48. SDIO SDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		0.99	4.68	—	ns
Clock fall time	t_F		0.90	3.64	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}		8	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}		1.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}		0	—	35	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}		0.8	—	—	ns

SDIO MMC SDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.50. SDIO MMC SDR Mode Timing (Location 0, 1.8V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	25	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.96	8.27	—	ns
Clock fall time	t_F		1.67	6.90	—	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:7] change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	t_{OH}		3	—	—	ns

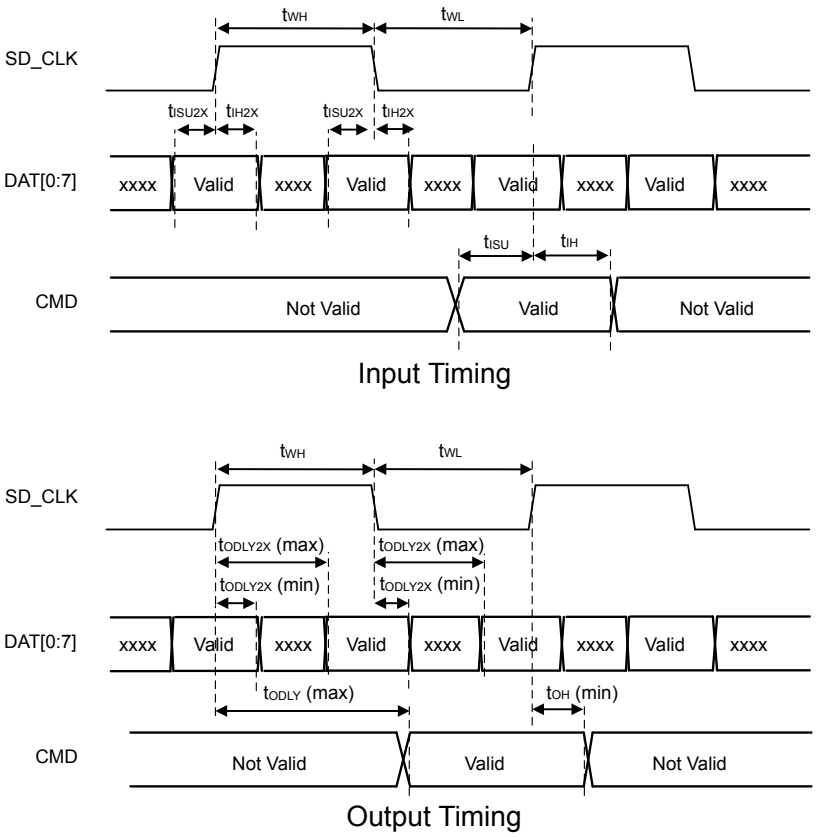


Figure 4.19. SDIO MMC DDR Mode Timing

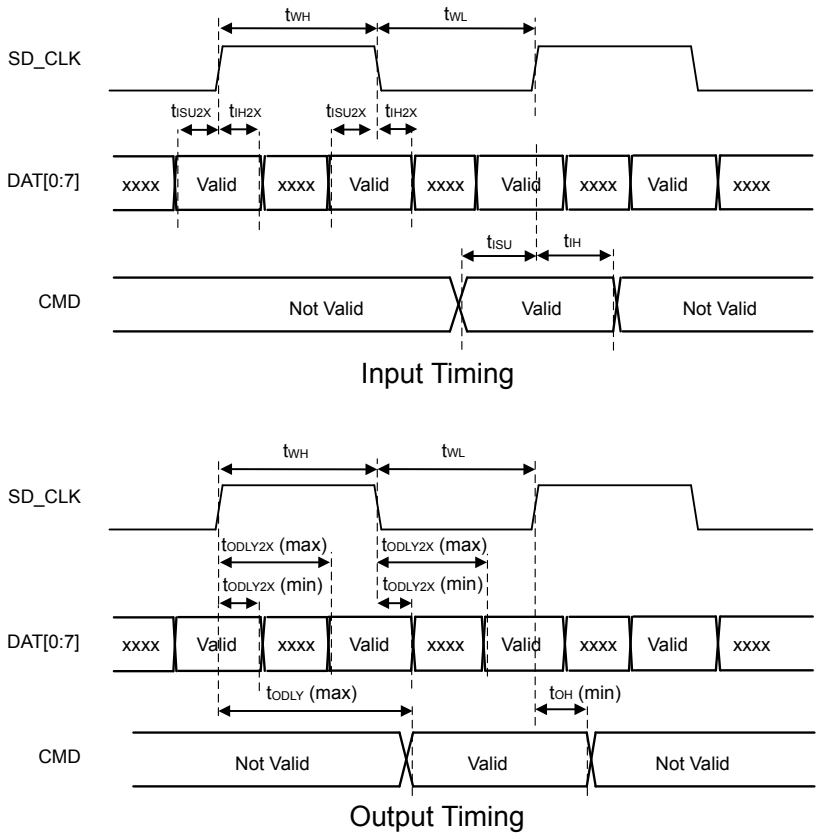


Figure 4.20. SDIO MMC DDR Mode Timing

4.1.28 Quad SPI (QSPI)

4.1.28.1 QSPI SDR Mode

QSPI SDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 23, RX DLL = 48, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.54. QSPI SDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full SCLK period	T		$(1/F_{SCLK})$ * 0.95	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 2.4	ns
Output hold	t_{OH}		T/2 - 32.9	—	—	ns
Input setup	t_{SU}		36.2 - T/2	—	—	ns
Input hold	t_H		T/2 - 3.3	—	—	ns

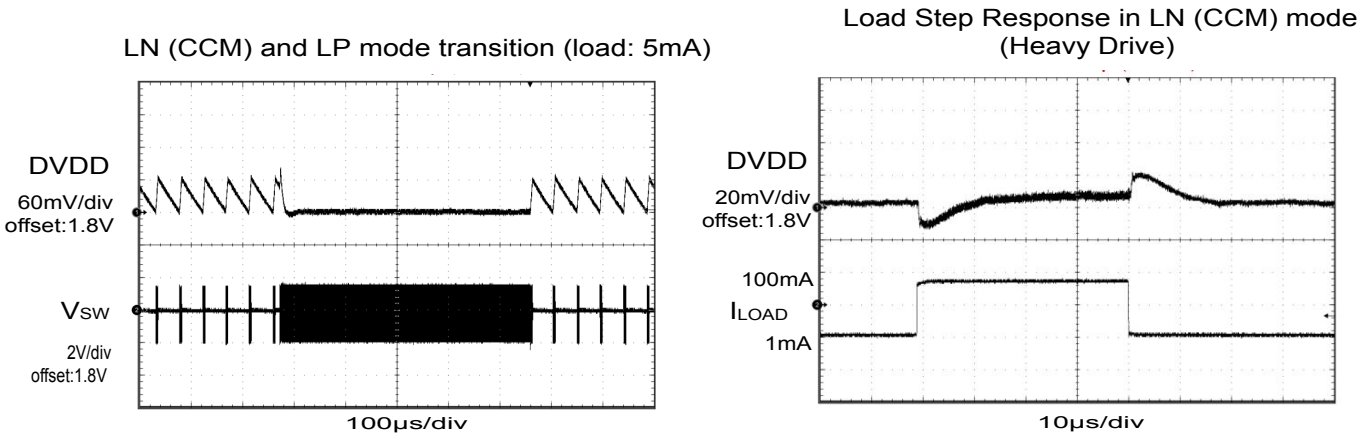


Figure 4.30. DC-DC Converter Transition Waveforms

5.8 EFM32GG11B8xx in QFP100 Device Pinout

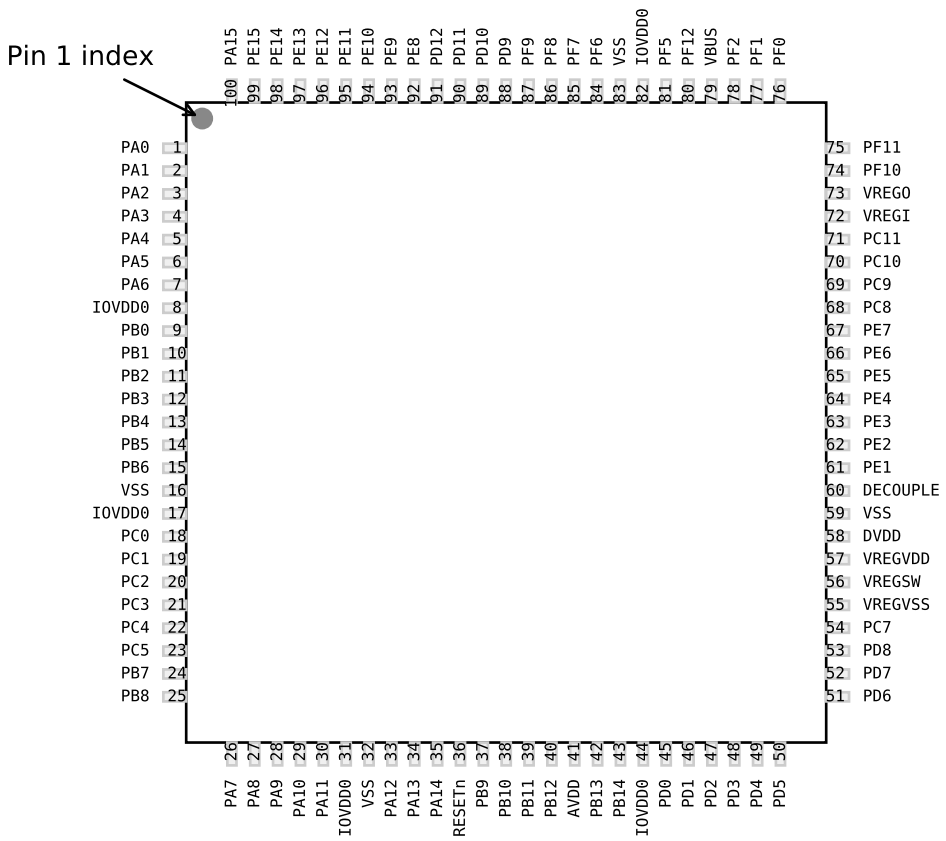


Figure 5.8. EFM32GG11B8xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.8. EFM32GG11B8xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF7	BUSCY BUSDX LCD_SEG25	EBI_BL1 #0 EBI_BL1 #4 EBI_BL1 #5 EBI_DCLK #1	TIM0_CC1 #1 TIM4_CC1 #4	ETH_RMIITXD0 #1 US2_RX #4 QSPI0_CS0 #0 ETH_MIIRXER #2 US1_RX #3 U0_RX #0	PRS_CH23 #2
PF6	BUSDY BUSCX LCD_SEG24	EBI_BL0 #0 EBI_BL0 #4 EBI_BL0 #5 EBI_CSTFT #1	TIM0_CC0 #1 TIM4_CC0 #4 WTIM3_CC2 #5	ETH_RMIITXD1 #1 US2_TX #4 QSPI0_SCLK #0 US1_TX #3 U0_TX #0	PRS_CH22 #2
PI11				US4_RTS #3	
PI8		EBI_A13 #2	TIM1_CC2 #7 TIM4_CC0 #3	US4_CLK #3	
PF5	BUSCY BUSDX LCD_SEG3	EBI_REn #0 EBI_REn #5 EBI_A27 #1	TIM0_CDTI2 #2 TIM1_CC3 #6 TIM4_CC0 #2	US2_CS #5 I2C2_SCL #0 USB_VBUSEN	PRS_CH2 #1 DBG_TDI
PF13	BUSCY BUSDX		TIM1_CC0 #6 TIM4_CC0 #1 TIM5_CC1 #7 WTIM3_CC0 #7	US5_CLK #2 I2C2_SDA #4	
PF3	BUSCY BUSDX LCD_SEG1	EBI_ALE #0	TIM4_CC0 #0 TIM0_CDTI0 #2 TIM1_CC1 #5	CAN1_TX #1 US1_CTS #2 I2C2_SCL #5	CMU_CLK1 #4 PRS_CH0 #1 ETM_TD3 #1
PF2	BUSDY BUSCX LCD_SEG0	EBI_ARDY #0 EBI_A26 #1	TIM0_CC2 #4 TIM1_CC0 #5 TIM2_CC0 #3	US2_CLK #5 CAN0_TX #1 US1_TX #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO DBG_SWO #0 GPIO_EM4WU4
PF1	BUSCY BUSDX	EBI_A25 #1	TIM0_CC1 #4 WTIM0_CC2 #4 LE-TIM0_OUT1 #2	US2_RX #5 CAN1_RX #1 US1_CS #2 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PA1	BUSAY BUSBX LCD_SEG14	EBI_AD10 #0 EBI_DCLK #3	TIM0_CC0 #7 TIM0_CC1 #0 TIM3_CC1 #4 PCNT0_S1IN #4	ETH_RMIIRXD1 #0 ETH_MIITXD3 #0 SDIO_DAT1 #1 US3_RX #0 QSPI0_CS1 #1 I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
PD12	LCD_SEG31	EBI_CS3 #0	TIM4_CC1 #6	ETH_RMIIRXER #1 SDIO_DAT4 #0 QSPI0_DQ3 #0 ETH_MIIRXCLK #2 US4_CS #1	
PD14		EBI_NANDWEn #1	TIM2_CDTI1 #1 TIM3_CC2 #6 WTIM0_CC2 #1	ETH_MDC #1 CAN0_RX #5 US4_RTS #1 US5_CS #1 I2C0_SDA #3	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.
LES_CH0	0: PC0		LESENSE channel 0.
LES_CH1	0: PC1		LESENSE channel 1.
LES_CH2	0: PC2		LESENSE channel 2.
LES_CH3	0: PC3		LESENSE channel 3.
LES_CH4	0: PC4		LESENSE channel 4.
LES_CH5	0: PC5		LESENSE channel 5.
LES_CH6	0: PC6		LESENSE channel 6.
LES_CH7	0: PC7		LESENSE channel 7.
LES_CH8	0: PC8		LESENSE channel 8.
LES_CH9	0: PC9		LESENSE channel 9.
LES_CH10	0: PC10		LESENSE channel 10.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PRS_CH20	0: PB4 1: PC12 2: PE2		Peripheral Reflex System PRS, channel 20.
PRS_CH21	0: PB5 1: PC13 2: PB11		Peripheral Reflex System PRS, channel 21.
PRS_CH22	0: PB7 1: PE0 2: PF6		Peripheral Reflex System PRS, channel 22.
PRS_CH23	0: PB8 1: PE1 2: PF7		Peripheral Reflex System PRS, channel 23.
QSPI0_CS0	0: PF7 1: PA0 2: PG9		Quad SPI 0 Chip Select 0.
QSPI0_CS1	0: PF8 1: PA1 2: PG10		Quad SPI 0 Chip Select 1.
QSPI0_DQ0	0: PD9 1: PA2 2: PG1		Quad SPI 0 Data 0.
QSPI0_DQ1	0: PD10 1: PA3 2: PG2		Quad SPI 0 Data 1.
QSPI0_DQ2	0: PD11 1: PA4 2: PG3		Quad SPI 0 Data 2.
QSPI0_DQ3	0: PD12 1: PA5 2: PG4		Quad SPI 0 Data 3.
QSPI0_DQ4	0: PE8 1: PB3 2: PG5		Quad SPI 0 Data 4.
QSPI0_DQ5	0: PE9 1: PB4 2: PG6		Quad SPI 0 Data 5.
QSPI0_DQ6	0: PE10 1: PB5 2: PG7		Quad SPI 0 Data 6.

8. BGA120 Package Specifications

8.1 BGA120 Package Dimensions

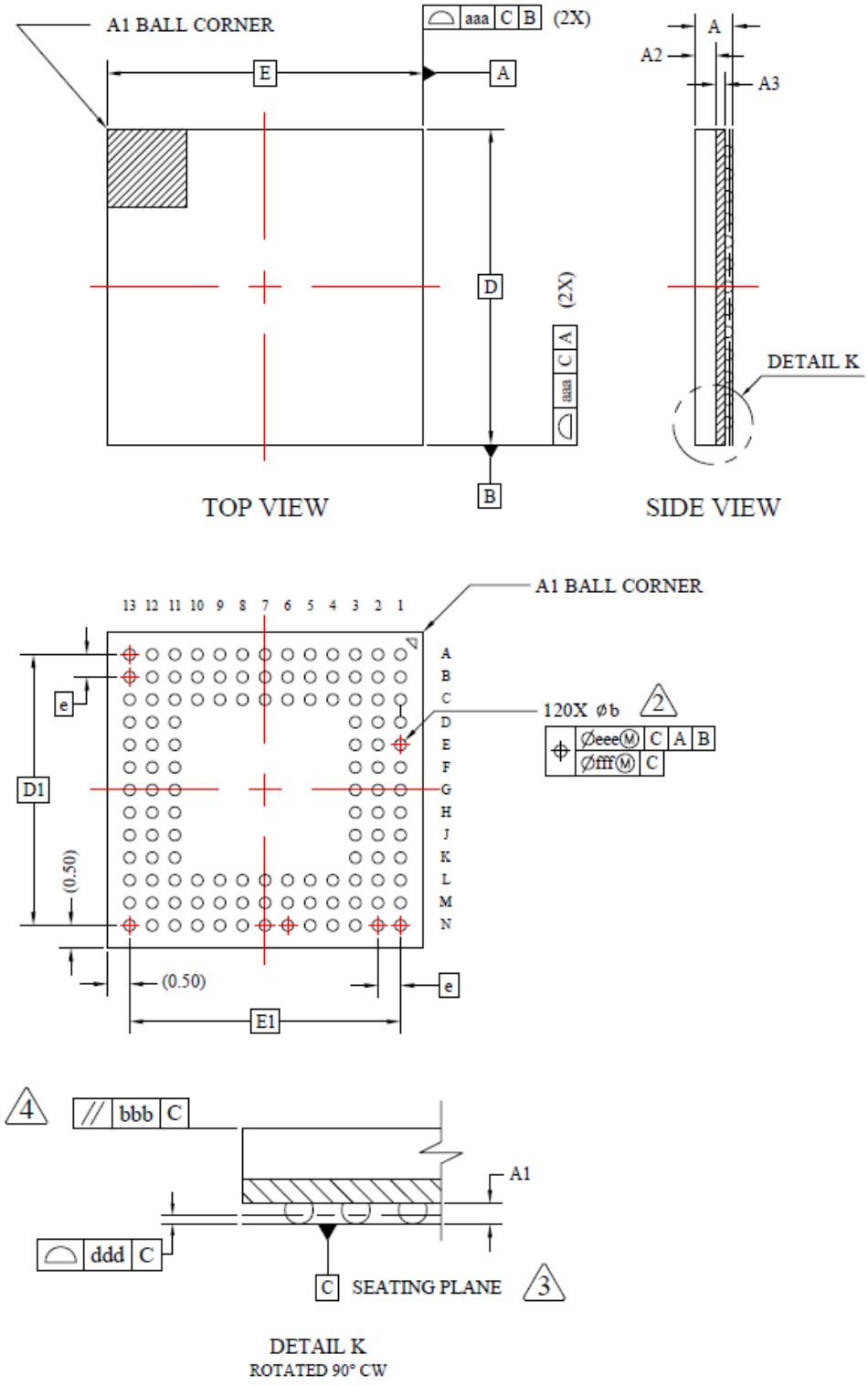
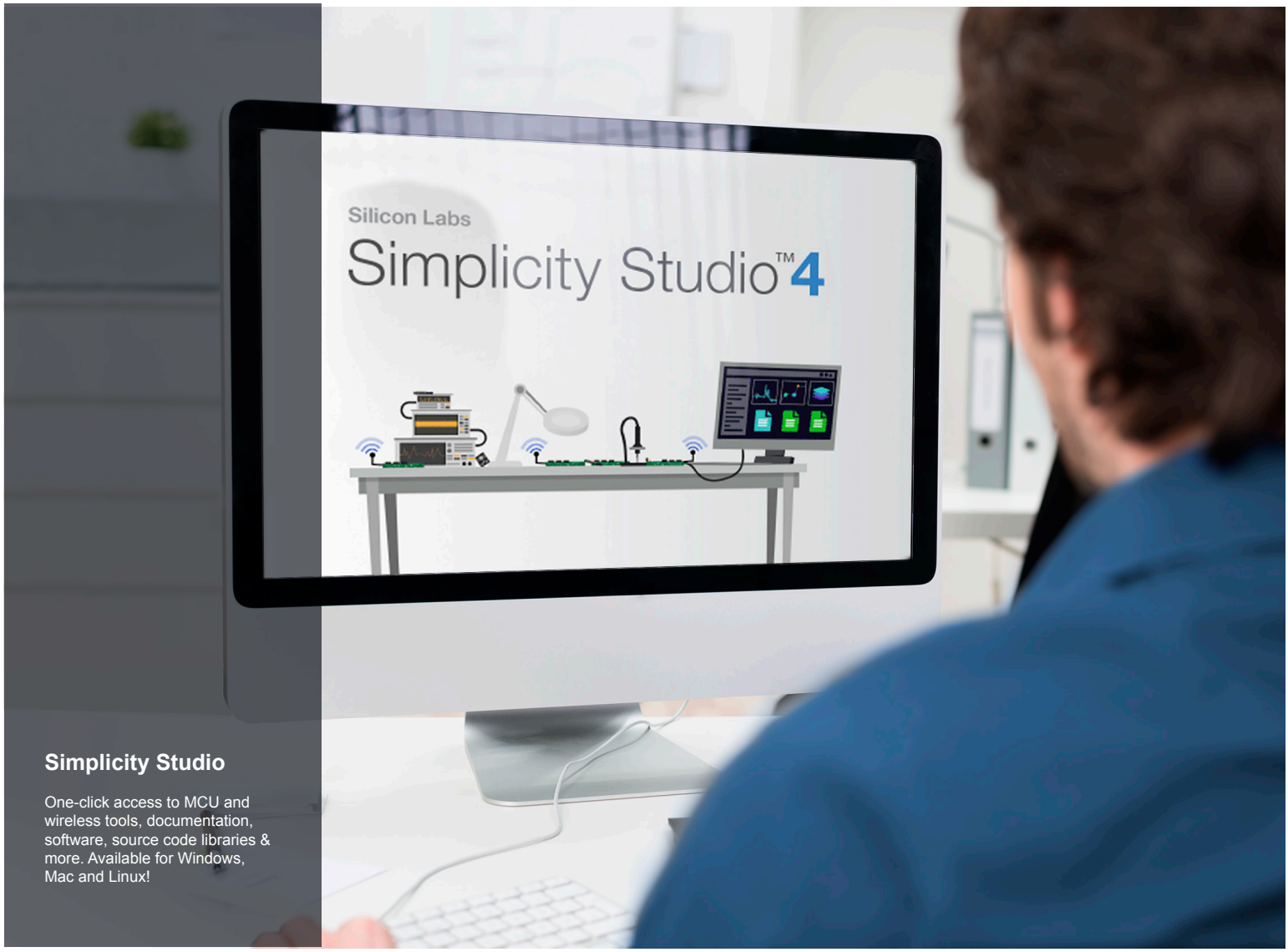


Figure 8.1. BGA120 Package Drawing



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