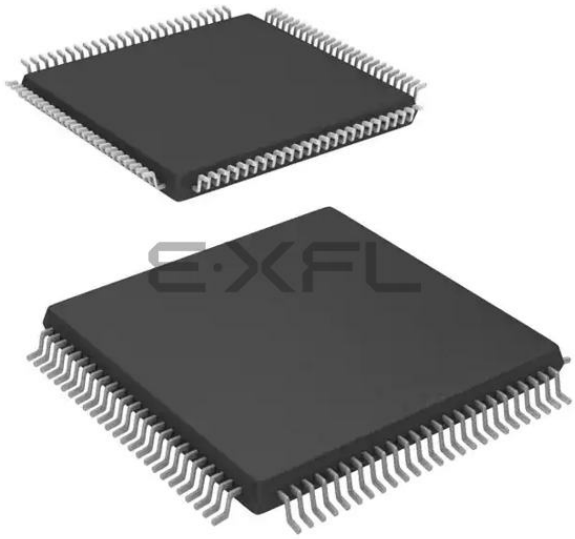

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b820f2048iq100-a

3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

4.1.5 5V Regulator

V_{VREGI} = 5 V, V_{VREGO} = 3.3 V, C_{VREGI} = 10 µF, C_{VREGO} = 4.7 µF, unless otherwise specified.

Table 4.5. 5V Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VREGI or VBUS input voltage range	V_{VREGI}	Regulating output	2.7	—	5.5	V
		Bypass mode enabled	2.7	—	3.8	V
VREGO output voltage	V_{VREGO}	Regulating output, 3.3 V setting	3.1	3.3	3.5	V
		EM4S open-loop output, I_{OUT} < 100 µA	1.8	—	3.8	V
Voltage output step size	V_{VREGO_SS}		—	0.1	—	V
Resistance in Bypass Mode	R_{BYP}	Bypass mode enabled	—	1.2	TBD	Ω
Output current	I_{OUT}	EM0 or EM1, V_{VREGI} > V_{VREGO} + 0.6 V	—	—	200	mA
		EM0 or EM1, V_{VREGI} > V_{VREGO} + 0.3 V	—	—	100	mA
		EM2, EM3, or EM4H, V_{VREGI} > V_{VREGO} + 0.6 V	—	—	2	mA
		EM2, EM3, or EM4H, V_{VREGI} > V_{VREGO} + 0.3 V	—	—	0.5	mA
		EM4S	—	—	20	µA
Load regulation	LR_{VREGO}	EM0 or EM1	—	0.10	—	mV/mA
		EM2, EM3, or EM4H	—	2.5	—	mV/mA
DC power supply rejection	PSR_{DC}		—	40	—	dB
VREGI or VBUS bypass capacitance	C_{VREGI}		—	10	—	µF
VREGO bypass capacitance	C_{VREGO}		1	4.7	10	µF
Supply current consumption	I_{VREGI}	EM0 or EM1, No load	—	29	—	µA
		EM2, EM3, or EM4H, No load	—	270	—	nA
		EM4S, No load	—	70	—	nA
VREGI and VBUS detection high threshold	V_{DET_H}		TBD	1.18	—	V
VREGI and VBUS detection low threshold	V_{DET_L}		—	1.12	TBD	V
Current monitor transfer ratio	$IMON_{XF}$	Translation of current through VREGO path to voltage at ADC input	—	0.35	—	mA/mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFRCO	—	3.4	—	µA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.94	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.56	—	µA
		128 byte RAM retention, no RTCC	—	0.56	—	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.1	—	µA
Current consumption of peripheral power domain 1, with voltage scaling enabled	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[1]	—	0.68	—	µA
Current consumption of peripheral power domain 2, with voltage scaling enabled	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[1]	—	0.28	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[1]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[4] = NORMAL	—	—	5	µs
		WARMUPMODE[4] = KEEPIN-STANDBY	—	—	2	µs
		WARMUPMODE[4] = KEEPINSLO-WACC	—	—	1	µs
SNDR at 1Msps and f_{IN} = 10kHz	$SNDR_{ADC}$	Internal reference[7], differential measurement	TBD	67	—	dB
		External reference[6], differential measurement	—	68	—	dB
Spurious-free dynamic range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing co-des	TBD	—	TBD	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	TBD	—	TBD	LSB
Offset error	$V_{ADCOFFSETERR}$		TBD	0	TBD	LSB
Gain error in ADC	$V_{ADCGAIN}$	Using internal reference	—	-0.2	TBD	%
		Using external reference	—	-1	—	%
Temperature sensor slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Note:

1. Derived from ADCCLK.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_BIASPROG register.
4. In ADCn_CNTL register.
5. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
6. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is ± 1.25 V.
7. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is ± 1.25 V. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.

4.1.19 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAINOUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes[8] [1].

Table 4.27. Operational Amplifier (OPAMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply voltage (from AVDD)	V_{OPA}	HCMDIS = 0, Rail-to-rail input range	2	—	3.8	V
		HCMDIS = 1	1.62	—	3.8	V
Input voltage	V_{IN}	HCMDIS = 0, Rail-to-rail input range	V_{VSS}	—	V_{OPA}	V
		HCMDIS = 1	V_{VSS}	—	V_{OPA}-1.2	V
Input impedance	R_{IN}		100	—	—	MΩ
Output voltage	V_{OUT}		V_{VSS}	—	V_{OPA}	V
Load capacitance[2]	C_{LOAD}	OUTSCALE = 0	—	—	75	pF
		OUTSCALE = 1	—	—	37.5	pF
Output impedance	R_{OUT}	DRIVESTRENGTH = 2 or 3, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -8 mA < I_{OUT} < 8 mA, Buffer connection, Full supply range	—	0.25	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -400 µA < I_{OUT} < 400 µA, Buffer connection, Full supply range	—	0.6	—	Ω
		DRIVESTRENGTH = 2 or 3, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -2 mA < I_{OUT} < 2 mA, Buffer connection, Full supply range	—	0.4	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -100 µA < I_{OUT} < 100 µA, Buffer connection, Full supply range	—	1	—	Ω
Internal closed-loop gain	G_{CL}	Buffer connection	TBD	1	TBD	-
		3x Gain connection	TBD	2.99	TBD	-
		16x Gain connection	TBD	15.7	TBD	-
Active current[4]	I_{OPA}	DRIVESTRENGTH = 3, OUTSCALE = 0	—	580	—	µA
		DRIVESTRENGTH = 2, OUTSCALE = 0	—	176	—	µA
		DRIVESTRENGTH = 1, OUTSCALE = 0	—	13	—	µA
		DRIVESTRENGTH = 0, OUTSCALE = 0	—	4.7	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew rate[5]	SR	DRIVESTRENGTH = 3, INCBW=1[3]	—	4.7	—	V/µs
		DRIVESTRENGTH = 3, INCBW=0	—	1.5	—	V/µs
		DRIVESTRENGTH = 2, INCBW=1[3]	—	1.27	—	V/µs
		DRIVESTRENGTH = 2, INCBW=0	—	0.42	—	V/µs
		DRIVESTRENGTH = 1, INCBW=1[3]	—	0.17	—	V/µs
		DRIVESTRENGTH = 1, INCBW=0	—	0.058	—	V/µs
		DRIVESTRENGTH = 0, INCBW=1[3]	—	0.044	—	V/µs
		DRIVESTRENGTH = 0, INCBW=0	—	0.015	—	V/µs
Startup time[6]	T_{START}	DRIVESTRENGTH = 2	—	—	12	µs
Input offset voltage	V_{OSI}	DRIVESTRENGTH = 2 or 3, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	TBD	—	TBD	mV
DC power supply rejection ratio[9]	$PSRR_{DC}$	Input referred	—	70	—	dB
DC common-mode rejection ratio[9]	$CMRR_{DC}$	Input referred	—	70	—	dB
Total harmonic distortion	THD_{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
MISO hold time [1] [3]	t_{H_MI}	USART2, location 4, IOVDD = 1.8 V	-11.6	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	-11.6	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	-9.1	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	-9.1	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	-8	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	-8	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

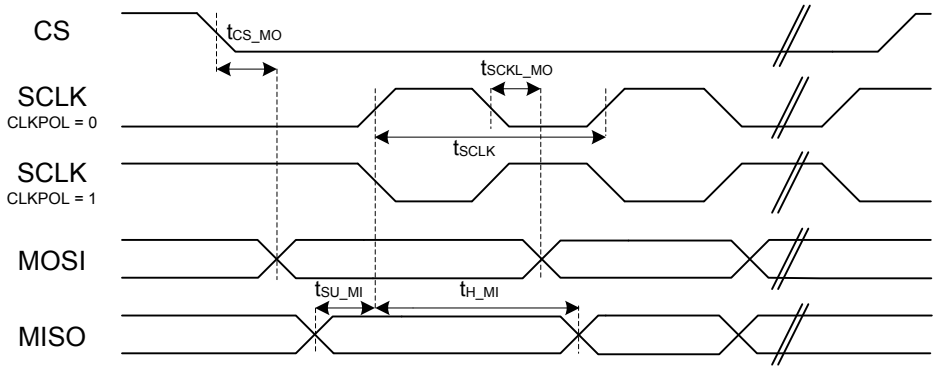

Figure 4.1. SPI Master Timing Diagram

SDIO MMC DDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Table 4.53. SDIO MMC DDR Mode Timing (Location 0, 3V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.13	2.37	—	ns
Clock fall time	t_F		1.01	2.02	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		3	—	—	ns
Input setup time, DAT[0:7] valid to SD_CLK	t_{ISU2X}		5.3	—	—	ns
Input hold time, SD_CLK to DAT[0:7] change	t_{IH2X}		2.5	—	—	ns
Output delay time, SD_CLK to DAT[0:7] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:7] change	t_{OH2X}		3	—	—	ns

QSPI SDR Mode Timing (Locations 1, 2)

Timing is specified with voltage scaling disabled, PHY-mode, route locations other than 0, TX DLL = 34, RX DLL = 59, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.55. QSPI SDR Mode Timing (Locations 1, 2)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full SCLK period	T		$(1/F_{SCLK})$ * 0.95	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 2.1	ns
Output hold	t_{OH}		T/2 - 42.3	—	—	ns
Input setup	t_{SU}		48.2 - T/2	—	—	ns
Input hold	t_H		T/2 - 5.1	—	—	ns

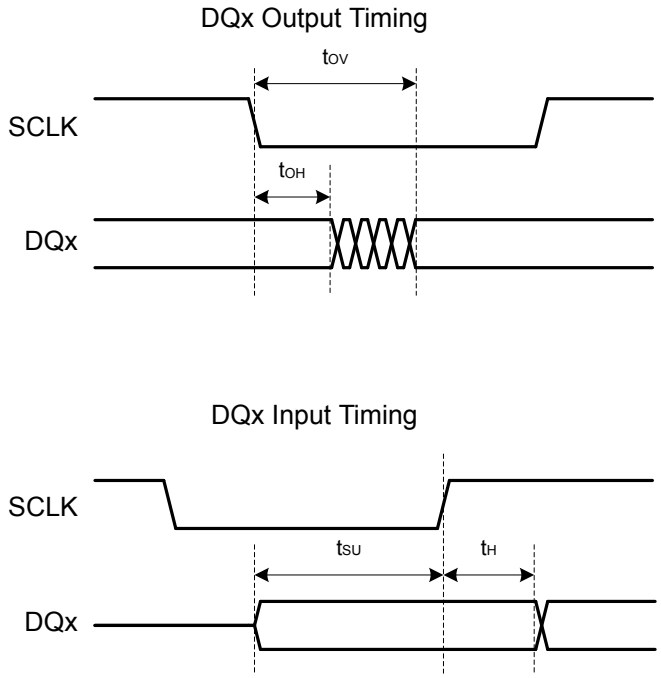

Figure 4.21. QSPI SDR Timing Diagrams

QSPI SDR Flash Timing Example

This example uses timing values for location 0 (SDR mode) to demonstrate the calculation of allowable flash timing using the QSPI in SDR mode.

- Using a configured SCLK frequency (F_{SCLK}) of 19 MHz:
- The resulting minimum period, T(min) = $(1/F_{SCLK})$ * 0.95 = 50.0 ns.
- Flash will see a minimum setup time of T/2 – t_{OV} = T/2 – (T/2 – 2.4) = 2.4 ns.
- Flash will see a minimum hold time of T/2 + t_{OH} = T/2 + (T/2 – 32.9) = T – 32.9 = 50.0 – 32.9 = 17.1 ns.
- Flash can have a maximum output valid time of T/2 – t_{SU} = T/2 – (36.2 – T/2) = T – 36.2 = 50.0 – 36.2 = 13.8 ns.
- Flash can have a minimum output hold time of t_H – T/2 = (T/2 – 3.3) – T/2 = - 3.3 ns.

4.1.28.2 QSPI DDR Mode

QSPI DDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 35, RX DLL = 70, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.56. QSPI DDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Half SCLK period	T/2	HFXO	$(1/F_{SCLK})$ * 0.4 - 0.4	—	—	ns
		HFRCO, AUXHFRCO, USHFRCO	$(1/F_{SCLK})$ * 0.44	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 5.0	ns
Output hold	t_{OH}		T/2 - 39.4	—	—	ns
Input setup	t_{SU}		33.1	—	—	ns
Input hold	t_H		-0.9	—	—	ns

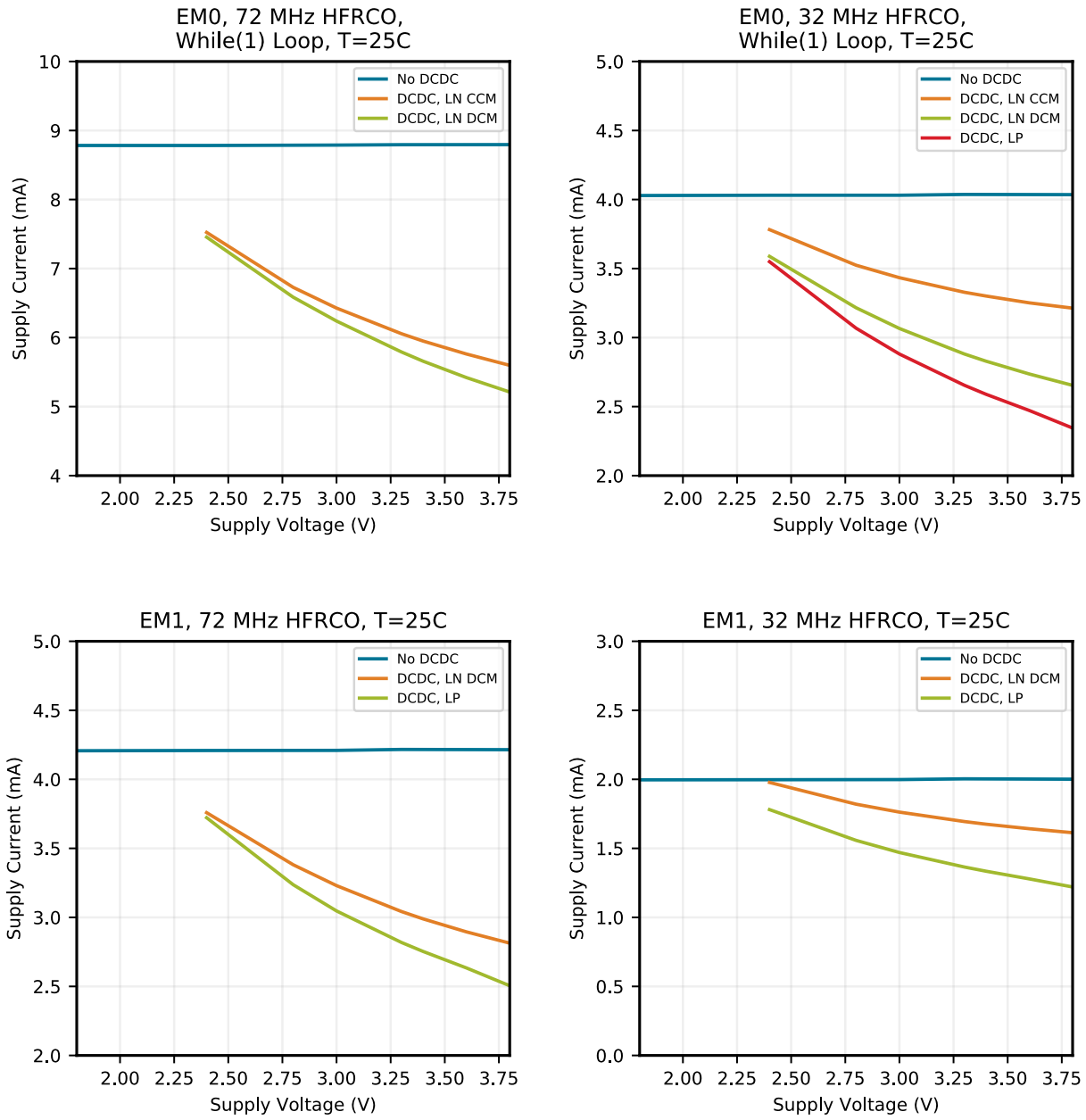

Figure 4.27. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PE6	BUSDY BUSCX LCD_COM2	EBI_A13 #0 EBI_A18 #1 EBI_A24 #3	TIM3_CC1 #3 TIM5_CC2 #0 TIM6_CDTI2 #2 WTIM0_CC2 #0 WTIM1_CC3 #4	US0_RX #1 US3_TX #1	PRS_CH6 #2
PE7	BUSCY BUSDX LCD_COM3	EBI_A14 #0 EBI_A19 #1 EBI_A25 #3	TIM3_CC2 #3 TIM5_CC0 #1 WTIM1_CC0 #5	US0_TX #1 US3_RX #1	PRS_CH7 #2
PG11		EBI_AD11 #2	TIM6_CDTI2 #1 WTIM0_CDTI0 #3	ETH_MIIRXD0 #1 CAN1_TX #6 US3_RTS #5 QSPI0_DQS #2	ETM_TD3 #5
PG10		EBI_AD10 #2	TIM2_CC2 #6 TIM6_CDTI1 #1 WTIM0_CC2 #3	ETH_MIIRXD1 #1 CAN1_RX #6 US3_CTS #3 QSPI0_CS1 #2	
PG9		EBI_AD09 #2	TIM2_CC1 #6 TIM6_CDTI0 #1 WTIM0_CC1 #3	ETH_MIIRXD2 #1 CAN0_TX #4 US3_CTS #5 QSPI0_CS0 #2	
PE3	BU_STAT	EBI_A10 #0 EBI_A15 #1	TIM3_CC0 #2 WTIM1_CC0 #4	US0_CTS #1 U0_RTS #1 U1_RX #3	ACMP1_O #1
PE4	BUSDY BUSCX LCD_COM0	EBI_A11 #0 EBI_A16 #1 EBI_A22 #3	TIM3_CC1 #2 TIM5_CC0 #0 TIM6_CDTI0 #2 WTIM0_CC0 #0 WTIM1_CC1 #4	US0_CS #1 US1_CS #5 US3_CS #1 U0_RX #6 U1_CTS #3 I2C0_SDA #7	PRS_CH16 #2
PG14		EBI_AD14 #2	TIM6_CC2 #2 WTIM2_CC0 #4 PCNT1_S0IN #7	ETH_MIICRS #1 US0_CLK #6	ETM_TD0 #5
PG13		EBI_AD13 #2	TIM6_CC1 #2 WTIM0_CDTI2 #3 WTIM2_CC2 #3	ETH_MIIRXER #1 US0_RX #6	ETM_TD1 #5
PG12		EBI_AD12 #2	TIM6_CC0 #2 WTIM0_CDTI1 #3 WTIM2_CC1 #3	ETH_MIIRXDV #1 US0_TX #6	ETM_TD2 #5
PE1	BUSCY BUSDX	EBI_A01 #2 EBI_A08 #0	TIM3_CC1 #1 WTIM1_CC2 #3 PCNT0_S1IN #1	CAN0_TX #6 U0_RX #1 I2C1_SCL #2	CMU_CLKI0 #4 PRS_CH23 #1 ACMP2_O #2
PE2	BU_VOUT	EBI_A09 #0 EBI_A14 #1	TIM3_CC2 #1 WTIM1_CC3 #3	US0_RTS #1 U0_CTS #1 U1_TX #3	PRS_CH20 #2 ACMP0_O #1
PG15		EBI_AD15 #2	WTIM2_CC1 #4 PCNT1_S1IN #7	ETH_MIICOL #1 US0_CS #6	ETM_TCLK #5
PB15	BUSAY BUSBX	EBI_CS3 #1 EBI_ARDY #2	TIM3_CC1 #7	ETH_TSUTMRTOG #1 SDIO_WP #2 US2_RTS #1 US5_RTS #1	PRS_CH17 #1 ETM_TD2 #1

5.21 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 5.20 GPIO Functionality Table for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.21. Alternate Functionality Overview

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ACMP0_O	0: PE13 1: PE2 2: PD6 3: PB11	4: PA6 5: PB0 6: PB2 7: PB3	Analog comparator ACMP0, digital output.
ACMP1_O	0: PF2 1: PE3 2: PD7 3: PA12	4: PA14 5: PB9 6: PB10 7: PA5	Analog comparator ACMP1, digital output.
ACMP2_O	0: PD8 1: PE0 2: PE1 3: PI0	4: PI1 5: PI2	Analog comparator ACMP2, digital output.
ACMP3_O	0: PF0 1: PC15 2: PC14 3: PC13	4: PI4 5: PI5	Analog comparator ACMP3, digital output.
ADC0_EXTN	0: PD7		Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PD6		Analog to digital converter ADC0 external reference input positive pin.
ADC1_EXTN	0: PD7		Analog to digital converter ADC1 external reference input negative pin.
ADC1_EXTP	0: PD6		Analog to digital converter ADC1 external reference input positive pin.
BOOT_RX	0: PF1		Bootloader RX.
BOOT_TX	0: PF0		Bootloader TX.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A10	0: PE3 1: PD6 2: PC10 3: PB10		External Bus Interface (EBI) address output pin 10.
EBI_A11	0: PE4 1: PD7 2: PI6 3: PB11		External Bus Interface (EBI) address output pin 11.
EBI_A12	0: PE5 1: PD8 2: PI7 3: PB12		External Bus Interface (EBI) address output pin 12.
EBI_A13	0: PE6 1: PC7 2: PI8 3: PD0		External Bus Interface (EBI) address output pin 13.
EBI_A14	0: PE7 1: PE2 2: PI9 3: PD1		External Bus Interface (EBI) address output pin 14.
EBI_A15	0: PC8 1: PE3 2: PI10 3: PD2		External Bus Interface (EBI) address output pin 15.
EBI_A16	0: PB0 1: PE4 2: PH4 3: PD3		External Bus Interface (EBI) address output pin 16.
EBI_A17	0: PB1 1: PE5 2: PH5 3: PD4		External Bus Interface (EBI) address output pin 17.
EBI_A18	0: PB2 1: PE6 2: PH6 3: PD5		External Bus Interface (EBI) address output pin 18.
EBI_A19	0: PB3 1: PE7 2: PH7 3: PD6		External Bus Interface (EBI) address output pin 19.
EBI_A20	0: PB4 1: PC8 2: PH8 3: PD7		External Bus Interface (EBI) address output pin 20.
EBI_A21	0: PB5 1: PC9 2: PH9 3: PC7		External Bus Interface (EBI) address output pin 21.
EBI_A22	0: PB6 1: PC10 2: PH10 3: PE4		External Bus Interface (EBI) address output pin 22.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
GPIO_EM4WU7	0: PB11		Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PF8		Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PE10		Pin can be used to wake the system up from EM4
HFXTAL_N	0: PB14		High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	0: PB13		High Frequency Crystal positive pin.
I2C0_SCL	0: PA1 1: PD7 2: PC7 3: PD15	4: PC1 5: PF1 6: PE13 7: PE5	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PD6 2: PC6 3: PD14	4: PC0 5: PF0 6: PE12 7: PE4	I2C0 Serial Data input / output.
I2C1_SCL	0: PC5 1: PB12 2: PE1 3: PD5	4: PF2 5: PH12 6: PH14 7: PI3	I2C1 Serial Clock Line input / output.
I2C1_SDA	0: PC4 1: PB11 2: PE0 3: PD4	4: PC11 5: PH11 6: PH13 7: PI2	I2C1 Serial Data input / output.
I2C2_SCL	0: PF5 1: PC15 2: PF11 3: PF12	4: PF14 5: PF3 6: PC13 7: PI5	I2C2 Serial Clock Line input / output.
I2C2_SDA	0: PE8 1: PC14 2: PF10 3: PF4	4: PF13 5: PF15 6: PC12 7: PI4	I2C2 Serial Data input / output.
IDAC0_OUT	0: PB11		IDAC0 output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM0_CC2	0: PE6 1: PD14 2: PG4 3: PG10	4: PF1 5: PB2 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0	0: PE10 1: PD15 2: PA12 3: PG11	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1	0: PE11 1: PG0 2: PA13 3: PG12	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	0: PE12 1: PG1 2: PA14 3: PG13	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	4: PE3 5: PE7 6: PH8 7: PH12	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14 1: PD3 2: PD7 3: PE0	4: PE4 5: PI0 6: PH9 7: PH13	Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	0: PD0 1: PD4 2: PD8 3: PE1	4: PE5 5: PI1 6: PH10 7: PH14	Wide timer 1 Capture Compare input / output channel 2.
WTIM1_CC3	0: PD1 1: PD5 2: PC6 3: PE2	4: PE6 5: PI2 6: PH11 7: PH15	Wide timer 1 Capture Compare input / output channel 3.
WTIM2_CC0	0: PA9 1: PA12 2: PB9 3: PB12	4: PG14 5: PD3 6: PH4 7: PH7	Wide timer 2 Capture Compare input / output channel 0.
WTIM2_CC1	0: PA10 1: PA13 2: PB10 3: PG12	4: PG15 5: PD4 6: PH5 7: PH8	Wide timer 2 Capture Compare input / output channel 1.
WTIM2_CC2	0: PA11 1: PA14 2: PB11 3: PG13	4: PH0 5: PD5 6: PH6 7: PH9	Wide timer 2 Capture Compare input / output channel 2.
WTIM3_CC0	0: PD9 1: PC8 2: PC11 3: PC14	4: PI3 5: PI6 6: PB6 7: PF13	Wide timer 3 Capture Compare input / output channel 0.
WTIM3_CC1	0: PD10 1: PC9 2: PC12 3: PF10	4: PI4 5: PI7 6: PF4 7: PF14	Wide timer 3 Capture Compare input / output channel 1.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM3_CC2	0: PD11 1: PC10 2: PC13 3: PF11	4: PI5 5: PF6 6: PF12 7: PF15	Wide timer 3 Capture Compare input / output channel 2.

Certain alternate function locations may have non-interference priority. These locations will take precedence over any other functions selected on that pin (i.e. another alternate function enabled to the same pin inadvertently).

Some alternate functions may also have high speed priority on certain locations. These locations ensure the fastest possible paths to the pins for timing-critical signals.

The following table lists the alternate functions and locations with special priority.

Table 5.22. Alternate Functionality Priority

Alternate Functionality	Location	Priority
CMU_CLK2	1: PA3 5: PD10	High Speed High Speed
CMU_CLKI0	1: PA3 5: PD10	High Speed High Speed
ETH_RMIICRSDV	0: PA4 1: PD11	High Speed High Speed
ETH_RMIIREFCLK	0: PA3 1: PD10	High Speed High Speed
ETH_RMIIRXD0	0: PA2 1: PD9	High Speed High Speed
ETH_RMIIRXD1	0: PA1 1: PF9	High Speed High Speed
ETH_RMIIRXER	0: PA5 1: PD12	High Speed High Speed
ETH_RMIITXD0	0: PE15 1: PF7	High Speed High Speed
ETH_RMIITXD1	0: PE14 1: PF6	High Speed High Speed
ETH_RMIITXEN	0: PA0 1: PF8	High Speed High Speed
QSPI0_CS0	0: PF7	High Speed
QSPI0_CS1	0: PF8	High Speed
QSPI0_DQ0	0: PD9	High Speed
QSPI0_DQ1	0: PD10	High Speed
QSPI0_DQ2	0: PD11	High Speed
QSPI0_DQ3	0: PD12	High Speed
QSPI0_DQ4	0: PE8	High Speed
QSPI0_DQ5	0: PE9	High Speed
QSPI0_DQ6	0: PE10	High Speed
QSPI0_DQ7	0: PE11	High Speed

Table 7.2. BGA152 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.20	
C1		6.50	
C2		6.50	
E1		0.5	
E2		0.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Table 9.1. BGA112 Package Dimensions

Dimension	Min	Typ	Max
A	-	-	1.30
A1	0.55	0.60	0.65
A2		0.21 BSC	
A3	0.30	0.35	0.40
d	0.43	0.48	0.53
D		10.00 BSC	
D1		8.00 BSC	
E		10.00 BSC	
E1		8.00 BSC	
e1		0.80 BSC	
e2		0.80 BSC	
L1		1.00 REF	
L2		1.00 REF	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.