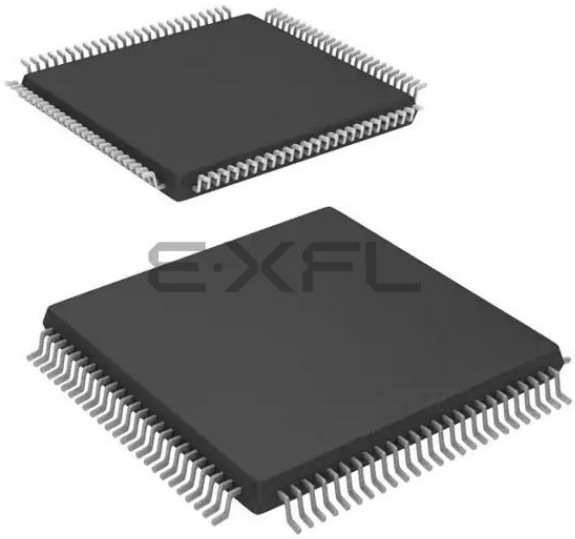

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 80 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.8V |
| Data Converters | A/D 16x12b SAR; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b820f2048iq100-b |

### 3.2.4 EM2 and EM3 Power Domains

The EFM32GG11 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 13. If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

**Table 3.1. EM2 and EM3 Peripheral Power Subdomains**

| Peripheral Power Domain 1 | Peripheral Power Domain 2 |
|---|---|
| ACMP0 | ACMP1 |
| PCNT0 | PCNT1 |
| ADC0 | PCNT2 |
| LETIMER0 | CSEN |
| LESENSE | VDAC0 |
| APORT | LEUART0 |
| - | LEUART1 |
| - | LETIMER1 |
| - | I2C0 |
| - | I2C1 |
| - | I2C2 |
| - | IDAC |
| - | ADC1 |
| - | ACMP2 |
| - | ACMP3 |
| - | LCD |
| - | RTC |

## 3.3 General Purpose Input/Output (GPIO)

EFM32GG11 has up to 144 General Purpose Input/Output pins. GPIO are organized on three independent supply rails, allowing for interface to multiple logic levels in the system simultaneously. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

## 3.4 Clocking

### 3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32GG11. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

### 3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

### 3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

## 3.6 Communications and Other Digital Peripherals

### 3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- $I^2S$

### 3.6.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter is a subset of the USART module, supporting full duplex asynchronous UART communication with hardware flow control and RS-485.

### 3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

### 3.6.4 Inter-Integrated Circuit Interface ($I^2C$)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$ bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the $I^2C$ module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

### 3.6.5 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices. The interface is memory mapped into the address bus of the Cortex-M4. This enables seamless access from software without manually manipulating the I/O settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface to external devices. Timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

The EBI contains a TFT controller which can drive a TFT via an RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

### 3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

### 3.8.5 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

### 3.8.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

### 3.8.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

### 3.8.8 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x36 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

## 3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32GG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

## 3.10 Core and Memory

### 3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor with FPU achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 2048 kB flash program memory
  - Dual-bank memory with read-while-write support
- Up to 512 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire or 4-pin JTAG debug interface

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode[3] | $I_{ACTIVE\_LPM}$ | 32 MHz HFRCO, CPU running while loop from flash | — | 82 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 83 | — | µA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 88 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 257 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1] | $I_{ACTIVE\_CCM\_VS}$ | 19 MHz HFRCO, CPU running while loop from flash | — | 117 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1231 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode[3] | $I_{ACTIVE\_LPM\_VS}$ | 19 MHz HFRCO, CPU running while loop from flash | — | 72 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 219 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2] | $I_{EM1\_DCM}$ | 72 MHz HFRCO | — | 42 | — | µA/MHz |
| | | 50 MHz crystal | — | 46 | — | µA/MHz |
| | | 48 MHz HFRCO | — | 46 | — | µA/MHz |
| | | 32 MHz HFRCO | — | 53 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 57 | — | µA/MHz |
| | | 16 MHz HFRCO | — | 72 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 663 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode[3] | $I_{EM1\_LPM}$ | 32 MHz HFRCO | — | 42 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 43 | — | µA/MHz |
| | | 16 MHz HFRCO | — | 48 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 219 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2] | $I_{EM1\_DCM\_VS}$ | 19 MHz HFRCO | — | 60 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 637 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode[3] | $I_{EM1\_LPM\_VS}$ | 19 MHz HFRCO | — | 39 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 190 | — | µA/MHz |
| Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode[3] | $I_{EM2\_VS}$ | Full 512 kB RAM retention and RTCC running from LFXO | — | 2.8 | — | µA |
| | | Full 512 kB RAM retention and RTCC running from LFRCO | — | 3.1 | — | µA |
| | | 16 kB (1 bank) RAM retention and RTCC running from LFRCO[5] | — | 2.1 | — | µA |
| Current consumption in EM3 mode, with voltage scaling enabled | $I_{EM3\_VS}$ | Full 512 kB RAM retention and CRYOTIMER running from ULFRCO | — | 2.4 | — | µA |

#### 4.1.10.3 Low-Frequency RC Oscillator (LFRCO)

**Table 4.14. Low-Frequency RC Oscillator (LFRCO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillation frequency | $f_{LFRCO}$ | ENVREF[2] = 1 | TBD | 32.768 | TBD | kHz |
| | | ENVREF[2] = 1, T > 85 °C | TBD | 32.768 | TBD | kHz |
| | | ENVREF[2] = 0 | TBD | 32.768 | TBD | kHz |
| Startup time | $t_{LFRCO}$ | | — | 500 | — | µs |
| Current consumption [1] | $I_{LFRCO}$ | ENVREF = 1 in CMU_LFRCOCTRL | — | 370 | — | nA |
| | | ENVREF = 0 in CMU_LFRCOCTRL | — | 520 | — | nA |

**Note:**
1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. In CMU_LFRCOCTRL register.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, $V_{INPUT}$ = 0.5 V, $V_{OUTPUT}$ = 1.5 V. Nominal voltage gain is 3.
2. If the maximum $C_{LOAD}$ is exceeded, an isolation resistor is required for stability. See AN0038 for more information.
3. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3, or the OPAMP may not be stable.
4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 µA current when the OPAMP drives 1.5 V between output and ground.
5. Step between 0.2V and $V_{OPA}$-0.2V, 10%-90% rising/falling range.
6. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1mV.
7. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network.
8. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. $V_{INPUT}$ = 0.5 V, $V_{OUTPUT}$ = 0.5 V.
9. When HCMDIS=1 and input common mode transitions the region from $V_{OPA}$-1.4V to $V_{OPA}$-1V, input offset will change. PSRR and CMRR specifications do not apply to this transition region.

### 4.1.20 LCD Driver

**Table 4.28. LCD Driver**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frame rate | $f_{LCDFR}$ | | TBD | — | TBD | Hz |
| LCD supply range[2] | $V_{LCDIN}$ | | 1.8 | — | 3.8 | V |
| LCD output voltage range | $V_{LCD}$ | Current source mode, No external LCD capacitor | 2.0 | — | $V_{LCDIN}$-0.4 | V |
| | | Step-down mode with external LCD capacitor | 2.0 | — | $V_{LCDIN}$ | V |
| | | Charge pump mode with external LCD capacitor | 2.0 | — | 1.9 * $V_{LCDIN}$ | V |
| Contrast control step size | $STEP_{CONTRAST}$ | Current source mode | — | 64 | — | mV |
| | | Charge pump or Step-down mode | — | 43 | — | mV |
| Contrast control step accuracy[1] | $ACC_{CONTRAST}$ | | — | +/-4 | — | % |

**Note:**

1. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation.
2. $V_{LCDIN}$ is selectable between the AVDD or DVDD supply pins, depending on EMU_PWRCTRL_ANASW.

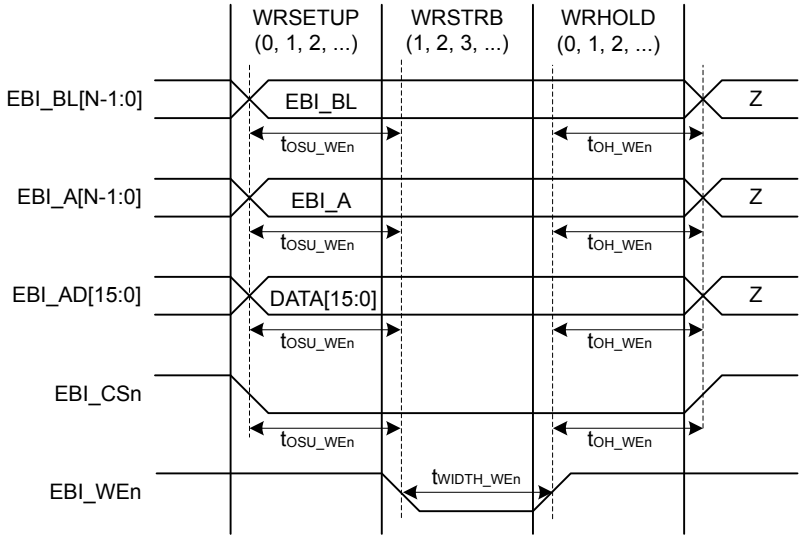


**Figure 4.3. EBI Write Enable Output Timing Diagram**

### EBI Address Latch Enable Output Timing

Timing applies to multiplexed addressing modes D8A24ALE and D16A16ALE for both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.37. EBI Address Latch Enable Output Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output hold time, from trailing EBI_ALE edge to EBI_AD invalid[1] [2] | $t_{OH\_ALEn}$ | IOVDD ≥ 1.62 V | -22 + (ADDRHOLD * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -11 + (ADDRHOLD * $t_{HFCORECLK}$) | — | — | ns |
| Output setup time, from EBI_AD valid to leading EBI_ALE edge | $t_{OSU\_ALEn}$ | IOVDD ≥ 1.62 V | -12 | — | — | ns |
| | | IOVDD ≥ 3.0 V | -9 | — | — | ns |
| EBI_ALEn pulse width[1] | $t_{WIDTH\_ALEn}$ | IOVDD ≥ 1.62 V | -4 + ((ADDRSETUP + 1) * $t_{\{\}HFCORECLK\{\}}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -3 + ((ADDRSETUP + 1) * $t_{\{\}HFCORECLK\{\}}$) | — | — | ns |

**Note:**

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALEn can be moved to the left by setting HALFALE=1. This decreases the length of $t_{WIDTH\_ALEn}$ and increases the length of $t_{OSU\_ALEn}$ by $t_{HFCORECLK}$ - 1/2 * $t_{HFCLKNODIV}$.
2. The figure shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

### EBI Read Enable Output Timing

Timing applies to both EBI_REn and EBI_NANDREn for all addressing modes and both polarities. Output timing for EBI_AD applies only to multiplexed addressing modes D8A24ALE and D16A16ALE. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.38. EBI Read Enable Output Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output hold time, from trailing EBI_REn / EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid | $t_{OH\_REn}$ | IOVDD ≥ 1.62 V | -23 + (RDHOLD * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -13 + (RDHOLD * $t_{HFCORECLK}$) | — | — | ns |
| Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_REn / EBI_NANDREn edge [1] | $t_{OSU\_REn}$ | IOVDD ≥ 1.62 V | -12 + (RDSETUP * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -11 + (RDSETUP * $t_{HFCORECLK}$) | — | — | ns |
| EBI_REn pulse width[1] [2] | $t_{WIDTH\_REn}$ | IOVDD ≥ 1.62 V | -6 + (MAX(1, RDSTRB) * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -4 + (MAX(1, RDSTRB) * $t_{HFCORECLK}$) | — | — | ns |

**Note:**

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of $t_{WIDTH\_REn}$ and increases the length of $t_{OSU\_REn}$ by 1/2 * $t_{HFCLKNODIV}$.
2. When page mode is used, RDSTRB is replaced by RDPA for page hits.

### EBI TFT Output Timing

All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.39. EBI TFT Output Timing**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output hold time, EBI_DCLK to EBI_AD invalid | $t_{OH\_DCLK}$ | IOVDD ≥ 1.62 V | -23 + (TFTHOLD * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -12 + (TFTHOLD * $t_{HFCORECLK}$) | — | — | ns |
| Output setup time, EBI_AD valid to EBI_DCLK | $t_{OSU\_DCLK}$ | IOVDD ≥ 1.62 V | -11 + (TFTSETUP * $t_{HFCORECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | -9 + (TFTSETUP * $t_{HFCORECLK}$) | — | — | ns |

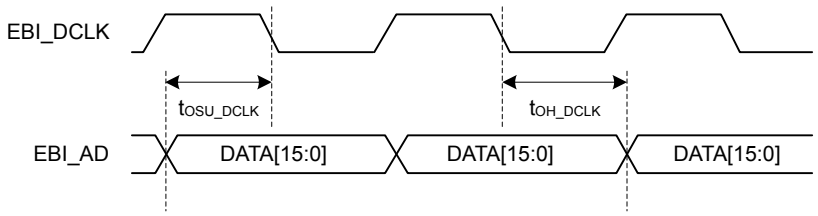


**Figure 4.6. EBI TFT Output Timing**

### SDIO SDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

**Table 4.48. SDIO SDR Mode Timing (Location 0)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency during data transfer | $F_{SD\_CLK}$ | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 20 | MHz |
| | | Using HFXO | — | — | TBD | MHz |
| Clock low time | $t_{WL}$ | Using HFRCO, AUXHFRCO, or USHFRCO | 22.6 | — | — | ns |
| | | Using HFXO | TBD | — | — | ns |
| Clock high time | $t_{WH}$ | Using HFRCO, AUXHFRCO, or USHFRCO | 22.6 | — | — | ns |
| | | Using HFXO | TBD | — | — | ns |
| Clock rise time | $t_R$ | | 0.99 | 4.68 | — | ns |
| Clock fall time | $t_F$ | | 0.90 | 3.64 | — | ns |
| Input setup time, CMD, DAT[0:3] valid to SD_CLK | $t_{ISU}$ | | 8 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:3] change | $t_{IH}$ | | 1.5 | — | — | ns |
| Output delay time, SD_CLK to CMD, DAT[0:3] valid | $t_{ODLY}$ | | 0 | — | 35 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:3] change | $t_{OH}$ | | 0.8 | — | — | ns |

### SDIO MMC DDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

**Table 4.52. SDIO MMC DDR Mode Timing (Location 0, 1.8V I/O)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency during data transfer | $F_{SD\_CLK}$ | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 18 | MHz |
| | | Using HFXO | — | — | TBD | MHz |
| Clock low time | $t_{WL}$ | Using HFRCO, AUXHFRCO, or USHFRCO | 25.1 | — | — | ns |
| | | Using HFXO | TBD | — | — | ns |
| Clock high time | $t_{WH}$ | Using HFRCO, AUXHFRCO, or USHFRCO | 25.1 | — | — | ns |
| | | Using HFXO | TBD | — | — | ns |
| Clock rise time | $t_R$ | | 1.13 | 5.21 | — | ns |
| Clock fall time | $t_F$ | | 1.01 | 4.10 | — | ns |
| Input setup time, CMD valid to SD_CLK | $t_{ISU}$ | | 5.3 | — | — | ns |
| Input hold time, SD_CLK to CMD change | $t_{IH}$ | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD valid | $t_{ODLY}$ | | 0 | — | 16 | ns |
| Output hold time, SD_CLK to CMD change | $t_{OH}$ | | 3 | — | — | ns |
| Input setup time, DAT[0:7] valid to SD_CLK | $t_{ISU2X}$ | | 5.3 | — | — | ns |
| Input hold time, SD_CLK to DAT[0:7] change | $t_{IH2X}$ | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to DAT[0:7] valid | $t_{ODLY2X}$ | | 0 | — | 16 | ns |
| Output hold time, SD_CLK to DAT[0:7] change | $t_{OH2X}$ | | 3 | — | — | ns |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PF3 | 79 | GPIO | PF4 | 80 | GPIO |
| PF5 | 81 | GPIO | PF6 | 84 | GPIO |
| PF7 | 85 | GPIO | PF8 | 86 | GPIO |
| PF9 | 87 | GPIO | PD9 | 88 | GPIO |
| PD10 | 89 | GPIO | PD11 | 90 | GPIO |
| PD12 | 91 | GPIO | PE8 | 92 | GPIO |
| PE9 | 93 | GPIO | PE10 | 94 | GPIO |
| PE11 | 95 | GPIO | PE12 | 96 | GPIO |
| PE13 | 97 | GPIO | PE14 | 98 | GPIO |
| PE15 | 99 | GPIO | PA15 | 100 | GPIO |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | EBI | Timers | Communication | Other |
| PD15 | | EBI_NANDREn #1 | TIM2_CDTI2 #1 TIM3_CC0 #7 WTIM0_CDTI0 #1 PCNT1_S0IN #2 | ETH_TSUEXTCLK #1 CAN0_TX #5 US5_CTS #1 I2C0_SCL #3 | |
| PC13 | VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSACMP1Y BUSACMP1X | EBI_ARDY #4 | TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 TIM5_CC2 #5 WTIM3_CC2 #2 PCNT0_S0IN #0 PCNT2_S1IN #4 | US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3 U1_RX #0 I2C2_SCL #6 | LES_CH13 PRS_CH21 #1 ACMP3_O #3 |
| PC12 | VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSACMP1Y BUSACMP1X | | TIM1_CC3 #0 TIM5_CC1 #5 WTIM3_CC1 #2 PCNT2_S0IN #4 | CAN1_RX #4 US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3 U1_TX #0 I2C2_SDA #6 | CMU_CLK0 #1 LES_CH12 PRS_CH20 #1 |
| PC11 | BUSACMP1Y BUSACMP1X | EBI_ALE #4 EBI_ALE #5 EBI_A23 #1 | TIM5_CC0 #5 WTIM3_CC0 #2 | CAN1_TX #4 US0_TX #2 I2C1_SDA #4 | LES_CH11 PRS_CH19 #1 |
| PA3 | BUSAY BUSBX LCD_SEG16 | EBI_AD12 #0 EBI_VSNC #3 | TIM0_CDTI0 #0 TIM3_CC0 #5 | ETH_RMIIREFCLK #0 ETH_MIITXD1 #0 SDIO_DAT3 #1 US3_CS #0 U0_TX #2 QSPI0_DQ1 #1 | CMU_CLK2 #1 CMU_CLKI0 #1 CMU_CLK2 #4 LES_ALTEX2 PRS_CH9 #1 ETM_TD1 #3 |
| PG2 | BUSACMP2Y BUSACMP2X | EBI_AD02 #2 | TIM6_CC2 #0 TIM2_CDTI2 #3 WTIM0_CC0 #2 LETIM1_OUT0 #7 | ETH_MIITXD2 #1 US3_CLK #4 QSPI0_DQ1 #2 | CMU_CLK0 #3 |
| PG1 | BUSACMP2Y BUSACMP2X | EBI_AD01 #2 | TIM6_CC1 #0 TIM2_CDTI1 #3 WTIM0_CDTI2 #1 LETIM1_OUT1 #6 | ETH_MIITXD3 #1 US3_RX #4 QSPI0_DQ0 #2 | CMU_CLK1 #3 |
| PC10 | BUSACMP1Y BUSACMP1X | EBI_A10 #2 EBI_A22 #1 | TIM2_CC2 #2 TIM5_CC2 #4 WTIM3_CC2 #1 | CAN1_TX #3 US0_RX #2 | LES_CH10 PRS_CH18 #1 |
| PC9 | BUSACMP1Y BUSACMP1X | EBI_A09 #2 EBI_A21 #1 EBI_A27 #3 | TIM2_CC1 #2 TIM5_CC1 #4 WTIM3_CC1 #1 | CAN1_RX #3 US0_CLK #2 | LES_CH9 PRS_CH5 #0 GPIO_EM4WU2 |
| PC8 | BUSACMP1Y BUSACMP1X | EBI_A08 #2 EBI_A15 #0 EBI_A20 #1 EBI_A26 #3 | TIM2_CC0 #2 TIM5_CC0 #4 WTIM3_CC0 #1 | US0_CS #2 | LES_CH8 PRS_CH4 #0 |
| PA4 | BUSBY BUSAX LCD_SEG17 | EBI_AD13 #0 EBI_HSNC #3 | TIM0_CDTI1 #0 TIM3_CC1 #5 | ETH_RMIICRSDV #0 ETH_MIITXD0 #0 SDIO_DAT4 #1 US3_CTS #0 U0_RX #2 QSPI0_DQ2 #1 | LES_ALTEX3 PRS_CH16 #0 ETM_TD2 #3 |
| PG4 | BUSACMP2Y BUSACMP2X | EBI_AD04 #2 | TIM6_CDTI1 #0 WTIM0_CC2 #2 | ETH_MIITXD0 #1 US3_CTS #4 QSPI0_DQ3 #2 | |

| Alternate | LOCATION | | |
|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| EBI_A10 | 0: PE3<br>1: PD6<br>2: PC10<br>3: PB10 | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | 0: PE4<br>1: PD7<br>2: PI6<br>3: PB11 | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | 0: PE5<br>1: PD8<br>2: PI7<br>3: PB12 | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | 0: PE6<br>1: PC7<br>2: PI8<br>3: PD0 | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | 0: PE7<br>1: PE2<br>2: PI9<br>3: PD1 | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | 0: PC8<br>1: PE3<br>2: PI10<br>3: PD2 | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | 0: PB0<br>1: PE4<br>2: PH4<br>3: PD3 | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | 0: PB1<br>1: PE5<br>2: PH5<br>3: PD4 | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | 0: PB2<br>1: PE6<br>2: PH6<br>3: PD5 | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | 0: PB3<br>1: PE7<br>2: PH7<br>3: PD6 | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | 0: PB4<br>1: PC8<br>2: PH8<br>3: PD7 | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | 0: PB5<br>1: PC9<br>2: PH9<br>3: PC7 | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | 0: PB6<br>1: PC10<br>2: PH10<br>3: PE4 | | External Bus Interface (EBI) address output pin 22. |

| Alternate | LOCATION | | |
|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| EBI_AD08 | 0: PA15<br>1: PC1<br>2: PG8 | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | 0: PA0<br>1: PC2<br>2: PG9 | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | 0: PA1<br>1: PC3<br>2: PG10 | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | 0: PA2<br>1: PC4<br>2: PG11 | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | 0: PA3<br>1: PC5<br>2: PG12 | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | 0: PA4<br>1: PA7<br>2: PG13 | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | 0: PA5<br>1: PA8<br>2: PG14 | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | 0: PA6<br>1: PA9<br>2: PG15 | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | 0: PF3<br>1: PB9<br>2: PC4<br>3: PB5 | 4: PC11<br>5: PC11 | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | 0: PF2<br>1: PD13<br>2: PB15<br>3: PB4 | 4: PC13<br>5: PF10 | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | 0: PF6<br>1: PF8<br>2: PB10<br>3: PC1 | 4: PF6<br>5: PF6 | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | 0: PF7<br>1: PF9<br>2: PB11<br>3: PC3 | 4: PF7<br>5: PF7 | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | 0: PD9<br>1: PA10<br>2: PC0<br>3: PB0 | 4: PE8 | External Bus Interface (EBI) Chip Select output 0. |

| Alternate Functionality | Location | Priority |
|---|---|---|
| QSPI0_DQS | 0: PF9 | High Speed |
| QSPI0_SCLK | 0: PF6 | High Speed |
| SDIO_CLK | 0: PE13 | High Speed |
| SDIO_CMD | 0: PE12 | High Speed |
| SDIO_DAT0 | 0: PE11 | High Speed |
| SDIO_DAT1 | 0: PE10 | High Speed |
| SDIO_DAT2 | 0: PE9 | High Speed |
| SDIO_DAT3 | 0: PE8 | High Speed |
| SDIO_DAT4 | 0: PD12 | High Speed |
| SDIO_DAT5 | 0: PD11 | High Speed |
| SDIO_DAT6 | 0: PD10 | High Speed |
| SDIO_DAT7 | 0: PD9 | High Speed |
| TIM0_CC0 | 3: PB6 | Non-interference |
| TIM0_CC1 | 3: PC0 | Non-interference |
| TIM0_CC2 | 3: PC1 | Non-interference |
| TIM0_CDTI0 | 1: PC13 | Non-interference |
| TIM0_CDTI1 | 1: PC14 | Non-interference |
| TIM0_CDTI2 | 1: PC15 | Non-interference |
| TIM2_CC0 | 0: PA8 | Non-interference |
| TIM2_CC1 | 0: PA9 | Non-interference |
| TIM2_CC2 | 0: PA10 | Non-interference |
| TIM2_CDTI0 | 0: PB0 | Non-interference |
| TIM2_CDTI1 | 0: PB1 | Non-interference |
| TIM2_CDTI2 | 0: PB2 | Non-interference |
| TIM4_CC0 | 0: PF3 | Non-interference |
| TIM4_CC1 | 0: PF4 | Non-interference |
| TIM4_CC2 | 0: PF12 | Non-interference |
| TIM4_CDTI0 | 0: PD0 | Non-interference |
| TIM4_CDTI1 | 0: PD1 | Non-interference |
| TIM4_CDTI2 | 0: PD3 | Non-interference |
| TIM6_CC0 | 0: PG0 | Non-interference |
| TIM6_CC1 | 0: PG1 | Non-interference |
| TIM6_CC2 | 0: PG2 | Non-interference |
| TIM6_CDTI0 | 0: PG3 | Non-interference |
| TIM6_CDTI1 | 0: PG4 | Non-interference |
| TIM6_CDTI2 | 0: PG5 | Non-interference |

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **OPA2_OUT** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT4Y | BUSDY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | | | PE0 |
| APORT3Y | BUSCY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | | | PE1 | |
| APORT2Y | BUSBY | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT1Y | BUSAY | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | |
| **OPA2_P** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1X | BUSAX | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT2X | BUSBX | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | |
| APORT3X | BUSCX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | | | PE0 |
| APORT4X | BUSDX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | | | PE1 | |
| **OPA3_N** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | |
| APORT2Y | BUSBY | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT3Y | BUSCY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | | | PE1 | |
| APORT4Y | BUSDY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | | | PE0 |

**Table 7.2. BGA152 PCB Land Pattern Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| X | | 0.20 | |
| C1 | | 6.50 | |
| C2 | | 6.50 | |
| E1 | | 0.5 | |
| E2 | | 0.5 | |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

# 13. Revision History

### Revision 0.6

March, 2018

- Removed "Confindential" watermark.
- Updated 4.1 Electrical Characteristics and 4.2 Typical Performance Curves with latest characterization data.

### Revision 0.2

October, 2017

- Updated memory maps to latest formatting and to include all peripherals.
- Updated all electrical specifications tables with latest characterization results.
- **Absolute Maximum Ratings** Table:
  - Removed redundant $I_{VSSMAX}$ line.
  - Added footnote to clarify $V_{DIGPIN}$ specification for 5V tolerant GPIO.
- **General Operating Conditions** Table:
  - Removed $dV_{DD}$ specification and redundant footnote about shorting VREGVDD and AVDD together.
  - Added footnote about IOVDD voltage restriction when CSEN peripheral is used with chopping enabled.
- **Flash Memory Characteristics** Table: Added timing measurement clarification for Device Erase and Mass Erase.
- **Analog to Digital Converter (ADC)** Table:
  - Added header text for general specification conditions.
  - Added footnote for clarification of input voltage limits.
- Minor typographical corrections, including capitalization, mis-spellings and punctuation marks, throughout document.
- Minor formatting and styling updates, including table formats, TOC location, and boilerplate information throughout document.

### Revision 0.1

April 27th, 2017

Initial release.