Silicon Labs - EFM32GG11B840F1024GL120-AR Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	95
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024gl120-ar

- **Timers/Counters**
  - 7× 16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels (4 + 4 on one timer instance)
    - Dead-Time Insertion on several timer instances
  - 4× 32-bit Timer/Counter
  - 32-bit Real Time Counter and Calendar (RTCC)
  - 24-bit Real Time Counter (RTC)
  - 32-bit Ultra Low Energy CRYOTIMER for periodic wakeup from any Energy Mode
  - 2× 16-bit Low Energy Timer for waveform generation
  - 3× 16-bit Pulse Counter with asynchronous operation
  - 2× Watchdog Timer with dedicated RC oscillator
- **Low Energy Sensor Interface (LESENSE)**
  - Autonomous sensor monitoring in Deep Sleep Mode
  - Wide range of sensors supported, including LC sensors and capacitive buttons
  - Up to 16 inputs
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
  - 2-pin Serial Wire Debug interface
  - 1-pin Serial Wire Viewer
  - 4-pin JTAG interface
  - Embedded Trace Macrocell (ETM)
- **Pre-Programmed USB/UART Bootloader**
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - Standard (-40 °C to 85 °C T_{AMB}) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
  - QFN64 (9x9 mm)
  - TQFP64 (10x10 mm)
  - TQFP100 (14x14 mm)
  - BGA112 (10x10 mm)
  - BGA120 (7x7 mm)
  - BGA152 (8x8 mm)
  - BGA192 (7x7mm)

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.10.4 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the [**Documentation**] area.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
Voltage on supply pins other than VREGI and VBUS	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1	V / µs
DC voltage on any GPIO pin	V_{DIGPIN}	5V tolerant GPIO pins[1 2 3]	-0.3	—	Min of 5.25 and IOVDD +2	V
		LCD pins[3]	-0.3	—	Min of 3.8 and IOVDD +2	V
		Standard GPIO pins	-0.3	—	IOVDD+0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA
Junction temperature	T_J	-G grade devices	-40	—	105	°C
		-I grade devices	-40	—	125	°C
Voltage on regulator supply pins VREGI and VBUS	V_{VREGI}		-0.3	—	5.5	V

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.
2. Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.
3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.
6. The maximum limit on T_A may be lower due to device self-heating, which depends on the power dissipation of the specific application. T_A (max) = T_J (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_J and $THETA_{JA}$.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal resistance, QFN64 Package	$THETA_{JA\_QFN64}$	4-Layer PCB, Air velocity = 0 m/s	—	17.8	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	15.4	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	13.8	—	°C/W
Thermal resistance, TQFP64 Package	$THETA_{JA\_TQFP64}$	4-Layer PCB, Air velocity = 0 m/s	—	33.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	32.1	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	30.1	—	°C/W
Thermal resistance, TQFP100 Package	$THETA_{JA\_TQFP100}$	4-Layer PCB, Air velocity = 0 m/s	—	44.1	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	37.7	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	35.5	—	°C/W
Thermal resistance, BGA112 Package	$THETA_{JA\_BGA112}$	4-Layer PCB, Air velocity = 0 m/s	—	42.0	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	37.0	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	35.3	—	°C/W
Thermal resistance, BGA120 Package	$THETA_{JA\_BGA120}$	4-Layer PCB, Air velocity = 0 m/s	—	47.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	41.8	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	39.6	—	°C/W
Thermal resistance, BGA152 Package	$THETA_{JA\_BGA152}$	4-Layer PCB, Air velocity = 0 m/s	—	35.7	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	31.0	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	29.5	—	°C/W
Thermal resistance, BGA192 Package	$THETA_{JA\_BGA192}$	4-Layer PCB, Air velocity = 0 m/s	—	47.9	—	°C/W
		4-Layer PCB, Air velocity = 1 m/s	—	41.8	—	°C/W
		4-Layer PCB, Air velocity = 2 m/s	—	39.6	—	°C/W

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode[3]	I_{ACTIVE_LPM}	32 MHz HFRCO, CPU running while loop from flash	—	82	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	83	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	88	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	257	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1]	$I_{ACTIVE\_CCM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	117	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1231	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode[3]	$I_{ACTIVE\_LPM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	72	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	219	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{EM1_DCM}	72 MHz HFRCO	—	42	—	µA/MHz
		50 MHz crystal	—	46	—	µA/MHz
		48 MHz HFRCO	—	46	—	µA/MHz
		32 MHz HFRCO	—	53	—	µA/MHz
		26 MHz HFRCO	—	57	—	µA/MHz
		16 MHz HFRCO	—	72	—	µA/MHz
		1 MHz HFRCO	—	663	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode[3]	I_{EM1_LPM}	32 MHz HFRCO	—	42	—	µA/MHz
		26 MHz HFRCO	—	43	—	µA/MHz
		16 MHz HFRCO	—	48	—	µA/MHz
		1 MHz HFRCO	—	219	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2]	$I_{EM1\_DCM\_VS}$	19 MHz HFRCO	—	60	—	µA/MHz
		1 MHz HFRCO	—	637	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode[3]	$I_{EM1\_LPM\_VS}$	19 MHz HFRCO	—	39	—	µA/MHz
		1 MHz HFRCO	—	190	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode[3]	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	2.8	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	3.1	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[5]	—	2.1	—	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.4	—	µA

4.1.10 Oscillators

4.1.10.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.12. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}		6	—	18	pF
On-chip tuning cap range [2]	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup [3]	I_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2, AGC[4] = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{LFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency limits	f_{HFRCO_BAND}	FREQRANGE = 0, FINETUNINGEN = 0	1	—	10	MHz
		FREQRANGE = 3, FINETUNINGEN = 0	2	—	17	MHz
		FREQRANGE = 6, FINETUNINGEN = 0	4	—	30	MHz
		FREQRANGE = 7, FINETUNINGEN = 0	5	—	34	MHz
		FREQRANGE = 8, FINETUNINGEN = 0	7	—	42	MHz
		FREQRANGE = 10, FINETUNINGEN = 0	12	—	58	MHz
		FREQRANGE = 11, FINETUNINGEN = 0	15	—	68	MHz
		FREQRANGE = 12, FINETUNINGEN = 0	18	—	83	MHz
		FREQRANGE = 13, FINETUNINGEN = 0	24	—	100	MHz
		FREQRANGE = 14, FINETUNINGEN = 0	28	—	119	MHz
		FREQRANGE = 15, FINETUNINGEN = 0	33	—	138	MHz
		FREQRANGE = 16, FINETUNINGEN = 0	43	—	163	MHz

Note:

1. Maximum DPLL lock time ~= 6 x (M+1) x t_{REF}, where t_{REF} is the reference clock period.

4.1.12 General-Purpose I/O (GPIO)

Table 4.20. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	IOVDD*0.3	V
Input high voltage	V_{IH}	GPIO pins	IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C	—	0.1	TBD	nA
		All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C	—	—	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD, T > 85 °C	—	—	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	TBD	µA
I/O pin pull-up/pull-down resistor	R_{PUD}		TBD	40	TBD	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		15	25	35	ns

SDIO MMC DDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Table 4.53. SDIO MMC DDR Mode Timing (Location 0, 3V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.13	2.37	—	ns
Clock fall time	t_F		1.01	2.02	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		3	—	—	ns
Input setup time, DAT[0:7] valid to SD_CLK	t_{ISU2X}		5.3	—	—	ns
Input hold time, SD_CLK to DAT[0:7] change	t_{IH2X}		2.5	—	—	ns
Output delay time, SD_CLK to DAT[0:7] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:7] change	t_{OH2X}		3	—	—	ns

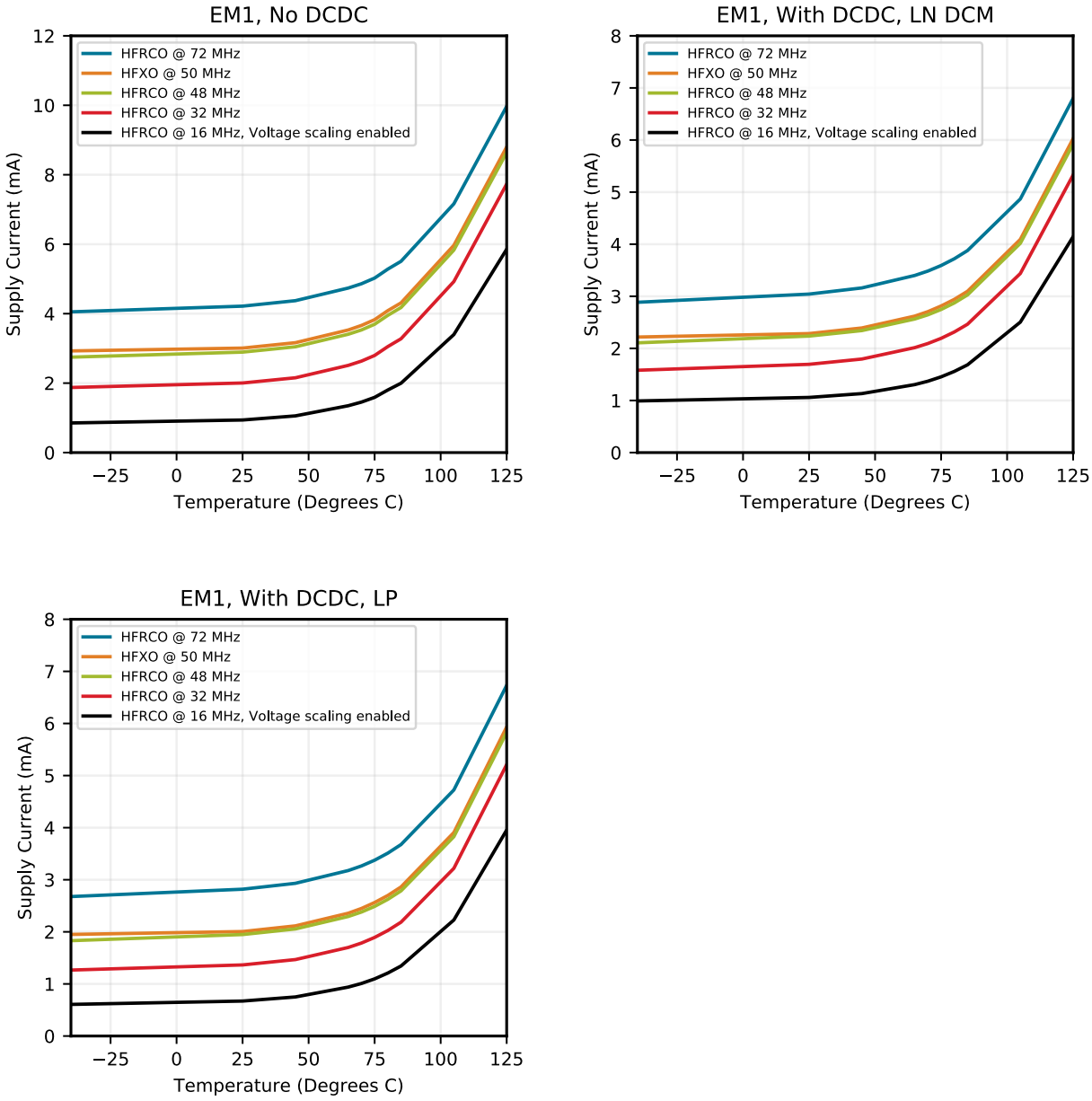

Figure 4.25. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

5.9 EFM32GG11B5xx in QFP100 Device Pinout

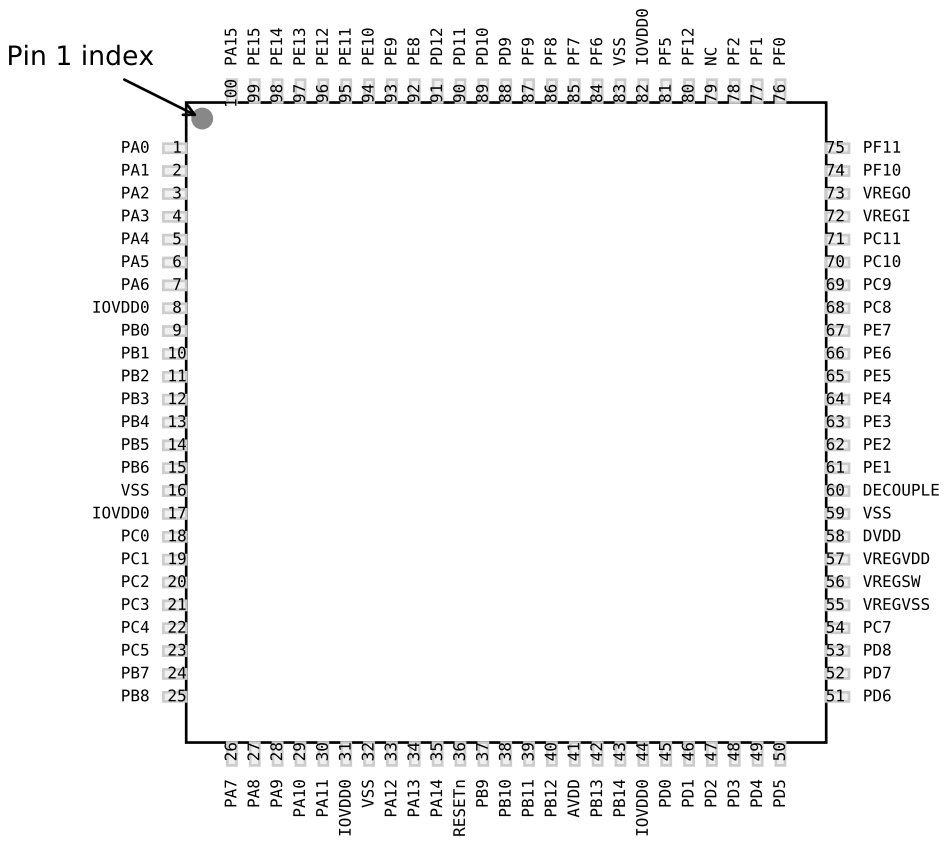

Figure 5.9. EFM32GG11B5xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.9. EFM32GG11B5xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA9	18	GPIO
PA10	19	GPIO	RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO (5V)
PC9	42	GPIO (5V)	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	57	GPIO
PE9	58	GPIO	PE10	59	GPIO
PE11	60	GPIO	PE12	61	GPIO
PE13	62	GPIO	PE14	63	GPIO
PE15	64	GPIO			

Note:
1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD15		EBI_NANDREn #1	TIM2_CDTI2 #1 TIM3_CC0 #7 WTIM0_CDTI0 #1 PCNT1_S0IN #2	ETH_TSUEXTCLK #1 CAN0_TX #5 US5_CTS #1 I2C0_SCL #3	
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSACMP1Y BUSACMP1X	EBI_ARDY #4	TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 TIM5_CC2 #5 WTIM3_CC2 #2 PCNT0_S0IN #0 PCNT2_S1IN #4	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3 U1_RX #0 I2C2_SCL #6	LES_CH13 PRS_CH21 #1 ACMP3_O #3
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSACMP1Y BUSACMP1X		TIM1_CC3 #0 TIM5_CC1 #5 WTIM3_CC1 #2 PCNT2_S0IN #4	CAN1_RX #4 US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3 U1_TX #0 I2C2_SDA #6	CMU_CLK0 #1 LES_CH12 PRS_CH20 #1
PC11	BUSACMP1Y BUSACMP1X	EBI_ALE #4 EBI_ALE #5 EBI_A23 #1	TIM5_CC0 #5 WTIM3_CC0 #2	CAN1_TX #4 US0_TX #2 I2C1_SDA #4	LES_CH11 PRS_CH19 #1
PA3	BUSAY BUSBX LCD_SEG16	EBI_AD12 #0 EBI_VSNC #3	TIM0_CDTI0 #0 TIM3_CC0 #5	ETH_RMIIREFCLK #0 ETH_MIITXD1 #0 SDIO_DAT3 #1 US3_CS #0 U0_TX #2 QSPI0_DQ1 #1	CMU_CLK2 #1 CMU_CLKI0 #1 CMU_CLK2 #4 LES_ALTEX2 PRS_CH9 #1 ETM_TD1 #3
PG2	BUSACMP2Y BUSACMP2X	EBI_AD02 #2	TIM6_CC2 #0 TIM2_CDTI2 #3 WTIM0_CC0 #2 LETIM1_OUT0 #7	ETH_MIITXD2 #1 US3_CLK #4 QSPI0_DQ1 #2	CMU_CLK0 #3
PG1	BUSACMP2Y BUSACMP2X	EBI_AD01 #2	TIM6_CC1 #0 TIM2_CDTI1 #3 WTIM0_CDTI2 #1 LETIM1_OUT1 #6	ETH_MIITXD3 #1 US3_RX #4 QSPI0_DQ0 #2	CMU_CLK1 #3
PC10	BUSACMP1Y BUSACMP1X	EBI_A10 #2 EBI_A22 #1	TIM2_CC2 #2 TIM5_CC2 #4 WTIM3_CC2 #1	CAN1_TX #3 US0_RX #2	LES_CH10 PRS_CH18 #1
PC9	BUSACMP1Y BUSACMP1X	EBI_A09 #2 EBI_A21 #1 EBI_A27 #3	TIM2_CC1 #2 TIM5_CC1 #4 WTIM3_CC1 #1	CAN1_RX #3 US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2
PC8	BUSACMP1Y BUSACMP1X	EBI_A08 #2 EBI_A15 #0 EBI_A20 #1 EBI_A26 #3	TIM2_CC0 #2 TIM5_CC0 #4 WTIM3_CC0 #1	US0_CS #2	LES_CH8 PRS_CH4 #0
PA4	BUSBY BUSAX LCD_SEG17	EBI_AD13 #0 EBI_HSNC #3	TIM0_CDTI1 #0 TIM3_CC1 #5	ETH_RMIICRSDV #0 ETH_MIITXD0 #0 SDIO_DAT4 #1 US3_CTS #0 U0_RX #2 QSPI0_DQ2 #1	LES_ALTEX3 PRS_CH16 #0 ETM_TD2 #3
PG4	BUSACMP2Y BUSACMP2X	EBI_AD04 #2	TIM6_CDTI1 #0 WTIM0_CC2 #2	ETH_MIITXD0 #1 US3_CTS #4 QSPI0_DQ3 #2	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A10	0: PE3 1: PD6 2: PC10 3: PB10		External Bus Interface (EBI) address output pin 10.
EBI_A11	0: PE4 1: PD7 2: PI6 3: PB11		External Bus Interface (EBI) address output pin 11.
EBI_A12	0: PE5 1: PD8 2: PI7 3: PB12		External Bus Interface (EBI) address output pin 12.
EBI_A13	0: PE6 1: PC7 2: PI8 3: PD0		External Bus Interface (EBI) address output pin 13.
EBI_A14	0: PE7 1: PE2 2: PI9 3: PD1		External Bus Interface (EBI) address output pin 14.
EBI_A15	0: PC8 1: PE3 2: PI10 3: PD2		External Bus Interface (EBI) address output pin 15.
EBI_A16	0: PB0 1: PE4 2: PH4 3: PD3		External Bus Interface (EBI) address output pin 16.
EBI_A17	0: PB1 1: PE5 2: PH5 3: PD4		External Bus Interface (EBI) address output pin 17.
EBI_A18	0: PB2 1: PE6 2: PH6 3: PD5		External Bus Interface (EBI) address output pin 18.
EBI_A19	0: PB3 1: PE7 2: PH7 3: PD6		External Bus Interface (EBI) address output pin 19.
EBI_A20	0: PB4 1: PC8 2: PH8 3: PD7		External Bus Interface (EBI) address output pin 20.
EBI_A21	0: PB5 1: PC9 2: PH9 3: PC7		External Bus Interface (EBI) address output pin 21.
EBI_A22	0: PB6 1: PC10 2: PH10 3: PE4		External Bus Interface (EBI) address output pin 22.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
U0_TX	0: PF6 1: PE0 2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.
U1_CTS	0: PC14 1: PF9 2: PB11 3: PE4	4: PC4 5: PH13	UART1 Clear To Send hardware flow control input.
U1_RTS	0: PC15 1: PF8 2: PB12 3: PE5	4: PC5 5: PH14	UART1 Request To Send hardware flow control output.
U1_RX	0: PC13 1: PF11 2: PB10 3: PE3	4: PE13 5: PH12	UART1 Receive input.
U1_TX	0: PC12 1: PF10 2: PB9 3: PE2	4: PE12 5: PH11	UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12 6: PG14	USART0 clock input / output.
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13 6: PG15	USART0 chip select input / output.
US0_CTS	0: PE14 1: PE3 2: PC7 3: PC13	4: PB6 5: PB11 6: PH0	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PE15 1: PE2 2: PC6 3: PC12	4: PB5 5: PD6 6: PH1	USART0 Request To Send hardware flow control output.
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1 6: PG13	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0 6: PG12	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4 6: PB2	USART1 chip select input / output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US5_RX	0: PE9 1: PA7 2: PB1 3: PH11		USART5 Asynchronous Receive. USART5 Synchronous mode Master Input / Slave Output (MISO).
US5_TX	0: PE8 1: PA6 2: PF15 3: PH10		USART5 Asynchronous Transmit. Also used as receive input in half duplex communication. USART5 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	0: PF10		USB D- pin.
USB_DP	0: PF11		USB D+ pin.
USB_ID	0: PF12		USB ID pin.
USB_VBUSEN	0: PF5		USB 5 V VBUS enable.
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6 2: PG2 3: PG8	4: PC15 5: PB0 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5 1: PD13 2: PG3 3: PG9	4: PF0 5: PB1 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM0_CC2	0: PE6 1: PD14 2: PG4 3: PG10	4: PF1 5: PB2 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0	0: PE10 1: PD15 2: PA12 3: PG11	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1	0: PE11 1: PG0 2: PA13 3: PG12	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	0: PE12 1: PG1 2: PA14 3: PG13	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	4: PE3 5: PE7 6: PH8 7: PH12	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14 1: PD3 2: PD7 3: PE0	4: PE4 5: PI0 6: PH9 7: PH13	Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	0: PD0 1: PD4 2: PD8 3: PE1	4: PE5 5: PI1 6: PH10 7: PH14	Wide timer 1 Capture Compare input / output channel 2.
WTIM1_CC3	0: PD1 1: PD5 2: PC6 3: PE2	4: PE6 5: PI2 6: PH11 7: PH15	Wide timer 1 Capture Compare input / output channel 3.
WTIM2_CC0	0: PA9 1: PA12 2: PB9 3: PB12	4: PG14 5: PD3 6: PH4 7: PH7	Wide timer 2 Capture Compare input / output channel 0.
WTIM2_CC1	0: PA10 1: PA13 2: PB10 3: PG12	4: PG15 5: PD4 6: PH5 7: PH8	Wide timer 2 Capture Compare input / output channel 1.
WTIM2_CC2	0: PA11 1: PA14 2: PB11 3: PG13	4: PH0 5: PD5 6: PH6 7: PH9	Wide timer 2 Capture Compare input / output channel 2.
WTIM3_CC0	0: PD9 1: PC8 2: PC11 3: PC14	4: PI3 5: PI6 6: PB6 7: PF13	Wide timer 3 Capture Compare input / output channel 0.
WTIM3_CC1	0: PD10 1: PC9 2: PC12 3: PF10	4: PI4 5: PI7 6: PF4 7: PF14	Wide timer 3 Capture Compare input / output channel 1.

7. BGA152 Package Specifications

7.1 BGA152 Package Dimensions

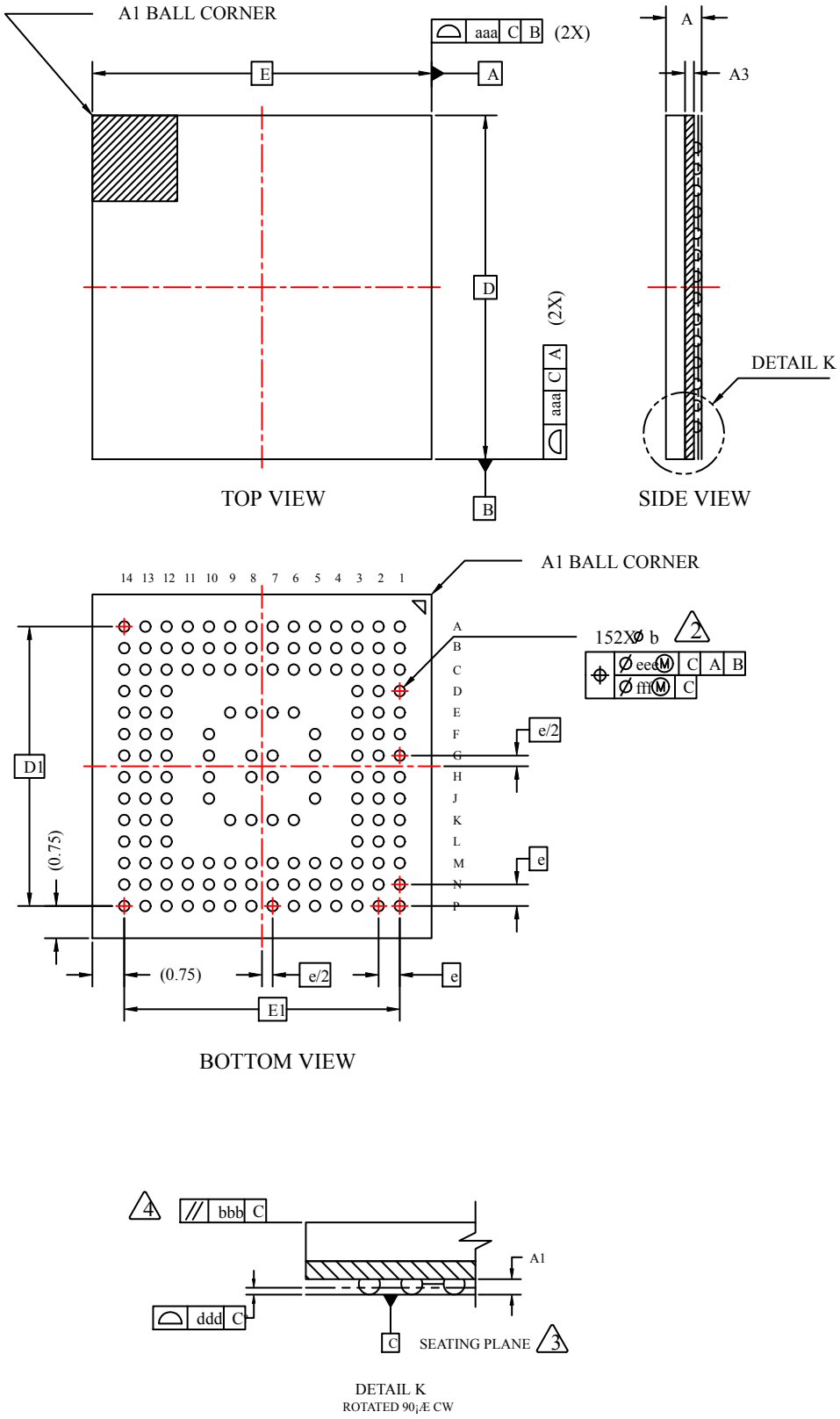

Figure 7.1. BGA152 Package Drawing

8.3 BGA120 Package Marking

Figure 8.3. BGA120 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

Table 9.2. BGA112 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.45	
C1		8.00	
C2		8.00	
E1		0.8	
E2		0.8	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.