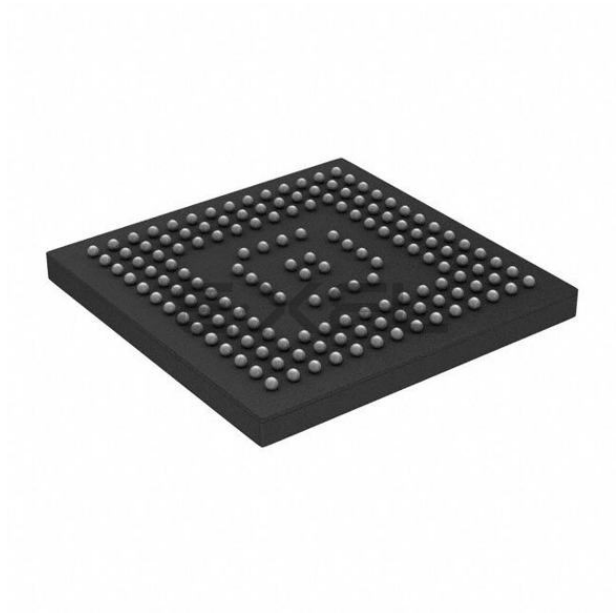

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	152-VFBGA
Supplier Device Package	152-BGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024gl152-ar

3. System Overview

3.1 Introduction

The Giant Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Giant Gecko Series 1 Reference Manual.

A block diagram of the Giant Gecko Series 1 family is shown in Figure 3.1 Detailed EFM32GG11 Block Diagram on page 11. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

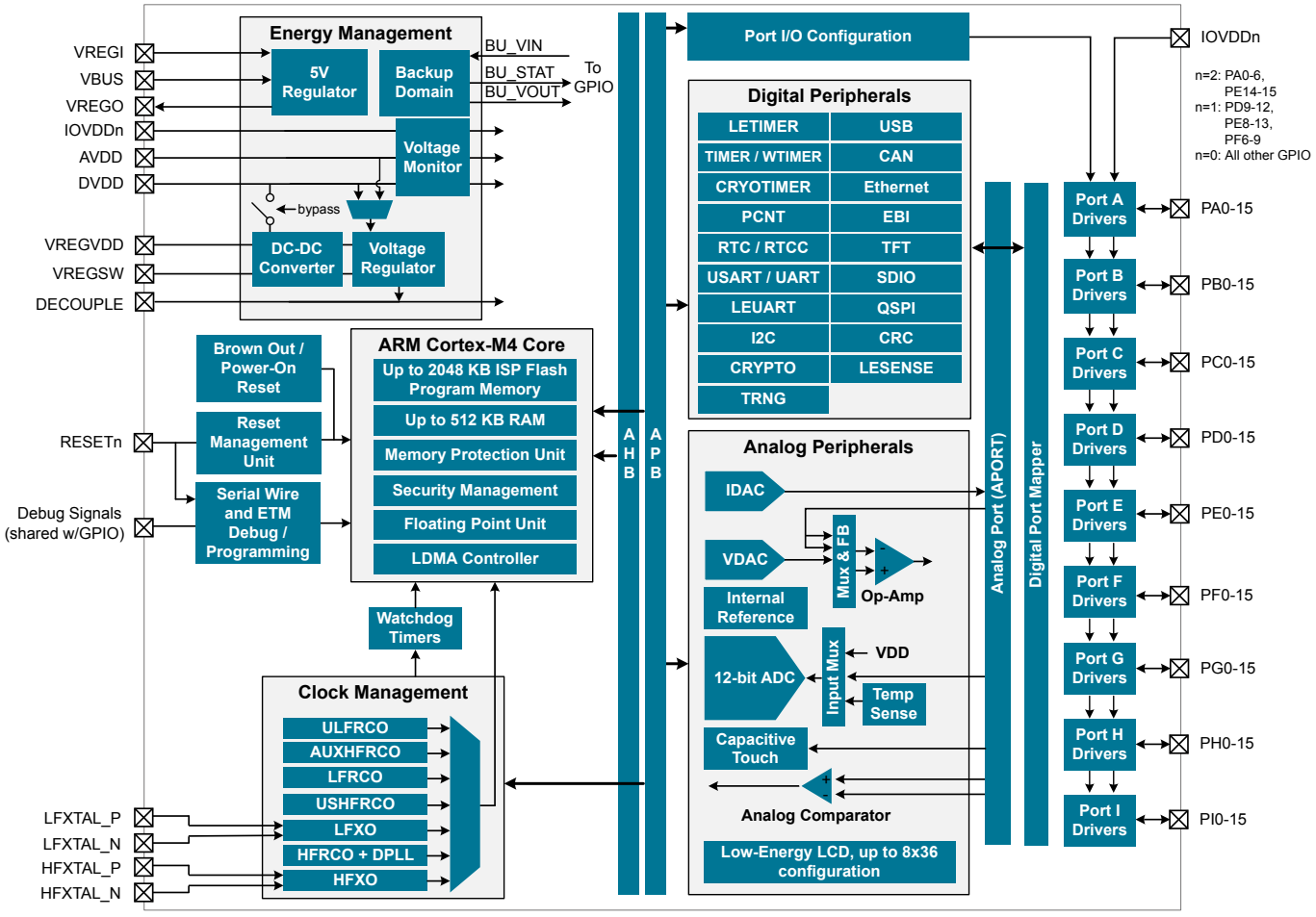

Figure 3.1. Detailed EFM32GG11 Block Diagram

4.1.6 Backup Supply Domain

Table 4.6. Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Backup supply voltage range	V_{BU_VIN}		1.8	—	3.8	V
PWRRES resistor	R_{PWRRES}	EMU_BUCTRL_PWRRES = RES0	3400	3900	4400	Ω
		EMU_BUCTRL_PWRRES = RES1	1450	1800	2150	Ω
		EMU_BUCTRL_PWRRES = RES2	1000	1350	1700	Ω
		EMU_BUCTRL_PWRRES = RES3	525	815	1100	Ω
Output impedance between BU_VIN and BU_VOUT [2]	R_{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	35	110	185	Ω
		EMU_BUCTRL_VOUTRES = MED	475	775	1075	Ω
		EMU_BUCTRL_VOUTRES = WEAK	5600	6500	7400	Ω
Supply current	I_{BU_VIN}	BU_VIN not powering backup domain	—	11	TBD	nA
		BU_VIN powering backup domain[1]	—	550	TBD	nA

Note:

1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.
2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Open-loop gain	G_{OL}	DRIVESTRENGTH = 3	—	135	—	dB
		DRIVESTRENGTH = 2	—	137	—	dB
		DRIVESTRENGTH = 1	—	121	—	dB
		DRIVESTRENGTH = 0	—	109	—	dB
Loop unit-gain frequency[7]	UGF	DRIVESTRENGTH = 3, Buffer connection	—	3.38	—	MHz
		DRIVESTRENGTH = 2, Buffer connection	—	0.9	—	MHz
		DRIVESTRENGTH = 1, Buffer connection	—	132	—	kHz
		DRIVESTRENGTH = 0, Buffer connection	—	34	—	kHz
		DRIVESTRENGTH = 3, 3x Gain connection	—	2.57	—	MHz
		DRIVESTRENGTH = 2, 3x Gain connection	—	0.71	—	MHz
		DRIVESTRENGTH = 1, 3x Gain connection	—	113	—	kHz
		DRIVESTRENGTH = 0, 3x Gain connection	—	28	—	kHz
Phase margin	PM	DRIVESTRENGTH = 3, Buffer connection	—	67	—	°
		DRIVESTRENGTH = 2, Buffer connection	—	69	—	°
		DRIVESTRENGTH = 1, Buffer connection	—	63	—	°
		DRIVESTRENGTH = 0, Buffer connection	—	68	—	°
Output voltage noise	N_{OUT}	DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz	—	146	—	µVrms
		DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz	—	163	—	µVrms
		DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz	—	170	—	µVrms
		DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz	—	176	—	µVrms
		DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz	—	313	—	µVrms
		DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz	—	271	—	µVrms
		DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz	—	247	—	µVrms
		DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz	—	245	—	µVrms

SPI Slave Timing

Table 4.35. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		6 * $t_{HFPERCLK}$	—	—	ns
SCLK high time[1] [3] [2]	t_{SCLK_HI}		2.5 * $t_{HFPERCLK}$	—	—	ns
SCLK low time[1] [3] [2]	t_{SCLK_LO}		2.5 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1] [3]	$t_{CS\_ACT\_MI}$		24	—	69	ns
CS disable to MISO [1] [3]	$t_{CS\_DIS\_MI}$		19	—	175	ns
MOSI setup time [1] [3]	t_{SU_MO}		7	—	—	ns
MOSI hold time [1] [3] [2]	t_{H_MO}		6	—	—	ns
SCLK to MISO [1] [3] [2]	t_{SCLK_MI}		16 + 1.5 * $t_{HFPERCLK}$	—	43 + 2.5 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

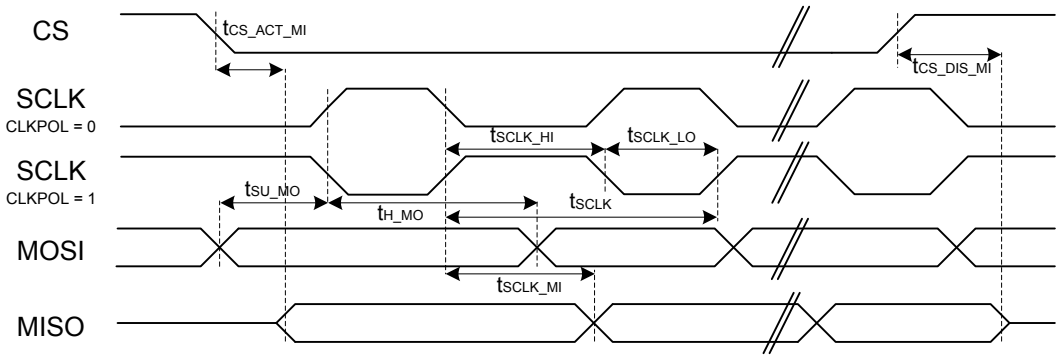

Figure 4.2. SPI Slave Timing Diagram

SDIO HS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Table 4.47. SDIO HS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	45	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	10.0	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	10.0	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.69	3.23	—	ns
Clock fall time	t_F		1.42	2.79	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}		0	—	13	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}		2	—	—	ns

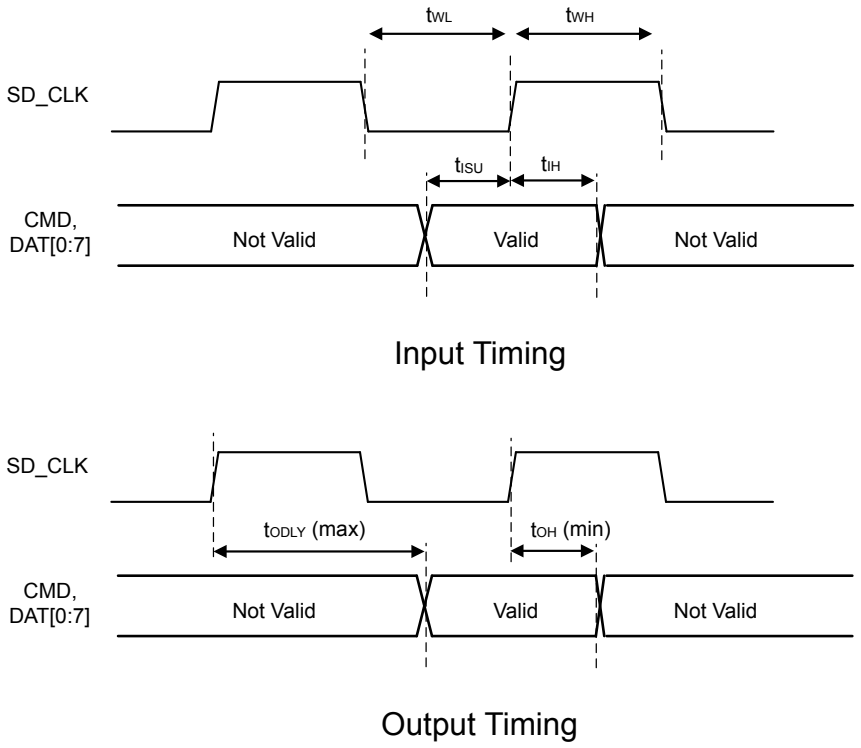

Figure 4.15. SDIO SDR Mode Timing

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	M2	GPIO	PB3	M3	GPIO
PC6	M14	GPIO	VREGVSS	M15 N16	Voltage regulator VSS
VREGSW	M16	DCDC regulator switching node	PB4	N1	GPIO
PB5	N2	GPIO	PB6	N3	GPIO
PD5	N14	GPIO	PD4	N15	GPIO
PC0	P1	GPIO (5V)	PC1	P2	GPIO (5V)
PC2	P3	GPIO (5V)	PA8	P4	GPIO
PA11	P5	GPIO	PA13	P6	GPIO (5V)
PB9	P7	GPIO (5V)	PB12	P8	GPIO
PH2	P9	GPIO (5V)	PH5	P10	GPIO
PH8	P11	GPIO (5V)	PH11	P12	GPIO (5V)
PH13	P13	GPIO (5V)	PD0	P14	GPIO (5V)
PD3	P15	GPIO	PD8	P16	GPIO
PB7	R1	GPIO	PC3	R2	GPIO (5V)
PC5	R3	GPIO	PA9	R4	GPIO
BODEN	R5	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	RESETn	R6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB10	R7	GPIO (5V)	PH0	R8	GPIO (5V)
PH3	R9	GPIO (5V)	PH6	R10	GPIO
PH9	R11	GPIO (5V)	PH12	R12	GPIO (5V)
PH14	R13	GPIO (5V)	PH15	R14	GPIO (5V)
PD2	R15	GPIO (5V)	PD7	R16	GPIO
PB8	T1	GPIO	PC4	T2	GPIO
PA7	T3	GPIO	PA10	T4	GPIO
PA12	T5	GPIO (5V)	PA14	T6	GPIO
PB11	T7	GPIO	PH1	T8	GPIO (5V)
PH4	T9	GPIO	PH7	T10	GPIO (5V)
PH10	T11	GPIO (5V)	PB13	T12	GPIO
PB14	T13	GPIO	AVDD	T14	Analog power supply.
PD1	T15	GPIO	PD6	T16	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF3	B9	GPIO
PF1	B10	GPIO (5V)	PF12	B11	GPIO
VBUS	B12	USB VBUS signal and auxiliary input to 5 V regulator.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 K12 L12 L13 M8 M11 N8	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L14	Digital IO power supply 0.
PF0	C10	GPIO (5V)	PE4	C11	GPIO
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PE5	D11	GPIO
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PE6	E11	GPIO
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE7	F11	GPIO
PC8	F12	GPIO (5V)	PC9	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE0	G11	GPIO (5V)
PE1	G12	GPIO (5V)	PE3	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
PC7	H13	GPIO	PD14	J1	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD15	J2	GPIO (5V)	PC6	J12	GPIO
DECOUPLE	J13	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC0	K1	GPIO (5V)
PC1	K2	GPIO (5V)	PD8	K13	GPIO
PC2	L1	GPIO (5V)	PC3	L2	GPIO (5V)
PA7	L3	GPIO	PB9	L15	GPIO (5V)
PB10	L16	GPIO (5V)	PD0	L17	GPIO (5V)
PD1	L18	GPIO	PD4	L19	GPIO
PD7	L20	GPIO	PB7	M1	GPIO
PC4	M2	GPIO	PA8	M3	GPIO
PA10	M4	GPIO	PA13	M5	GPIO (5V)
PA14	M6	GPIO	RESETn	M7	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	M9 M10 N11	Analog power supply.	PD3	M12	GPIO
PD6	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	PB12	N7	GPIO
PB13	N9	GPIO	PB14	N10	GPIO
PD2	N12	GPIO (5V)	PD5	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.11 EFM32GG11B3xx in QFP100 Device Pinout

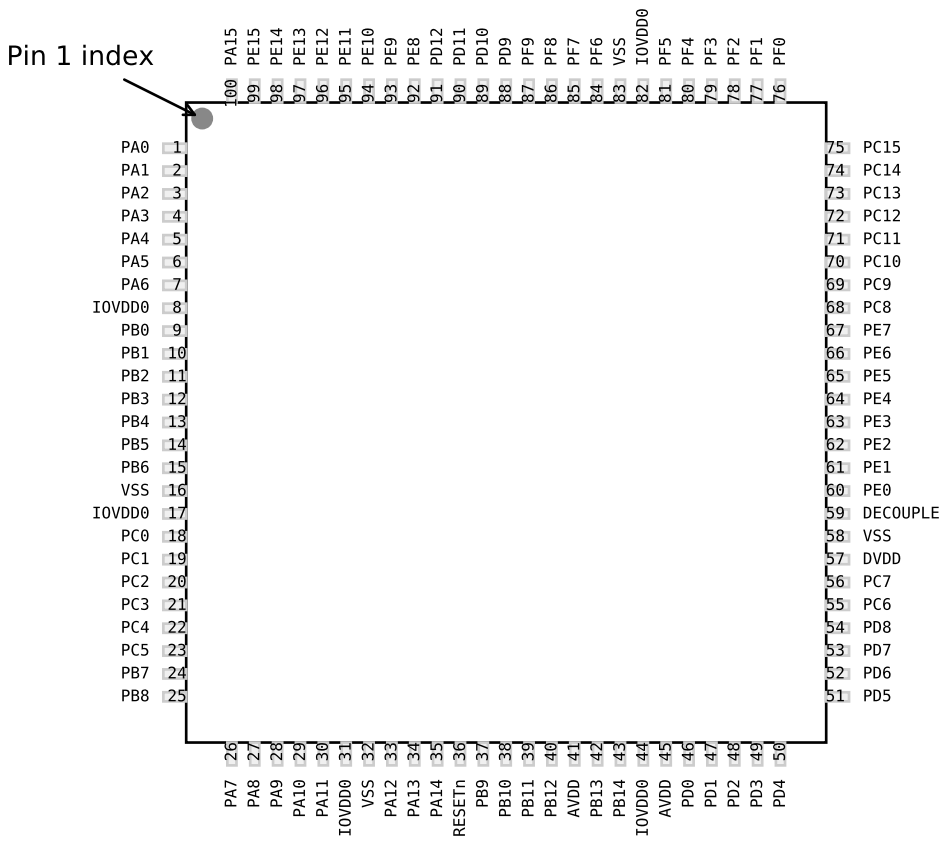

Figure 5.11. EFM32GG11B3xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.11. EFM32GG11B3xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF7	BUSCY BUSDX LCD_SEG25	EBI_BL1 #0 EBI_BL1 #4 EBI_BL1 #5 EBI_DCLK #1	TIM0_CC1 #1 TIM4_CC1 #4	ETH_RMIITXD0 #1 US2_RX #4 QSPI0_CS0 #0 ETH_MIIRXER #2 US1_RX #3 U0_RX #0	PRS_CH23 #2
PF6	BUSDY BUSCX LCD_SEG24	EBI_BL0 #0 EBI_BL0 #4 EBI_BL0 #5 EBI_CSTFT #1	TIM0_CC0 #1 TIM4_CC0 #4 WTIM3_CC2 #5	ETH_RMIITXD1 #1 US2_TX #4 QSPI0_SCLK #0 US1_TX #3 U0_TX #0	PRS_CH22 #2
PI11				US4_RTS #3	
PI8		EBI_A13 #2	TIM1_CC2 #7 TIM4_CC0 #3	US4_CLK #3	
PF5	BUSCY BUSDX LCD_SEG3	EBI_REn #0 EBI_REn #5 EBI_A27 #1	TIM0_CDTI2 #2 TIM1_CC3 #6 TIM4_CC0 #2	US2_CS #5 I2C2_SCL #0 USB_VBUSEN	PRS_CH2 #1 DBG_TDI
PF13	BUSCY BUSDX		TIM1_CC0 #6 TIM4_CC0 #1 TIM5_CC1 #7 WTIM3_CC0 #7	US5_CLK #2 I2C2_SDA #4	
PF3	BUSCY BUSDX LCD_SEG1	EBI_ALE #0	TIM4_CC0 #0 TIM0_CDTI0 #2 TIM1_CC1 #5	CAN1_TX #1 US1_CTS #2 I2C2_SCL #5	CMU_CLK1 #4 PRS_CH0 #1 ETM_TD3 #1
PF2	BUSDY BUSCX LCD_SEG0	EBI_ARDY #0 EBI_A26 #1	TIM0_CC2 #4 TIM1_CC0 #5 TIM2_CC0 #3	US2_CLK #5 CAN0_TX #1 US1_TX #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO DBG_SWO #0 GPIO_EM4WU4
PF1	BUSCY BUSDX	EBI_A25 #1	TIM0_CC1 #4 WTIM0_CC2 #4 LE-TIM0_OUT1 #2	US2_RX #5 CAN1_RX #1 US1_CS #2 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PA1	BUSAY BUSBX LCD_SEG14	EBI_AD10 #0 EBI_DCLK #3	TIM0_CC0 #7 TIM0_CC1 #0 TIM3_CC1 #4 PCNT0_S1IN #4	ETH_RMIIRXD1 #0 ETH_MIITXD3 #0 SDIO_DAT1 #1 US3_RX #0 QSPI0_CS1 #1 I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
PD12	LCD_SEG31	EBI_CS3 #0	TIM4_CC1 #6	ETH_RMIIRXER #1 SDIO_DAT4 #0 QSPI0_DQ3 #0 ETH_MIIRXCLK #2 US4_CS #1	
PD14		EBI_NANDWEn #1	TIM2_CDTI1 #1 TIM3_CC2 #6 WTIM0_CC2 #1	ETH_MDC #1 CAN0_RX #5 US4_RTS #1 US5_CS #1 I2C0_SDA #3	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PB0	BUSBY BUSAX LCD_SEG32	EBI_AD00 #1 EBI_CS0 #3 EBI_A16 #0	TIM2_CDTI0 #0 TIM1_CC0 #2 TIM3_CC2 #7 WTIM0_CC0 #5 PCNT0_S0IN #5 PCNT1_S1IN #2	LEU1_TX #3	PRS_CH4 #1 ACMP0_O #5
PE0	BUSDY BUSCX	EBI_A00 #2 EBI_A07 #0	TIM3_CC0 #1 WTIM1_CC1 #3 PCNT0_S0IN #1	CAN0_RX #6 U0_TX #1 I2C1_SDA #2	PRS_CH22 #1 ACMP2_O #1
PC7	BUSACMP0Y BUSACMP0X OPA3_N	EBI_A06 #0 EBI_A13 #1 EBI_A21 #3	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 LEU1_RX #0 I2C0_SCL #2	LES_CH7 PRS_CH15 #1 ETM_TD0 #2
PB1	BUSAY BUSBX LCD_SEG33	EBI_AD01 #1 EBI_CS1 #3 EBI_A17 #0	TIM2_CDTI1 #0 TIM1_CC1 #2 WTIM0_CC1 #5 LE-TIM1_OUT1 #5 PCNT0_S1IN #5	ETH_MIICRS #0 US5_RX #2 LEU1_RX #3	PRS_CH5 #1
PB2	BUSBY BUSAX LCD_SEG34	EBI_AD02 #1 EBI_CS2 #3 EBI_A18 #0	TIM2_CDTI2 #0 TIM1_CC2 #2 WTIM0_CC2 #5 LE-TIM1_OUT0 #5	ETH_MIICOL #0 US1_CS #6	PRS_CH18 #0 ACMP0_O #6
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	EBI_AD03 #1 EBI_CS3 #3 EBI_A19 #0	TIM1_CC3 #2 WTIM0_CC0 #6 PCNT1_S0IN #1	ETH_MIICRS #2 ETH_MDIO #0 SDIO_DAT6 #1 US2_TX #1 US3_TX #2 QSPI0_DQ4 #1	PRS_CH19 #0 ACMP0_O #7
PC6	BUSACMP0Y BUSACMP0X OPA3_P	EBI_A05 #0	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 LEU1_TX #0 I2C0_SDA #2	LES_CH6 PRS_CH14 #1 ETM_TCLK #2
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	EBI_AD04 #1 EBI_ARDY #3 EBI_A20 #0	WTIM0_CC1 #6 PCNT1_S1IN #1	ETH_MIICOL #2 ETH_MDC #0 SDIO_DAT7 #1 US2_RX #1 QSPI0_DQ5 #1 LEU1_TX #4	PRS_CH20 #0
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	EBI_AD05 #1 EBI_ALE #3 EBI_A21 #0	WTIM0_CC2 #6 LE-TIM1_OUT0 #4 PCNT0_S0IN #6	ETH_TSUEXTCLK #0 US0_RTS #4 US2_CLK #1 QSPI0_DQ6 #1 LEU1_RX #4	PRS_CH21 #0
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	EBI_AD06 #1 EBI_WEn #3 EBI_A22 #0	TIM0_CC0 #3 TIM2_CC0 #4 WTIM3_CC0 #6 LE-TIM1_OUT1 #4 PCNT0_S1IN #6	ETH_TSUTMRTOG #0 US0_CTS #4 US2_CS #1 QSPI0_DQ7 #1	PRS_CH12 #1
PD5	BUSADC0Y BUSADC0X OPA2_OUT	EBI_A09 #1 EBI_A18 #3	TIM6_CC1 #7 WTIM0_CDTI1 #4 WTIM1_CC3 #1 WTIM2_CC2 #5	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3	PRS_CH11 #2 ETM_TD3 #0 ETM_TD3 #2

5.21 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 5.20 GPIO Functionality Table for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.21. Alternate Functionality Overview

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ACMP0_O	0: PE13 1: PE2 2: PD6 3: PB11	4: PA6 5: PB0 6: PB2 7: PB3	Analog comparator ACMP0, digital output.
ACMP1_O	0: PF2 1: PE3 2: PD7 3: PA12	4: PA14 5: PB9 6: PB10 7: PA5	Analog comparator ACMP1, digital output.
ACMP2_O	0: PD8 1: PE0 2: PE1 3: PI0	4: PI1 5: PI2	Analog comparator ACMP2, digital output.
ACMP3_O	0: PF0 1: PC15 2: PC14 3: PC13	4: PI4 5: PI5	Analog comparator ACMP3, digital output.
ADC0_EXTN	0: PD7		Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PD6		Analog to digital converter ADC0 external reference input positive pin.
ADC1_EXTN	0: PD7		Analog to digital converter ADC1 external reference input negative pin.
ADC1_EXTP	0: PD6		Analog to digital converter ADC1 external reference input positive pin.
BOOT_RX	0: PF1		Bootloader RX.
BOOT_TX	0: PF0		Bootloader TX.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
BU_STAT	0: PE3		Backup Power Domain status, whether or not the system is in backup mode.
BU_VIN	0: PD8		Battery input for Backup Power Domain.
BU_VOUT	0: PE2		Power output for Backup Power Domain.
CAN0_RX	0: PC0 1: PF0 2: PD0 3: PB9	4: PG8 5: PD14 6: PE0 7: PI12	CAN0 RX.
CAN0_TX	0: PC1 1: PF2 2: PD1 3: PB10	4: PG9 5: PD15 6: PE1 7: PI13	CAN0 TX.
CAN1_RX	0: PC2 1: PF1 2: PD3 3: PC9	4: PC12 5: PA12 6: PG10 7: PI14	CAN1 RX.
CAN1_TX	0: PC3 1: PF3 2: PD4 3: PC10	4: PC11 5: PA13 6: PG11 7: PI15	CAN1 TX.
CMU_CLK0	0: PA2 1: PC12 2: PD7 3: PG2	4: PF2 5: PA12	Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA1 1: PD8 2: PE12 3: PG1	4: PF3 5: PB11	Clock Management Unit, clock output number 1.
CMU_CLK2	0: PA0 1: PA3 2: PD6 3: PG0	4: PA3 5: PD10	Clock Management Unit, clock output number 2.
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	4: PE1 5: PD10 6: PE12 7: PB11	Clock Management Unit, clock input number 0.
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A23	0: PC0 1: PC11 2: PH11 3: PE5		External Bus Interface (EBI) address output pin 23.
EBI_A24	0: PC1 1: PF0 2: PH12 3: PE6		External Bus Interface (EBI) address output pin 24.
EBI_A25	0: PC2 1: PF1 2: PH13 3: PE7		External Bus Interface (EBI) address output pin 25.
EBI_A26	0: PC4 1: PF2 2: PH14 3: PC8		External Bus Interface (EBI) address output pin 26.
EBI_A27	0: PD2 1: PF5 2: PH15 3: PC9		External Bus Interface (EBI) address output pin 27.
EBI_AD00	0: PE8 1: PB0 2: PG0		External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	0: PE9 1: PB1 2: PG1		External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	0: PE10 1: PB2 2: PG2		External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	0: PE11 1: PB3 2: PG3		External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	0: PE12 1: PB4 2: PG4		External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	0: PE13 1: PB5 2: PG5		External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	0: PE14 1: PB6 2: PG6		External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	0: PE15 1: PC0 2: PG7		External Bus Interface (EBI) address and data input / output pin 07.

6. BGA192 Package Specifications

6.1 BGA192 Package Dimensions

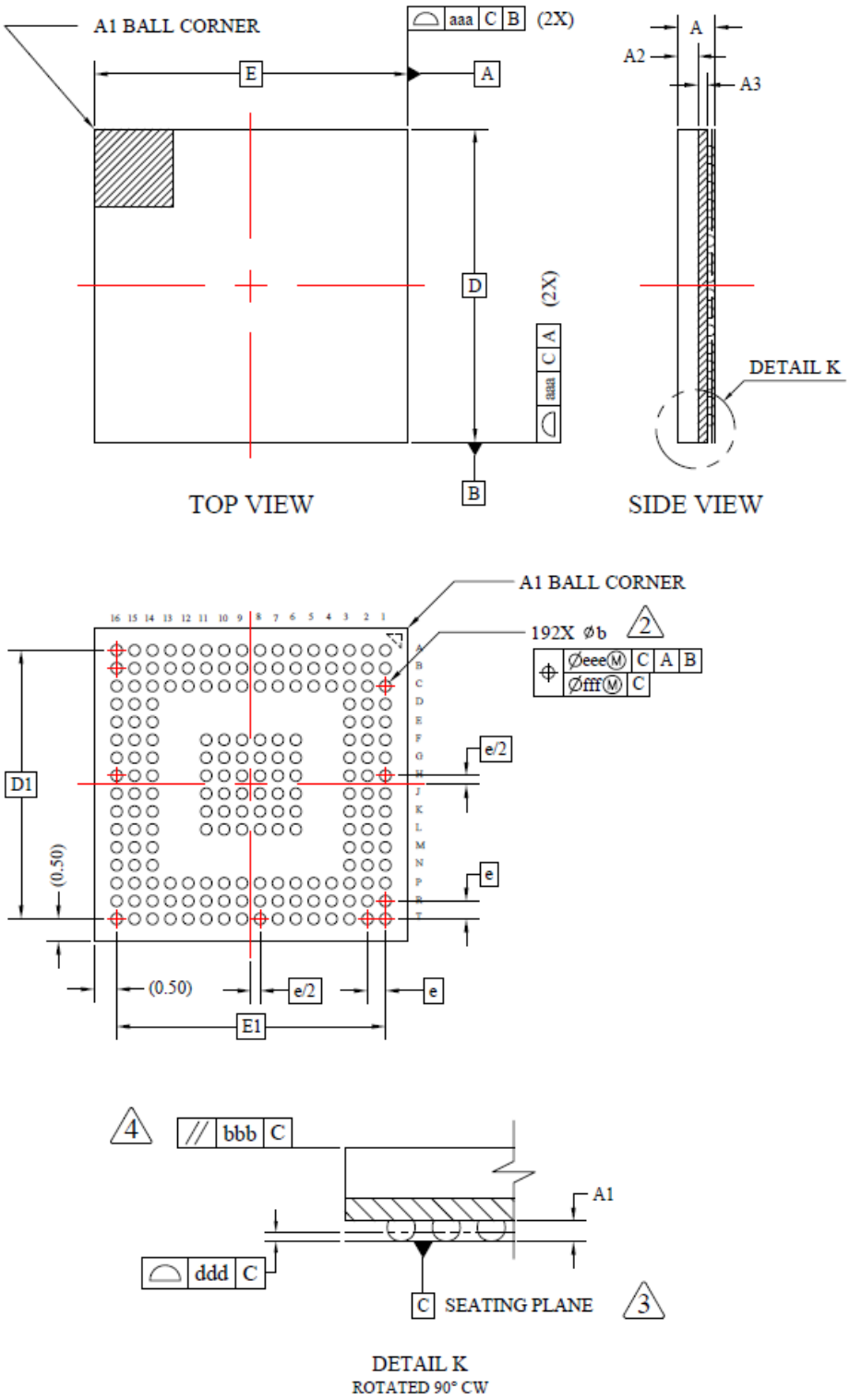

Figure 6.1. BGA192 Package Drawing

Table 9.1. BGA112 Package Dimensions

Dimension	Min	Typ	Max
A	-	-	1.30
A1	0.55	0.60	0.65
A2		0.21 BSC	
A3	0.30	0.35	0.40
d	0.43	0.48	0.53
D		10.00 BSC	
D1		8.00 BSC	
E		10.00 BSC	
E1		8.00 BSC	
e1		0.80 BSC	
e2		0.80 BSC	
L1		1.00 REF	
L2		1.00 REF	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. TQFP100 Package Specifications

10.1 TQFP100 Package Dimensions

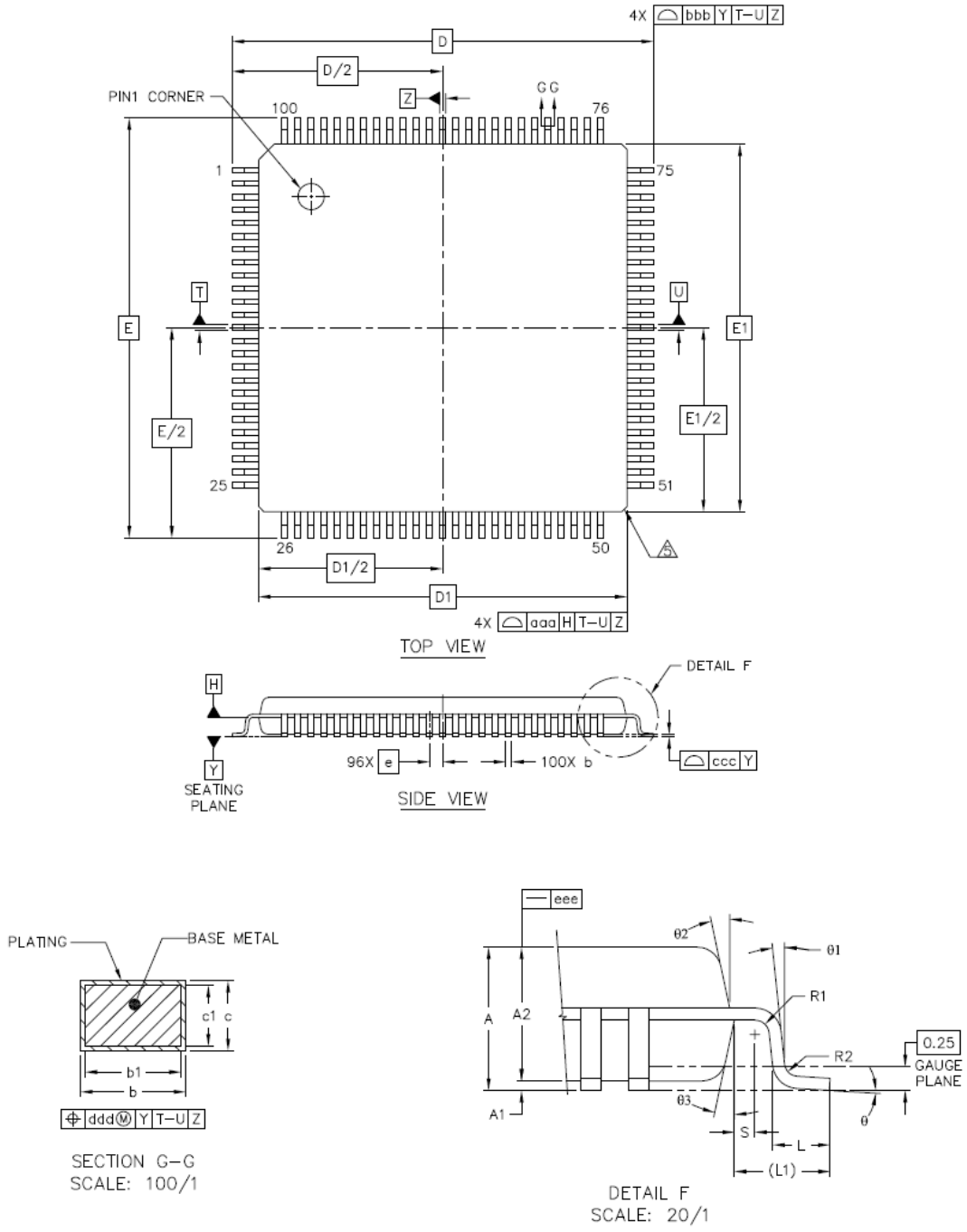

Figure 10.1. TQFP100 Package Drawing

Table 12.1. QFN64 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.203 REF		
D	9.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.