

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	144
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	192-VFBGA
Supplier Device Package	192-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024gl192-a

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

5.	Pin Definitions	115
	5.1 EFM32GG11B8xx in BGA192 Device Pinout	.115
	5.2 EFM32GG11B8xx in BGA152 Device Pinout	.119
	5.3 EFM32GG11B8xx in BGA120 Device Pinout	.123
	5.4 EFM32GG11B5xx in BGA120 Device Pinout	.126
	5.5 EFM32GG11B4xx in BGA120 Device Pinout	129
	5.6 EFM32GG11B4xx in BGA112 Device Pinout	.132
	5.7 EFM32GG11B3xx in BGA112 Device Pinout	.135
	5.8 EFM32GG11B8xx in QFP100 Device Pinout	138
	5.9 EFM32GG11B5xx in QFP100 Device Pinout	141
	5.10 EFM32GG11B4xx in QFP100 Device Pinout	144
	5.11 EFM32GG11B3xx in QFP100 Device Pinout	147
	5.12 EFM32GG11B8xx in QFP64 Device Pinout	150
	5.13 EFM32GG11B5xx in QFP64 Device Pinout	152
	5.14 EFM32GG11B4xx in QFP64 Device Pinout	154
	5.15 EFM32GG11B1xx in QFP64 Device Pinout	156
	5.16 EFM32GG11B8xx in QFN64 Device Pinout	158
	5.17 EFM32GG11B5xx in QFN64 Device Pinout	.160
	5.18 EFM32GG11B4xx in QFN64 Device Pinout	.162
	5.19 EFM32GG11B1xx in QFN64 Device Pinout	164
	5.20 GPIO Functionality Table	166
	5.21 Alternate Functionality Overview	178
	5.22 Analog Port (APORT) Client Maps	211
6.	BGA192 Package Specifications	224
	6.1 BGA192 Package Dimensions	.224
	6.2 BGA192 PCB Land Pattern	226
	6.3 BGA192 Package Marking	228
7.	BGA152 Package Specifications	229
	7.1 BGA152 Package Dimensions	.229
	7.2 BGA152 PCB Land Pattern	231
	7.3 BGA152 Package Marking	233
8.	BGA120 Package Specifications	234
	8.1 BGA120 Package Dimensions	.234
	8.2 BGA120 PCB Land Pattern	236
	8.3 BGA120 Package Marking	238
9.	BGA112 Package Specifications	239
	9.1 BGA112 Package Dimensions	.239

3. System Overview

3.1 Introduction

The Giant Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Giant Gecko Series 1 Reference Manual.

A block diagram of the Giant Gecko Series 1 family is shown in Figure 3.1 Detailed EFM32GG11 Block Diagram on page 11. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.



Figure 3.1. Detailed EFM32GG11 Block Diagram

3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I²S

3.6.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter is a subset of the USART module, supporting full duplex asynchronous UART communication with hardware flow control and RS-485.

3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.4 Inter-Integrated Circuit Interface (I²C)

The I²C module provides an interface between the MCU and a serial I²C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I²C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.6.5 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices. The interface is memory mapped into the address bus of the Cortex-M4. This enables seamless access from software without manually manipulating the I/O settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface to external devices. Timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

The EBI contains a TFT controller which can drive a TFT via an RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

4.1.6 Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Backup supply voltage range	V _{BU_VIN}		1.8	_	3.8	V
PWRRES resistor	R _{PWRRES}	EMU_BUCTRL_PWRRES = RES0	3400	3900	4400	Ω
		EMU_BUCTRL_PWRRES = RES1	1450	1800	2150	Ω
		EMU_BUCTRL_PWRRES = RES2	1000	1350	1700	Ω
		EMU_BUCTRL_PWRRES = RES3	525	815	1100	Ω
Output impedance between BU_VIN and BU_VOUT ²	R _{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	35	110	185	Ω
		EMU_BUCTRL_VOUTRES = MED	475	775	1075	Ω
		EMU_BUCTRL_VOUTRES = WEAK	5600	6500	7400	Ω
Supply current	I _{BU_VIN}	BU_VIN not powering backup do- main	—	11	TBD	nA
		BU_VIN powering backup do- main ¹	_	550	TBD	nA

Table 4.6. Backup Supply Domain

Note:

1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.

2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

4.1.19 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes^{8 1}.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Supply voltage (from AVDD)	V _{OPA}	HCMDIS = 0, Rail-to-rail input range	2	—	3.8	V
		HCMDIS = 1	1.62	_	3.8	V
Input voltage	V _{IN}	HCMDIS = 0, Rail-to-rail input range	V _{VSS}	—	V _{OPA}	V
		HCMDIS = 1	V _{VSS}	_	V _{OPA} -1.2	V
Input impedance	R _{IN}		100	_	—	MΩ
Output voltage	V _{OUT}		V _{VSS}	_	V _{OPA}	V
Load capacitance ²	C _{LOAD}	OUTSCALE = 0	_	—	75	pF
		OUTSCALE = 1	_	_	37.5	pF
Output impedance	R _{OUT}	$\label{eq:VOUT} \begin{array}{l} DRIVESTRENGTH = 2 \text{ or } 3, 0.4 \text{ V} \\ \leq V_{OUT} \leq V_{OPA} \text{ - } 0.4 \text{ V}, \text{ -8 mA } < \\ I_{OUT} < 8 \text{ mA}, \text{ Buffer connection}, \\ \text{Full supply range} \end{array}$	_	0.25		Ω
		$ DRIVESTRENGTH = 0 \text{ or } 1, 0.4 \text{ V} \\ \leq \text{V}_{\text{OUT}} \leq \text{V}_{\text{OPA}} - 0.4 \text{ V}, -400 \mu\text{A} < \\ \text{I}_{\text{OUT}} < 400 \mu\text{A}, \text{Buffer connection,} \\ \text{Full supply range} $	_	0.6	_	Ω
		$\label{eq:DRIVESTRENGTH} \begin{array}{l} DRIVESTRENGTH = 2 \mbox{ or } 3, \mbox{ 0.1 V} \\ \leq V_{OUT} \leq V_{OPA} - 0.1 \mbox{ V}, \mbox{ -2 mA} < \\ I_{OUT} < 2 \mbox{ mA}, \mbox{ Buffer connection}, \\ \mbox{ Full supply range} \end{array}$		0.4	_	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V $\leq V_{OUT} \leq V_{OPA} - 0.1 V$, -100 µA < $I_{OUT} < 100 µA$, Buffer connection, Full supply range	_	1	_	Ω
Internal closed-loop gain	G _{CL}	Buffer connection	TBD	1	TBD	-
		3x Gain connection	TBD	2.99	TBD	-
		16x Gain connection	TBD	15.7	TBD	-
Active current ⁴	I _{OPA}	DRIVESTRENGTH = 3, OUT- SCALE = 0	—	580	_	μA
		DRIVESTRENGTH = 2, OUT- SCALE = 0	_	176	_	μA
		DRIVESTRENGTH = 1, OUT- SCALE = 0	—	13	_	μA
		DRIVESTRENGTH = 0, OUT- SCALE = 0	_	4.7	_	μA

Table 4.27. Operational Amplifier (OPAMP)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Open-loop gain	G _{OL}	DRIVESTRENGTH = 3		135		dB
		DRIVESTRENGTH = 2	_	137	_	dB
		DRIVESTRENGTH = 1		121		dB
		DRIVESTRENGTH = 0		109		dB
Loop unit-gain frequency ⁷	UGF	DRIVESTRENGTH = 3, Buffer connection		3.38	_	MHz
		DRIVESTRENGTH = 2, Buffer connection	_	0.9	_	MHz
		DRIVESTRENGTH = 1, Buffer connection		132	_	kHz
		DRIVESTRENGTH = 0, Buffer connection		34	_	kHz
		DRIVESTRENGTH = 3, 3x Gain connection		2.57		MHz
		DRIVESTRENGTH = 2, 3x Gain connection	_	0.71	_	MHz
		DRIVESTRENGTH = 1, 3x Gain connection		113	_	kHz
		DRIVESTRENGTH = 0, 3x Gain connection		28	_	kHz
Phase margin	РМ	DRIVESTRENGTH = 3, Buffer connection	_	67	_	0
		DRIVESTRENGTH = 2, Buffer connection	_	69	_	o
		DRIVESTRENGTH = 1, Buffer connection	_	63	_	o
		DRIVESTRENGTH = 0, Buffer connection	_	68	_	o
Output voltage noise	N _{OUT}	DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz	—	146	_	µVrms
		DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz	—	163	_	µVrms
		DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz	—	170	—	µVrms
		DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz	_	176		µVrms
		DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz	—	313	_	µVrms
		DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz	—	271	—	µVrms
		DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz	_	247	_	µVrms
		DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz		245		µVrms

Parameter	Symbol	Test Condition	Min	Min Typ		Unit
Note:	·		·	•		
1. Specified configuratio V. Nominal voltage ga	n for 3X-Gain con iin is 3.	figuration is: INCBW = 1, HCM	/IDIS = 1, RESINSEL =	VSS, V _{INPUT} =	= 0.5 V, V _{OUT}	_{PUT} = 1.5
2. If the maximum C _{LOA}	_D is exceeded, an	isolation resistor is required for	or stability. See AN0038	3 for more infor	mation.	
3. When INCBW is set to or the OPAMP may n	o 1 the OPAMP ba ot be stable.	andwidth is increased. This is	allowed only when the r	non-inverting c	lose-loop gai	n is ≥ 3,
4. Current into the load drive the resistor feed another ~10 μA curre	esistor is exclude back network. The nt when the OPAN	d. When the OPAMP is conne e internal resistor feedback ne /IP drives 1.5 V between outp	ected with closed-loop g twork has total resistan ut and ground.	ain > 1, there v ce of 143.5 kC	will be extra c 0hm, which wi	urrent to Il cause
5. Step between 0.2V ar	nd V _{OPA} -0.2V, 10%	%-90% rising/falling range.				
6. From enable to outpu	t settled. In sample	e-and-off mode, RC network a	after OPAMP will contrib	oute extra dela	y. Settling err	or < 1mV.
7. In unit gain connectio product of the OPAMI	n, UGF is the gain P and 1/3 attenuat	l-bandwidth product of the OP tion of the feedback network.	AMP. In 3x Gain conne	ction, UGF is t	he gain-band	width
8. Specified configuratio V _{OUTPUT} = 0.5 V.	n for Unit gain buf	fer configuration is: INCBW =	0, HCMDIS = 0, RESIN	ISEL = DISAB	LE. V _{INPUT} =	0.5 V,
9. When HCMDIS=1 and and CMRR specificati	d input common m	node transitions the region from to this transition region.	m V _{OPA} -1.4V to V _{OPA} -1	V, input offset	will change. F	PSRR

4.1.20 LCD Driver

Table 4.28. LCD Driver

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Frame rate	f _{LCDFR}		TBD	_	TBD	Hz
LCD supply range ²	V _{LCDIN}		1.8		3.8	V
LCD output voltage range	V _{LCD}	Current source mode, No external LCD capacitor	2.0	_	V _{LCDIN} -0.4	V
		Step-down mode with external LCD capacitor	2.0	—	V _{LCDIN}	V
		Charge pump mode with external LCD capacitor	2.0	—	1.9 * V _{LCDIN}	V
Contrast control step size	STEP _{CONTRAST}	Current source mode	_	64	—	mV
		Charge pump or Step-down mode		43	—	mV
Contrast control step accura- cy ¹	ACC _{CONTRAST}		—	+/-4	_	%

Note:

1. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation.

2. V_{LCDIN} is selectable between the AVDD or DVDD supply pins, depending on EMU_PWRCTRL_ANASW.

EBI Ready/Wait Timing Requirements

Timing applies to both EBI_REn and EBI_WEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.41.	EBI Ready/Wait	Timing	Requirements
-------------	----------------	--------	--------------

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge	tsu_ardy	IOVDD ≥ 1.62 V	55 + (3 * t _{HFCOR-} _{ECLK})	_	_	ns
		IOVDD ≥ 3.0 V	36 + (3 * t _{HFCOR-} _{ECLK})	_	_	ns
Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid	th_ardy	IOVDD ≥ 1.62 V	-9	_	_	ns



Figure 4.8. EBI Ready/Wait Timing Requirements

SDIO MMC SDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Clock frequency during data transfer	F _{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	_	_	25	MHz
		Using HFXO	_		TBD	MHz
Clock low time	t _{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t _{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	18.1	_	—	ns
		Using HFXO	TBD	_	—	ns
Clock rise time	t _R		1.96	8.27	—	ns
Clock fall time	t _F		1.67	6.90	_	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	t _{ISU}		5.3		_	ns
Input hold time, SD_CLK to CMD, DAT[0:7] change	t _{IH}		2.5		_	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	todly		0	—	16	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	t _{OH}		3	_	_	ns

Table 4.50. SDIO MMC SDR Mode Timing (Location 0, 1.8V I/O)

5. Pin Definitions

5.1 EFM32GG11B8xx in BGA192 Device Pinout

Pin A1 index	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	لا	<u>رمج</u>		(1) ³	ar th	(T)	(1)	F9	~F8	<u>(19</u>	510	(A)	(N)5	(T)	619	FO)
4	PAN	PEr C	PE-	PEr	PEN	PEN	pt.	60.	60	62.	62	Pr.	100	Pr 2	Pr.	90 0
В	PAU	6017	6070	600	pry	64g	PEI	640	\$IT	628	662	PET3	643	PEL	6EJ	VREGO
С	49	6013	P014	6013	P113	PI14	PI13	PI13	P170	6IJ	pF13	PET3	PFA	673	PC14	VREGI
D	(TAG)	600	P015											PC13	C12	PC77
E	EA9	602	6CJ											¢C70	609	623
F	PAG	PGA	PG3			TONDOS	IOND)	55	MC.	TONDOG	TONDE)		619	p14	P13
G	PAS	609	PG5			TONDE	TONDI	(JS)	159.	TONDOG	TONDE)		623	617	610
н	049	608	PGT			159	159	(55)	(15 ⁵)	(15 ⁵)	(15 ⁵)			PES	PEG	PET
J	617	PG10	PG9			455	(5 ⁵)	(15 ⁵)	159	(15 ⁵)	159			PE3	PEA C	ECOUPLE
к	PG14	PG13	PG12			TONDO	TONDE	159	(5°).	TONDE	TONDE)		PEL	PE2	DADD
L	PG13	PB15	PB0			TONDE	TONDE	159	(5°).	TONDE	TONDE)		PEO	60)	REGUDD
М	PB ¹	682	PB3											60	REGVS	VREGSW
Ν	PBA	PB5	680											609	P04	REGUSS
Ρ	609	PC3	602	849	PAI	PA13	PB9	PB12	PH2	PHS	PH8	eH1]	PH13	009	603	809
R	681	PC3	609	649	BODEN	RESET	B19	PH0	pH3	646	PH9	PHIZ	PH14	PH15	602	109
т	PB8	PCA	(TAG)	PA10	PAIZ	PALA	B 1	PHI	PHA	(PHT)	PH10	PB13	p814	AVOD	607	009

Figure 5.1. EFM32GG11B8xx in BGA192 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA15	A1	GPIO	PE15	A2	GPIO
PE14	A3	GPIO	PE13	A4	GPIO
PE12	A5	GPIO	PE11	A6	GPIO
PE10	A7	GPIO	PE9	A8	GPIO
PE8	A9	GPIO	PI9	A10	GPIO (5V)
PI6	A11	GPIO (5V)	PF14	A12	GPIO (5V)

PB2M3GPIOPB3M3GPIOPC6M1GPIOVRECVSM1value regulator VSSVREGWM4DCO regulator switching nodePB4N1GPIOPB5M2GPIOPD4M3GPIOPD5M1GPIOPD4M2GPIOPC0P1GPIO(SV)PA6P2GPIO(SV)PH1P5GPIO(SV)PH2P4GPIOPH2P1GPIO(SV)PH1P12GPIOPH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P14GPIO(SV)PH3P1GPIO(SV)PH1P14GPIO(SV)PH3P3GPIO(SV)PH1P14GPIO(SV)PH3P3GPIO(SV)PH1P14GPIO(SV)PH3P3GPIO(SV)PH2R2GPIO(SV)PH3P3GPIO(SV)PH3R4GPIO(SV)PH4S1GPIO(SV)GPICR2GPIO(SV)PS0R3GPIO(SV)GPISR4GPIO(SV)PS0R4GPIO(SV)GPISR4 <td< th=""><th>Pin Name</th><th>Pin(s)</th><th>Description</th><th>Pin Name</th><th>Pin(s)</th><th>Description</th></td<>	Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC6M14GPI0VREGVSM15Voltage regulator VSSVREGSWM16DCDC regulator switching nodePP84N1GPI0PB65N2GPI0PP80N3GPI0PD55N14GPI0PP10PP2GPI0PC0P1GPI0PP10PP2GPI0PC1P3GPI0PP10PP2GPI0PC2P3GPI0GPI0PP3GPI0PC1P4GPI0GPI0PP3GPI0PC2P3GPI0GPI0PP41GPI0PC3P3GPI0GPI0PP3GPI0PH3P16GPI0PP30PP3GPI0PH3P17GPI0GPI0PP40GPI0PH3P13GPI0PP10P11GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30R2GPI0PH3P13GPI0PP30R4GPI0PH5R3GPI0PP40R18GPI0PH5R4GPI0PP40R18GPI0PH4P13GPI0PP40R18GPI0PH4R19GPI0GP10PP40R10PH4R19GPI0GP10R14GPI0PH4R19GPI0GP10R14 <t< td=""><td>PB2</td><td>M2</td><td>GPIO</td><td>PB3</td><td>M3</td><td>GPIO</td></t<>	PB2	M2	GPIO	PB3	M3	GPIO
VREGSWM14DCD regulator switching nodePB4N1CPI0PB5N2GPI0PPB6N3GPI0PD5N14GPI0PD4N15GPI0PC0P3GPI0 (5V)PA1PA2GPI0PA1P5GPI0PA3P6GPI0PA1P5GPI0PA3P6GPI0P14P7GPI0 (5V)PH12P8GPI0P14P1GPI0 (5V)PH13P10GPI0 (5V)P14P1GPI0 (5V)PH14P12GPI0 (5V)P14P13GPI0 (5V)PH10P12GPI0 (5V)P143P13GPI0 (5V)PH10P14GPI0 (5V)P143P14GPI0 (5V)PH10P14GPI0 (5V)P143P15GPI0 (5V)PD0P14GPI0 (5V)P15GPI0 (5V)PD0P14GPI0 (5V)P16R1GPI0 (5V)GPI0 (5V)Restingut active low. To apply an extractive low. To apply an extractina	PC6	M14	GPIO	VREGVSS	M15 N16	Voltage regulator VSS
PB5N2GPIOPB6N3GPIOPD5N14GPIOPD4N15GPIOPC0P1GPIO (5V)PC1P2GPIO (5V)PC1P3GPIO (5V)PA8P4GPIO (5V)PB9P7GPIO (5V)PB12P8GPIO (5V)PH8P1GPIO (5V)PH10P12GPIO (5V)PH3P13GPIO (5V)PD0PH10P12GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3SP15GPIO (5V)PD0P14GPIO (5V)PD3P15GPIO (5V)PD0P14GPIO (5V)PD4N14GPIO (5V)PD1PA9R4PD5R3GPIO (5V)FPA9R4GPIO (5V)PD5R3GPIO (5V)PH4R4GPIO (5V)PH4R4GPIO (5V)PH4R14GPIO (5V)PH4R14GPIO (5V)PH10R14GPIO (5V)PH4R14GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH4R14GPIO (5V)PH4<	VREGSW	M16	DCDC regulator switching node	PB4	N1	GPIO
PD5N14GP0PD4N15GP10PC0P1GP10 (5V)PC1P2GP10 (5V)PC2P3GP10 (5V)PA8P4GP10 (5V)PB9P7GP10 (5V)PB12P8GP10 (5V)PH2P9GP10 (5V)PH11P12GP10 (5V)PH3P11GP10 (5V)PH11P12GP10 (5V)PH3P13GP10 (5V)PD0P14GP10 (5V)PH3P13GP10 (5V)PD0P14GP10 (5V)PH3P15GP10 (5V)PD0P14GP10 (5V)PB7R1GP10 (5V)PD0P14GP10 (5V)PB7R3GP10 - Controlled to failed to main extension may be of the single active tow. To apply an extend extension exten	PB5	N2	GPIO	PB6	N3	GPIO
PC0P1GPI0 (5V)PC1P2GPI0 (5V)PC2P3GPI0 (5V)PA8P4GPI0PA11P5GPI0 (5V)PA13P6GPI0 (5V)PB9P7GPI0 (5V)PB12P8GPI0 (5V)PH2P9GPI0 (5V)PH15P10GPI0 (5V)PH3P11GPI0 (5V)PH11P12GPI0 (5V)PH3P13GPI0 (5V)PH10P14GPI0 (5V)PH3P13GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0 (5V)PD0P14GPI0 (5V)PD3R1GPI0 (5V)PD3R2GPI0 (5V)PC5R3GPI0 (5V)PA9R4GPI0 (5V)PC5R3GPI0 (5V)PA9R4GPI0 (5V)BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to M20D.R68GPI0 (5V)PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH10R14GPI0 (5V)PH4R13GPI0 (5V)PH10R14GPI0 (5V)PH4R13GPI0 (5V)PH10R14GPI0 (5V)PH4R15GPI0 (5V)PA14T6GPI0PH4R13GPI0 (5V)PA14T6GPI0PH4R13GPI0 (5V)PA14T6GPI0 (5V)PH4T3GPI0 (5V) <td>PD5</td> <td>N14</td> <td>GPIO</td> <td>PD4</td> <td>N15</td> <td>GPIO</td>	PD5	N14	GPIO	PD4	N15	GPIO
PC2 P3 GPIO (5V) PA8 P4 GPIO PA11 P5 GPIO PA13 P6 GPIO (5V) PB9 P7 GPIO (5V) PB12 P8 GPIO PH2 P9 GPIO (5V) PH5 P10 GPIO PH3 P11 GPIO (5V) PH11 P12 GPIO (5V) PH3 P13 GPIO (5V) PD0 P14 GPIO (5V) PH3 P13 GPIO (5V) PD0 P14 GPIO (5V) PD3 P15 GPIO PD3 P15 GPIO (5V) PD3 P15 GPIO PC3 R2 GPIO (5V) PD5 R3 GPIO PA9 R4 GPIO BODEN R5 Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. RESETn R6 GPIO (5V) PB10 R7 GPIO (5V) PH0 R8 GPIO (5V) PH3 R9 GPIO (5V) PH1 R1 GPIO (PC0	P1	GPIO (5V)	PC1	P2	GPIO (5V)
PA11 P5 GPIO PA13 P6 GPIO (5V) PB9 P7 GPIO (5V) PB12 P8 GPIO PH2 P9 GPIO (5V) PH5 P10 GPIO PH8 P11 GPIO (5V) PH11 P12 GPIO (5V) PH3 P13 GPIO (5V) PD0 P14 GPIO (5V) PD3 P15 GPIO (5V) PD0 P14 GPIO (5V) PD3 P15 GPIO PD3 P15 GPIO PD4 PB7 R1 GPIO PC3 R2 GPIO (5V) PC5 R3 GPIO PA9 R4 GPIO BODEN R5 Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. RESETn R6 Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and left the internal pul-upensure that reset is released. PB10 R7 GPIO (5V) PH0 R8 GPIO (5V) PH3 R9 GPIO (5V) P	PC2	P3	GPIO (5V)	PA8	P4	GPIO
PB9P7GPIO (5V)PB12P8GPIOPH2P9GPIO (5V)PH5P10GPIOPH8P11GPIO (5V)PD11P12GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD2P23R2GPIO (5V)PB7R1GPIOPA9R4GPIOPC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin wyb be left disconnected or tied to AVDD.RESETNR6Reset input, active low. To apply an ex- terral reset source to this pin, it is re- arrest only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIOPH4R13GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PD7R16GPIOPH3T1GPIOPA10T4GPIOPH4T3GPIO (5V)PA14T6GPIOPH4T3GPIO (5V)PH11T8GPIO (5V)PH4T9GPIO (5V)PH1T10GPIOPH4T9GPIO (5V)PH7T10GPIOPH4T9GPIO (5V)PH3T12GPIOPH4T13GPIO (5V)PH3T12GPIOPH4T14GPIO (5V)PH3T14Anal	PA11	P5	GPIO	PA13	P6	GPIO (5V)
PH2P9GPI0 (5V)PH5P10GPI0PH8P11GPI0 (5V)PH11P12GPI0 (5V)PH3P13GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0PD0P14GPI0 (5V)PB7R1GPI0PC3R2GPI0 (5V)PC5R3GPI0PA9R4GPI0BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin out during reset, and let the internal pull-up ensure that reset is released.PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH6R10GPI0PH4R13GPI0 (5V)PH12R12GPI0 (5V)PH4R13GPI0 (5V)PH15R14GPI0 (5V)PH4R13GPI0 (5V)PD7R16GPI0PH3T1GPI0 (5V)PD7R16GPI0PH4T3GPI0 (5V)PA14T6GPI0PH4T3GPI0 (5V)PA14T6GPI0PH4T7GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T1GPI0 (5V)PB13T12GPI0PH4<	PB9	P7	GPIO (5V)	PB12	P8	GPIO
PH8P11GPIO (5V)PH11P12GPIO (5V)PH13P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD8P16GPIOPB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENRsBrown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETNR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and left the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIOPH4R13GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPA3T3GPIO (5V)PD7R16GPIOPH4T3GPIO (5V)PD7R16GPIOPH4T3GPIO (5V)PA14T6GPIOPH4T9GPIO (5V)PH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIOPH7 <t< td=""><td>PH2</td><td>P9</td><td>GPIO (5V)</td><td>PH5</td><td>P10</td><td>GPIO</td></t<>	PH2	P9	GPIO (5V)	PH5	P10	GPIO
PH13P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD8P16GPIOPB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPA7T3GPIO (5V)PA14T6GPIOPA12T5GPIO (5V)PA14T6GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH3T12GPIOPH4T9GPIO (5V)PH3T12GPIOPH4T13GPIOAVDDT14Analog power supply.PH4T15GPIO <td>PH8</td> <td>P11</td> <td>GPIO (5V)</td> <td>PH11</td> <td>P12</td> <td>GPIO (5V)</td>	PH8	P11	GPIO (5V)	PH11	P12	GPIO (5V)
PD3P15GPI0PD8P16GPI0PB7R1GPI0PC3R2GPI0 (5V)PC5R3GPI0PA9R4GPI0BC5R3GPI0PA9R4GPI0BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnReset input, active low. To apply an ex- ternal reset source to this pin, it is re- quied to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH6R10GPI0PH3R9GPI0 (5V)PH6R10GPI0 (5V)PH3R1GPI0 (5V)PH12R12GPI0 (5V)PH4R13GPI0 (5V)PH15R14GPI0 (5V)PD2R15GPI0 (5V)PD7R16GPI0PB8T1GPI0PA10T4GPI0PA12T5GPI0 (5V)PA14T6GPI0PA14T9GPI0 (5V)PH1T8GPI0 (5V)PH4T9GPI0 (5V)PB13T12GPI0PH4T13GPI0 (5V)PB13T12GPI0PB14T13GPI0AVDDT14Analog power supply.PB14T15GPI0PD6T16GPI0	PH13	P13	GPIO (5V)	PD0	P14	GPIO (5V)
PB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnReset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R13GPIO (5V)PH15R14GPIO (5V)PH14R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPA12T5GPIO (5V)PA14T6GPIOPH14T9GPIO (5V)PH1T10GPIO (5V)PH14T1GPIO (5V)PA14T6GPIOPH15T11GPIO (5V)PA14T6GPIO (5V)PH14T13GPIO (5V)PH1T10GPIO (5V)PH14T13GPIO (5V)PH1T10GPIO (5V)PH10T11GPIO (5V)PH3T12GPIOPH10T11GPIO (5V)PH3T12GPIOPH10T11GPIO (5V)PH3<	PD3	P15	GPIO	PD8	P16	GPIO
PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIO (5V)PH4R11GPIO (5V)PH6R10GPIO (5V)PH4R13GPIO (5V)PH12R12GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PD7R16GPIOPA7T3GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PH3T12GPIOPH10T11GPIO (5V)PH6T14Analog power supply.PB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PB7	R1	GPIO	PC3	R2	GPIO (5V)
BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- termal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensurePB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R1GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PD7R16GPIOPA12T5GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PB13T12GPIOPH10T11GPIO (5V)PB13T12GPIOPB14T13GPIO (5V)PD6T16GPIOPD1T15GPIOPD6T16GPIO	PC5	R3	GPIO	PA9	R4	GPIO
PB10 R7 GPIO (5V) PH0 R8 GPIO (5V) PH3 R9 GPIO (5V) PH6 R10 GPIO PH9 R11 GPIO (5V) PH12 R12 GPIO (5V) PH14 R13 GPIO (5V) PH12 R14 GPIO (5V) PD14 R13 GPIO (5V) PH12 R14 GPIO (5V) PD2 R15 GPIO (5V) PD7 R16 GPIO PD2 R15 GPIO (5V) PD7 R16 GPIO PB8 T1 GPIO (5V) PD7 R16 GPIO PB4 T3 GPIO (5V) PC4 T2 GPIO PA12 T5 GPIO (5V) PA14 T6 GPIO PB11 T7 GPIO (5V) PH1 T8 GPIO (5V) PH4 T9 GPIO (5V) PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14	BODEN	R5	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	RESETn	R6	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PH3R9GPIO (5V)PH6R10GPIOPH9R11GPIO (5V)PH12R12GPIO (5V)PH14R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIO (5V)PB8T1GPIO (5V)PC4T2GPIOPA7T3GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PB10	R7	GPIO (5V)	PH0	R8	GPIO (5V)
PH9 R11 GPIO (5V) PH12 R12 GPIO (5V) PH14 R13 GPIO (5V) PH15 R14 GPIO (5V) PD2 R15 GPIO (5V) PD7 R16 GPIO PB8 T1 GPIO (5V) PC4 T2 GPIO PA7 T3 GPIO PA10 T4 GPIO PA12 T5 GPIO (5V) PA10 T4 GPIO PA12 T5 GPIO (5V) PA14 T6 GPIO PB11 T7 GPIO PH1 T8 GPIO (5V) PH10 T1 GPIO PH1 T8 GPIO (5V) PH4 T9 GPIO PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH3	R9	GPIO (5V)	PH6	R10	GPIO
PH14 R13 GPIO (5V) PH15 R14 GPIO (5V) PD2 R15 GPIO (5V) PD7 R16 GPIO PB8 T1 GPIO (5V) PC4 T2 GPIO PA7 T3 GPIO (5V) PA10 T4 GPIO PA12 T5 GPIO (5V) PA14 T6 GPIO PB11 T7 GPIO (5V) PA14 T6 GPIO (5V) PH44 T9 GPIO (5V) PH1 T8 GPIO (5V) PH4 T9 GPIO (5V) PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO (5V) PB13 T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH9	R11	GPIO (5V)	PH12	R12	GPIO (5V)
PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIOPC4T2GPIOPA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PH14	R13	GPIO (5V)	PH15	R14	GPIO (5V)
PB8T1GPIOPC4T2GPIOPA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PD2	R15	GPIO (5V)	PD7	R16	GPIO
PA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PB8	T1	GPIO	PC4	T2	GPIO
PA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PA7	Т3	GPIO	PA10	T4	GPIO
PB11 T7 GPIO PH1 T8 GPIO (5V) PH4 T9 GPIO PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PA12	T5	GPIO (5V)	PA14	Т6	GPIO
PH4 T9 GPIO PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PB11	T7	GPIO	PH1	Т8	GPIO (5V)
PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH4	Т9	GPIO	PH7	T10	GPIO (5V)
PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH10	T11	GPIO (5V)	PB13	T12	GPIO
PD1 T15 GPIO PD6 T16 GPIO	PB14	T13	GPIO	AVDD	T14	Analog power supply.
	PD1	T15	GPIO	PD6	T16	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA15	B1	GPIO	PE14	B2	GPIO
PE12	B3	GPIO	PE8	B4	GPIO
PD11	B5	GPIO	PD9	B6	GPIO
PF8	B7	GPIO	PF6	B8	GPIO
PF14	B9	GPIO (5V)	PF12	B10	GPIO
PF2	B11	GPIO	PF0	B12	GPIO (5V)
PC14	B13	GPIO (5V)	VREGO	B14	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs
PA1	C1	GPIO	PA0	C2	GPIO
PD13	C3	GPIO (5V)	PE10	C4	GPIO
PI8	C5	GPIO (5V)	PI7	C6	GPIO (5V)
Pl6	C7	GPIO (5V)	PF5	C8	GPIO
PF15	C9	GPIO (5V)	PF4	C10	GPIO
PF3	C11	GPIO	PC13	C12	GPIO (5V)
PC12	C13	GPIO (5V)	VREGI	C14	Input to 5 V regulator.
PA3	D1	GPIO	PA2	D2	GPIO
PD14	D3	GPIO (5V)	PC11	D12	GPIO (5V)
PC10	D13	GPIO (5V)	PC9	D14	GPIO (5V)
PA5	E1	GPIO	PA4	E2	GPIO
PD15	E3	GPIO (5V)	IOVDD1	E6	Digital IO power supply 1.
VSS	E7 E8 G5 G7 G8 G10 H5 H7 H8 H10 K7 K8	Ground	IOVDD0	E9 F10 J5 J10 K6 K9	Digital IO power supply 0.
PC8	E12	GPIO (5V)	PI5	E13	GPIO (5V)
Pl4	E14	GPIO (5V)	PG0	F1	GPIO (5V)
PA6	F2	GPIO	PG1	F3	GPIO (5V)
IOVDD2	F5	Digital IO power supply 2.	PI3	F12	GPIO (5V)
PI2	F13	GPIO (5V)	PI1	F14	GPIO (5V)
PG3	G1	GPIO (5V)	PG4	G2	GPIO (5V)
PG2	G3	GPIO (5V)	PE7	G12	GPIO
PI0 G1	G13	GPIO (5V)	DECOUPLE	G14	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	K2	GPIO (5V)	PE0	K12	GPIO (5V)
VREGSW	K13	DCDC regulator switching node	PC2	L1	GPIO (5V)
PC3	L2	GPIO (5V)	PA7	L3	GPIO
PB9	L13	GPIO (5V)	PB10	L14	GPIO (5V)
PD1	L17	GPIO	PC6	L18	GPIO
PC7	L19	GPIO	VREGVSS	L20	Voltage regulator VSS
PB7	M1	GPIO	PC4	M2	GPIO
PA8	M3	GPIO	PA10	M4	GPIO
PA13	M5	GPIO (5V)	PA14	M6	GPIO
RESETn	M7	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB12	M8	GPIO
PD0	M9	GPIO (5V)	PD2	M10	GPIO (5V)
PD3	M11	GPIO	PD4	M12	GPIO
PD8	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	BODEN	N7	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.
PB13	N8	GPIO	PB14	N9	GPIO
AVDD	N10	Analog power supply.	PD5	N11	GPIO
PD6	N12	GPIO	PD7	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD15	J2	GPIO (5V)	PC6	J12	GPIO
DECOUPLE	J13	Decouple output for on-chip voltage regulator. An external decoupling ca- pacitor is required at this pin.	PC0	K1	GPIO (5V)
PC1	K2	GPIO (5V)	PD8	K13	GPIO
PC2	L1	GPIO (5V)	PC3	L2	GPIO (5V)
PA7	L3	GPIO	PB9	L15	GPIO (5V)
PB10	L16	GPIO (5V)	PD0	L17	GPIO (5V)
PD1	L18	GPIO	PD4	L19	GPIO
PD7	L20	GPIO	PB7	M1	GPIO
PC4	M2	GPIO	PA8	M3	GPIO
PA10	M4	GPIO	PA13	M5	GPIO (5V)
PA14	M6	GPIO	RESETn	M7	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	M9 M10 N11	Analog power supply.	PD3	M12	GPIO
PD6	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	PB12	N7	GPIO
PB13	N9	GPIO	PB14	N10	GPIO
PD2	N12	GPIO (5V)	PD5	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.



Figure 5.8. EFM32GG11B8xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO



Figure 5.12. EFM32GG11B8xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.12. EFM32GG11B8xx in QFP64 Device Pino
--

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD13		EBI_ARDY #1	TIM2_CDTI0 #1 TIM3_CC1 #6 WTIM0_CC1 #1	ETH_MDIO #1 US4_CTS #1 US5_CLK #1	ETM_TD1 #1
PI15				CAN1_TX #7 US3_CS #5	
PI14				CAN1_RX #7 US3_CLK #5	
PI13				CAN0_TX #7 US3_RX #5	
PI12				CAN0_RX #7 US3_TX #5	
PI10		EBI_A15 #2	TIM4_CC2 #3	US4_CTS #3	
PI7		EBI_A12 #2	TIM1_CC1 #7 TIM4_CC2 #2 WTIM3_CC1 #5	US4_RX #3	
PF15	BUSCY BUSDX		TIM1_CC2 #6 TIM4_CC2 #1 WTIM3_CC2 #7	US5_TX #2 I2C2_SDA #5	
PF12	BUSDY BUSCX	EBI_NANDREn #5	TIM4_CC2 #0 TIM1_CC3 #5 TIM5_CC0 #7 WTIM3_CC2 #6	US5_CS #2 I2C2_SCL #3 USB_ID	
PF4	BUSDY BUSCX LCD_SEG2	EBI_WEn #0 EBI_WEn #5	TIM4_CC1 #0 TIM0_CDTI1 #2 TIM1_CC2 #5 WTIM3_CC1 #6	US1_RTS #2 I2C2_SDA #3	PRS_CH1 #1
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BUSACMP1Y BU- SACMP1X	EBI_NANDREn #4	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LE- TIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 U1_RTS #0 LEU0_RX #5 I2C2_SCL #1	LES_CH15 PRS_CH1 #2 ACMP3_O #1 DBG_SWO #1
PC14	VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSACMP1Y BU- SACMP1X	EBI_NANDWEn #4	TIM0_CDTI1 #1 TIM1_CC1 #0 TIM1_CC3 #4 TIM5_CC0 #6 WTIM3_CC0 #3 LE- TIM0_OUT0 #5 PCNT0_S1IN #0	US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 U1_CTS #0 LEU0_TX #5 I2C2_SDA #1	LES_CH14 PRS_CH0 #2 ACMP3_O #2
PA2	BUSBY BUSAX LCD_SEG15	EBI_AD11 #0 EBI_DTEN #3	TIM0_CC2 #0 TIM3_CC2 #4	ETH_RMIIRXD0 #0 ETH_MIITXD2 #0 SDIO_DAT2 #1 US1_RX #6 US3_CLK #0 QSPI0_DQ0 #1	CMU_CLK0 #0 PRS_CH8 #1 ETM_TD0 #3
PG0	BUSACMP2Y BU- SACMP2X	EBI_AD00 #2	TIM6_CC0 #0 TIM2_CDTI0 #3 WTIM0_CDTI1 #1 LETIM1_OUT0 #6	ETH_MIITXCLK #1 US3_TX #4 QSPI0_SCLK #2	CMU_CLK2 #3

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PB0	BUSBY BUSAX LCD_SEG32	EBI_AD00 #1 EBI_CS0 #3 EBI_A16 #0	TIM2_CDTI0 #0 TIM1_CC0 #2 TIM3_CC2 #7 WTIM0_CC0 #5 PCNT0_S0IN #5 PCNT1_S1IN #2	LEU1_TX #3	PRS_CH4 #1 ACMP0_O #5
PE0	BUSDY BUSCX	EBI_A00 #2 EBI_A07 #0	TIM3_CC0 #1 WTIM1_CC1 #3 PCNT0_S0IN #1	CAN0_RX #6 U0_TX #1 I2C1_SDA #2	PRS_CH22 #1 ACMP2_O #1
PC7	BUSACMP0Y BU- SACMP0X OPA3_N	EBI_A06 #0 EBI_A13 #1 EBI_A21 #3	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 LEU1_RX #0 I2C0_SCL #2	LES_CH7 PRS_CH15 #1 ETM_TD0 #2
PB1	BUSAY BUSBX LCD_SEG33	EBI_AD01 #1 EBI_CS1 #3 EBI_A17 #0	TIM2_CDTI1 #0 TIM1_CC1 #2 WTIM0_CC1 #5 LE- TIM1_OUT1 #5 PCNT0_S1IN #5	ETH_MIICRS #0 US5_RX #2 LEU1_RX #3	PRS_CH5 #1
PB2	BUSBY BUSAX LCD_SEG34	EBI_AD02 #1 EBI_CS2 #3 EBI_A18 #0	TIM2_CDTI2 #0 TIM1_CC2 #2 WTIM0_CC2 #5 LE- TIM1_OUT0 #5	ETH_MIICOL #0 US1_CS #6	PRS_CH18 #0 ACMP0_O #6
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	EBI_AD03 #1 EBI_CS3 #3 EBI_A19 #0	TIM1_CC3 #2 WTIM0_CC0 #6 PCNT1_S0IN #1	ETH_MIICRS #2 ETH_MDIO #0 SDIO_DAT6 #1 US2_TX #1 US3_TX #2 QSPI0_DQ4 #1	PRS_CH19 #0 ACMP0_O #7
PC6	BUSACMP0Y BU- SACMP0X OPA3_P	EBI_A05 #0	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 LEU1_TX #0 I2C0_SDA #2	LES_CH6 PRS_CH14 #1 ETM_TCLK #2
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	EBI_AD04 #1 EBI_ARDY #3 EBI_A20 #0	WTIM0_CC1 #6 PCNT1_S1IN #1	ETH_MIICOL #2 ETH_MDC #0 SDIO_DAT7 #1 US2_RX #1 QSPI0_DQ5 #1 LEU1_TX #4	PRS_CH20 #0
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	EBI_AD05 #1 EBI_ALE #3 EBI_A21 #0	WTIM0_CC2 #6 LE- TIM1_OUT0 #4 PCNT0_S0IN #6	ETH_TSUEXTCLK #0 US0_RTS #4 US2_CLK #1 QSPI0_DQ6 #1 LEU1_RX #4	PRS_CH21 #0
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	EBI_AD06 #1 EBI_WEn #3 EBI_A22 #0	TIM0_CC0 #3 TIM2_CC0 #4 WTIM3_CC0 #6 LE- TIM1_OUT1 #4 PCNT0_S1IN #6	ETH_TSUTMRTOG #0 US0_CTS #4 US2_CS #1 QSPI0_DQ7 #1	PRS_CH12 #1
PD5	BUSADC0Y BU- SADC0X OPA2_OUT	EBI_A09 #1 EBI_A18 #3	TIM6_CC1 #7 WTIM0_CDTI1 #4 WTIM1_CC3 #1 WTIM2_CC2 #5	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3	PRS_CH11 #2 ETM_TD3 #0 ETM_TD3 #2

Alternate LOCATION		ATION	
Functionality	0 - 3	4 - 7	Description
SDIO_DAT7	0: PD9 1: PB4		SDIO Data 7.
SDIO_WP	0: PF9 1: PC5 2: PB15 3: PB9		SDIO Write Protect.
TIM0_CC0	0: PA0 1: PF6 2: PD1 3: PB6	4: PF0 5: PC4 6: PA8 7: PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PF7 2: PD2 3: PC0	4: PF1 5: PC5 6: PA9 7: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PF8 2: PD3 3: PC1	4: PF2 5: PA7 6: PA10 7: PA13	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PC13 2: PF3 3: PC2	4: PB7	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PC14 2: PF4 3: PC3	4: PB8	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PC15 2: PF5 3: PC4	4: PB11	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PC13 1: PE10 2: PB0 3: PB7	4: PD6 5: PF2 6: PF13 7: PI6	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PC14 1: PE11 2: PB1 3: PB8	4: PD7 5: PF3 6: PF14 7: PI7	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PC15 1: PE12 2: PB2 3: PB11	4: PC13 5: PF4 6: PF15 7: PI8	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PC12 1: PE13 2: PB3 3: PB12	4: PC14 5: PF12 6: PF5 7: PI9	Timer 1 Capture Compare input / output channel 3.
TIM2_CC0	0: PA8 1: PA12 2: PC8 3: PF2	4: PB6 5: PC2 6: PG8 7: PG5	Timer 2 Capture Compare input / output channel 0.

Table 12.2. QFN64 PCB Land Pattern Dimensions

Dimension	Тур
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	7.30
Y2	7.30

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This Land Pattern Design is based on the IPC-7351 guidelines.

3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

6. The stencil thickness should be 0.125 mm (5 mils).

7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.

8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch can be used for the center ground pad.

9. A No-Clean, Type-3 solder paste is recommended.

10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.