

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	144
Program Memory Size	1MB (1M × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	192-VFBGA
Supplier Device Package	192-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024gl192-ar

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

	ETU ETU	Λ				1 DDC	
0x40024000	EIH	1		8%40100008		PRS	0x400e6000
0x40022400	LICD	1	CM4 Peripherals	8xe8866666	1 /	BMU	0x400e5400
0x40022000	USB			Q×dfffffff	1 .		0x400e5000
0x40020400	CMU			Oxd0000000		СМИ	0x400e4400
0x40020000	5M0	1	QSPIO	8559999999	l i		0x400e4000
0x4001d400	TENCO	4 、		8×8222222	1 /	EMU	0x400e3000
0x4001d000	TRNGO	· ·	EBI Region 3	0×8ffffffff	1 /	coverture.	0x4008f400
0x4001c800	OSPIO	1	5010	Av8hffffff	ł /		0x4008f000
0x4001c400	GPCBC	4 \	EBI Region 2	0288000000	i i	CSEN	0x4008e400
0x4001c000	Grence	· ·	EBI Region 1	8x84555555	/	GGEN	0x4008e000
0x4001b000	WTIMER3	1	EBI Region 0	8×83ffffff	1 /	12C2	0x40089c00
0x4001ac00	WTIMER2	4 、		0x80000000 0x7fffffff	ł j	12C1	0x40089800
0x4001a800	WTIMER1	· ·		0246010400		12C0	0x40089400
0x4001a400	WTIMERO	1	Bit Set	0x460f03ff		GPIO	0x40088000
0x4001a000	WHITEHO	1 \	(Peripherals / CRTP100)	0×46000000	,	VDACO	0x40086400
0x40019c00	TIMEB6			8×455‡5555	/	VDACU	0x40086000
0x40019800	TIMERS	1	Bit Clear	0x440f03ff	1 /	IDAC0	0x40084400
0x40019400	TIMER4	1	(Peripherals / CRYPTO0)	0×44000000			0x40084000
0x40019000	TIMEB3	([\]		8×43ffffff	1 /	ADC1	0x40082800
0x40018c00	TIMER3	1	Pit Pand	0x43e3ffff		ADC0	0x40082400
0x40018800	TIMEB1	1	(Peripherals / CRYPTO0 / SI	00) 0×42000000	l i		0x40082000
0x40018400	TIMEBO	(`	· ·	0x41ffffff	/	АСМРЗ	0x40080c00
0x40018000		1		0x40140000		ACMP2	0x40080800
0x40014800	UABT1	1 ,	USB	8%48199999	l (ACMPI	0x40080400
0x40014400	UABTO	· ·		8×488f5fff	1 /	ACMIPO	0×40080000
0x40014000		1	SDIO	0x400f1fff	1 /	PCNT2	0x4006ec00
0x40011800	USART5	1 ,	3510	0x40011000	l.	PCNT1	0x4006e800
0x40011400	USART4	۱ ۱		8\$488+8466	/	PCNT0	0x4006e400
0x40011000	USART3	1 \	CRYPTO0	8×488‡8355	/		0x4006a800
0x40010c00	USART2		Peripherals 1	0×400effff	1	LEUART1	0x4006a400
0x40010800	USART1			0x40040000	4	LEUARTO	0x4006a000
0x40010400	USART0	1	Peripherals 0	024000000	\mathbf{A}	L ETIMEB1	0×40066800
0x40010000			1	8x3f99999		LETIMERO	0x40066400
0x4000b400	EB	1 /	SRAM (bit-band)	8x25fffffff	1 \		0×40066000
0x40006000		1 /		0x22000000	Λ.	RTCC	0x40062400
0x40004800	CAN1			0220080000	\ \		0x40062000
0x40004400	CANO	1 .	RAM2 (data space)	8×28845555	N.	RTC	0×40060000
0x40004000		1 /	RAM1 (data space)	8×2883ffff	1 \	LECENCE	0x40055400
0x40003000	LDMA		DAMO (data array)	0x2001ffff	۱ <i>۱</i>	LESENSE	0x40055000
0x40002000			RAMU (data space)	020000000		ICD	0x40054400
0x40001400	FPUEH			⊎x1tttttt			0x40054000
0×40001000			Code		\ \	WDOG1	UX40052800
0x400000000	MSC	/		0×00000000		WDOG0	0x40052400
0.0000000000000000000000000000000000000		-			-		- 0140002000

Figure 3.3. EFM32GG11 Memory Map — Peripherals

4.1.11 Flash Memory Characteristics⁵

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Flash erase cycles before failure	EC _{FLASH}		10000	—		cycles
Flash data retention	RET _{FLASH}	T ≤ 85 °C	10	_	_	years
		T ≤ 125 °C	10	_	_	years
Word (32-bit) programming time	t _{W_PROG}	Burst write, 128 words, average time per word	20	26.2	32	μs
		Single word	59	68.7	83	μs
Page erase time ⁴	t _{PERASE}		20	26.8	35	ms
Mass erase time ¹	t _{MERASE}		20	26.9	35	ms
Device erase time ^{2 3}	t _{DERASE}	T ≤ 85 °C	—	80.7	95	ms
		T ≤ 125 °C	—	80.7	100	ms
Erase current ⁶	I _{ERASE}	Page Erase	—	—	1.7	mA
		Mass or Device Erase	—	_	2.1	mA
Write current ⁶	I _{WRITE}		_	_	3.9	mA
Supply voltage during flash erase and write	V _{FLASH}		1.62		3.6	V

Table 4.19. Flash Memory Characteristics⁵

Note:

- 1. Mass erase is issued by the CPU and erases all flash.
- 2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
- 3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
- 4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
- 5. Flash data retention information is published in the Quarterly Quality and Reliability Report.

6. Measured at 25 °C.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Start up time	t _{IDAC_SU}	Output within 1% of steady state value	—	5	_	μs
Settling time, (output settled	t _{IDAC_SETTLE}	Range setting is changed	—	5	_	μs
ue),		Step value is changed		1	_	μs
Current consumption ²	I _{IDAC}	EM0 or EM1 Source mode, ex- cluding output current, Across op- erating temperature range	_	11	TBD	μA
		EM0 or EM1 Sink mode, exclud- ing output current, Across operat- ing temperature range	_	13	TBD	μA
		EM2 or EM3 Source mode, ex- cluding output current, T = 25 °C	—	0.05		μA
		EM2 or EM3 Sink mode, exclud- ing output current, T = 25 °C	—	0.07	_	μA
		EM2 or EM3 Source mode, excluding output current, $T \ge 85 \text{ °C}$	—	11	_	μA
		EM2 or EM3 Sink mode, exclud- ing output current, $T \ge 85 \degree C$	—	13	_	μA
Output voltage compliance in source mode, source current	I _{COMP} _SRC	RANGESEL1=0, output voltage = min(V _{IOVDD} , V _{AVDD} ² -100 mv)	_	0.11	_	%
sourced at 0 V		RANGESEL1=1, output voltage = min(V _{IOVDD} , V _{AVDD} ² -100 mV)		0.06		%
		RANGESEL1=2, output voltage = min(V _{IOVDD} , V _{AVDD} ² -150 mV)	_	0.04		%
		RANGESEL1=3, output voltage = min(V _{IOVDD} , V _{AVDD} ² -250 mV)	_	0.03	_	%
Output voltage compliance in sink mode, sink current	I _{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV		0.29		%
change relative to current sunk at IOVDD		RANGESEL1=1, output voltage = 100 mV	_	0.27		%
		RANGESEL1=2, output voltage = 150 mV	—	0.12	_	%
		RANGESEL1=3, output voltage = 250 mV	_	0.03		%

Note:

1. In IDAC_CURPROG register.

 The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Supply current, continuous conversions, WARMUP- MODE=KEEPCSENWARM	ICSEN_ACTIVE	SAR or Delta Modulation conver- sions of 33 pF capacitor, CS0CG=0 (Gain = 10x), always on		90.5		μA
HFPERCLK supply current	ICSEN_HFPERCLK	Current contribution from HFPERCLK when clock to CSEN block is enabled.	_	2.25	_	µA/MHz

Note:

 Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

4.1.27 Serial Data I/O Host Controller (SDIO)

SDIO DS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.46. SDIO DS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Clock frequency during data transfer	F _{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	_	_	23	MHz
		Using HFXO	_	_	TBD	MHz
Clock low time	t _{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	_	_	ns
		Using HFXO	TBD	—	_	ns
Clock high time	t _{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7		_	ns
		Using HFXO	TBD	_	_	ns
Clock rise time	t _R		1.69	3.23	_	ns
Clock fall time	t _F		1.42	2.79	_	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t _{ISU}		6	_	_	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t _{IH}		0	—	_	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	todly		0	_	14	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t _{OH}		5			ns

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.



Figure 4.24. EM0 Active Mode Typical Supply Current vs. Temperature



Figure 4.28. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Supply



Figure 5.2. EFM32GG11B8xx in BGA152 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.2. EFM32GG11B8xx in BGA152 D	Device Pinout
--------------------------------------	---------------

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE13	A2	GPIO
PE11	A3	GPIO	PE9	A4	GPIO
PD12	A5	GPIO	PD10	A6	GPIO
PF9	A7	GPIO	PF7	A8	GPIO
PF13	A9	GPIO (5V)	VBUS	A10	USB VBUS signal and auxiliary input to 5 V regulator.
PF1	A11	GPIO (5V)	PC15	A12	GPIO (5V)
PF11	A13	GPIO (5V)	PF10	A14	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC4	13	GPIO	PC5	14	GPIO
PB7	15	GPIO	PB8	16	GPIO
PA8	17	GPIO	PA12	18	GPIO (5V)
PA14	19	GPIO	RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	21	GPIO	PB12	22	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD8	35	GPIO	VREGVSS	36	Voltage regulator VSS
VREGSW	37	DCDC regulator switching node	VREGVDD	38	Voltage regulator VDD input
DVDD	39	Digital power supply.	DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	41	GPIO	PE5	42	GPIO
PE6	43	GPIO	PE7	44	GPIO
VREGI	45	Input to 5 V regulator.	VREGO	46	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs
PF10	47	GPIO (5V)	PF11	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.
PF12	53	GPIO	PF5	54	GPIO
PE8	57	GPIO	PE9	58	GPIO
PE10	59	GPIO	PE11	60	GPIO
PE12	61	GPIO	PE13	62	GPIO
PE14	63	GPIO	PE15	64	GPIO
Note:	1	1]		I	

1. GPIO with 5V tolerance are indicated by (5V).



Figure 5.16. EFM32GG11B8xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling ca- pacitor is required at this pin.	PC8	41	GPIO (5V)
PC9	42	GPIO (5V)	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO
Note:		·]			·

1. GPIO with 5V tolerance are indicated by (5V).

Alternate LOC		ATION	
Functionality	0 - 3	4 - 7	Description
EBI_CS1	0: PD10 1: PA11 2: PC1 3: PB1	4: PE9	External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	0: PD11 1: PA12 2: PC2 3: PB2	4: PE10	External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	0: PD12 1: PB15 2: PC3 3: PB3	4: PE11	External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	0: PA7 1: PF6 2: PB12 3: PA0		External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	0: PA8 1: PF7 2: PH0 3: PA1		External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	0: PA9 1: PD9 2: PH1 3: PA2		External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	0: PA11 1: PD11 2: PH3 3: PA4		External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	0: PC3 1: PD15 2: PB9 3: PC4	4: PC15 5: PF12	External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	0: PC5 1: PD14 2: PA13 3: PC2	4: PC14 5: PF11	External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	0: PF5 1: PA14 2: PA12 3: PC0	4: PF9 5: PF5	External Bus Interface (EBI) Read Enable output.
EBI_VSNC	0: PA10 1: PD10 2: PH2 3: PA3		External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	0: PF4 1: PA13 2: PC5 3: PB6	4: PF8 5: PF4	External Bus Interface (EBI) Write Enable output.
ETH_MDC	0: PB4 1: PD14 2: PC1 3: PA6		Ethernet Management Data Clock.

Alternate	LOCA		
Functionality	0 - 3	4 - 7	Description
ETH_MIITXD2	0: PA2 1: PG2		Ethernet MII Transmit Data Bit 2.
ETH_MIITXD3	0: PA1 1: PG1		Ethernet MII Transmit Data Bit 3.
ETH_MIITXEN	0: PA5 1: PG5		Ethernet MII Transmit Enable.
ETH_MIITXER	0: PA6 1: PG6		Ethernet MII Transmit Error.
ETH_RMIICRSDV	0: PA4 1: PD11		Ethernet RMII Carrier Sense / Data Valid.
ETH_RMIIREFCLK	0: PA3 1: PD10		Ethernet RMII Reference Clock.
ETH_RMIIRXD0	0: PA2 1: PD9		Ethernet RMII Receive Data Bit 0.
ETH_RMIIRXD1	0: PA1 1: PF9		Ethernet RMII Receive Data Bit 1.
ETH_RMIIRXER	0: PA5 1: PD12		Ethernet RMII Receive Error.
ETH_RMIITXD0	0: PE15 1: PF7		Ethernet RMII Transmit Data Bit 0.
ETH_RMIITXD1	0: PE14 1: PF6		Ethernet RMII Transmit Data Bit 1.
ETH_RMIITXEN	0: PA0 1: PF8		Ethernet RMII Transmit Enable.
ETH_TSUEXTCLK	0: PB5 1: PD15 2: PC2 3: PF8		Ethernet IEEE1588 External Reference Clock.

Alternate Functionality	Location	Priority
QSPI0_DQS	0: PF9	High Speed
QSPI0_SCLK	0: PF6	High Speed
SDIO_CLK	0: PE13	High Speed
SDIO_CMD	0: PE12	High Speed
SDIO_DAT0	0: PE11	High Speed
SDIO_DAT1	0: PE10	High Speed
SDIO_DAT2	0: PE9	High Speed
SDIO_DAT3	0: PE8	High Speed
SDIO_DAT4	0: PD12	High Speed
SDIO_DAT5	0: PD11	High Speed
SDIO_DAT6	0: PD10	High Speed
SDIO_DAT7	0: PD9	High Speed
TIM0_CC0	3: PB6	Non-interference
TIM0_CC1	3: PC0	Non-interference
TIM0_CC2	3: PC1	Non-interference
TIM0_CDTI0	1: PC13	Non-interference
TIM0_CDTI1	1: PC14	Non-interference
TIM0_CDTI2	1: PC15	Non-interference
TIM2_CC0	0: PA8	Non-interference
TIM2_CC1	0: PA9	Non-interference
TIM2_CC2	0: PA10	Non-interference
TIM2_CDTI0	0: PB0	Non-interference
TIM2_CDTI1	0: PB1	Non-interference
TIM2_CDTI2	0: PB2	Non-interference
TIM4_CC0	0: PF3	Non-interference
TIM4_CC1	0: PF4	Non-interference
TIM4_CC2	0: PF12	Non-interference
TIM4_CDTI0	0: PD0	Non-interference
TIM4_CDTI1	0: PD1	Non-interference
TIM4_CDTI2	0: PD3	Non-interference
TIM6_CC0	0: PG0	Non-interference
TIM6_CC1	0: PG1	Non-interference
TIM6_CC2	0: PG2	Non-interference
TIM6_CDTI0	0: PG3	Non-interference
TIM6_CDTI1	0: PG4	Non-interference
TIM6_CDTI2	0: PG5	Non-interference

7. BGA152 Package Specifications

7.1 BGA152 Package Dimensions



Figure 7.1. BGA152 Package Drawing

Dimension	Min	Тур	Мах		
A	-	-	1.20		
A1	0.05	-	0.15		
A2	0.95	1.00	1.05		
b	0.17	0.22	0.27		
b1	0.17	0.20	0.23		
С	0.09	-	0.20		
c1	0.09	-	0.16		
D	16.0 BSC				
E	16.0 BSC				
D1	14.0 BSC				
E1	14.0 BSC				
е	0.50 BSC				
L1	1 REF				
L	0.45	0.60	0.75		
θ	0	3.5	7		
θ1	0	-	-		
θ2	11	12	13		
θ3	11	12	13		
R1	0.08	-	-		
R2	0.08	-	0.2		
S	0.2	-	-		
ааа	0.2				
bbb	0.2				
ССС	0.08				
ddd	0.08				
еее	0.05				

Table 10.1. TQFP100 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. QFN64 Package Specifications

12.1 QFN64 Package Dimensions



Figure 12.1. QFN64 Package Drawing

Table 12.2. QFN64 PCB Land Pattern Dimensions

Dimension	Тур
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	7.30
Y2	7.30

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This Land Pattern Design is based on the IPC-7351 guidelines.

3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

6. The stencil thickness should be 0.125 mm (5 mils).

7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.

8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch can be used for the center ground pad.

9. A No-Clean, Type-3 solder paste is recommended.

10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.