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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024gm64-a

- **Timers/Counters**
 - 7× 16-bit Timer/Counter
 - 3 + 4 Compare/Capture/PWM channels (4 + 4 on one timer instance)
 - Dead-Time Insertion on several timer instances
 - 4× 32-bit Timer/Counter
 - 32-bit Real Time Counter and Calendar (RTCC)
 - 24-bit Real Time Counter (RTC)
 - 32-bit Ultra Low Energy CRYOTIMER for periodic wakeup from any Energy Mode
 - 2× 16-bit Low Energy Timer for waveform generation
 - 3× 16-bit Pulse Counter with asynchronous operation
 - 2× Watchdog Timer with dedicated RC oscillator
- **Low Energy Sensor Interface (LESENSE)**
 - Autonomous sensor monitoring in Deep Sleep Mode
 - Wide range of sensors supported, including LC sensors and capacitive buttons
 - Up to 16 inputs
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
 - 2-pin Serial Wire Debug interface
 - 1-pin Serial Wire Viewer
 - 4-pin JTAG interface
 - Embedded Trace Macrocell (ETM)
- **Pre-Programmed USB/UART Bootloader**
- **Wide Operating Range**
 - 1.8 V to 3.8 V single power supply
 - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
 - Standard (-40 °C to 85 °C T_{AMB}) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
 - QFN64 (9x9 mm)
 - TQFP64 (10x10 mm)
 - TQFP100 (14x14 mm)
 - BGA112 (10x10 mm)
 - BGA120 (7x7 mm)
 - BGA152 (8x8 mm)
 - BGA192 (7x7mm)

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3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Giant Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only privileged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range ⁶	T_A	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage ²	V_{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage ^{2 1}	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass, $T \leq 85^\circ\text{C}$	—	—	200	mA
		DCDC in bypass, $T > 85^\circ\text{C}$	—	—	100	mA
DVDD operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	V_{IOVDD}	All IOVDD pins ⁵	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor ^{3 4}	$C_{DECOUPLE}$		0.75	1.0	2.75	μF
HFCORECLK frequency	f_{CORE}	VSCALE2, MODE = WS3	—	—	72	MHz
		VSCALE2, MODE = WS2	—	—	54	MHz
		VSCALE2, MODE = WS1	—	—	36	MHz
		VSCALE2, MODE = WS0	—	—	18	MHz
		VSCALE0, MODE = WS2	—	—	20	MHz
		VSCALE0, MODE = WS1	—	—	14	MHz
		VSCALE0, MODE = WS0	—	—	7	MHz
HFCLK frequency	f_{HFCLK}	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFSRCCLK frequency	$f_{HFSRCCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFBUSCLK frequency	$f_{HFBUSCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERCLK frequency	$f_{HFPERCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERBCLK frequency	$f_{HFPERBCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFPERCCLK frequency	$f_{HFPERCCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive ² , $T \leq 85\text{ }^{\circ}\text{C}$	—	—	200	mA
		Low noise (LN) mode, Heavy Drive ² , $T > 85\text{ }^{\circ}\text{C}$	—	—	100	mA
		Low noise (LN) mode, Medium Drive ²	—	—	100	mA
		Low noise (LN) mode, Light Drive ²	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 0	—	—	75	μA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 3	—	—	10	mA
DCDC nominal output capacitor ⁵	C_{DCDC}	25% tolerance	1	4.7	4.7	μF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	μH
Resistance in Bypass mode	R_{BYP}		—	1.2	2.5	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF . Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 μF . See Application Note AN0948 for details.

4.1.13 Voltage Monitor (VMON)

Table 4.21. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I _{SENSE})	I _{VMON}	In EM0 or EM1, 1 supply monitored, T ≤ 85 °C	—	6.0	TBD	μA
		In EM0 or EM1, 4 supplies monitored, T ≤ 85 °C	—	14.9	TBD	μA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I _{SENSE}	In EM0 or EM1	—	2	—	μA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V _{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N _{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t _{VMON_RES}	Supply drops at 1V/μs rate	—	460	—	ns
Hysteresis	V _{VMON_HYST}		—	26	—	mV

4.1.23 I2C

4.1.23.1 I2C Standard-mode (Sm)¹

Table 4.31. I2C Standard-mode (Sm)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	μs
SCL clock high time	t_{HIGH}		4	—	—	μs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time ³	t_{HD_DAT}		100	—	3450	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	μs
(Repeated) START condition hold time	t_{HD_STA}		4	—	—	μs
STOP condition set-up time	t_{SU_STO}		4	—	—	μs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	μs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

EBI Read Enable Output Timing

Timing applies to both EBI_REn and EBI_NANDREn for all addressing modes and both polarities. Output timing for EBI_AD applies only to multiplexed addressing modes D8A24ALE and D16A16ALE. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.38. EBI Read Enable Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_REn / EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CS _n , EBI_BLn invalid	t _{OH_REn}	IOVDD ≥ 1.62 V	-23 + (RDHOLD * t _{HFCOR-ECLK})	—	—	ns
		IOVDD ≥ 3.0 V	-13 + (RDHOLD * t _{HFCOR-ECLK})	—	—	ns
Output setup time, from EBI_AD, EBI_A, EBI_CS _n , EBI_BLn valid to leading EBI_REn / EBI_NANDREn edge ¹	t _{OSU_REn}	IOVDD ≥ 1.62 V	-12 + (RDSETUP * t _{HFCOR-ECLK})	—	—	ns
		IOVDD ≥ 3.0 V	-11 + (RDSETUP * t _{HFCOR-ECLK})	—	—	ns
EBI_REn pulse width ^{1 2}	t _{WIDTH_REn}	IOVDD ≥ 1.62 V	-6 + (MAX(1, RDSTRB) * t _{HFCOR-ECLK})	—	—	ns
		IOVDD ≥ 3.0 V	-4 + (MAX(1, RDSTRB) * t _{HFCOR-ECLK})	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of t_{WIDTH_REn} and increases the length of t_{OSU_REn} by 1/2 * t_{HFCLKNODIV}.
2. When page mode is used, RDSTRB is replaced by RDPA for page hits.

EBI Ready/Wait Timing Requirements

Timing applies to both EBI_REn and EBI_WEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.41. EBI Ready/Wait Timing Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge	t_{SU_ARDY}	IOVDD \geq 1.62 V	$55 + (3 * t_{HFCOR-ECLK})$	—	—	ns
		IOVDD \geq 3.0 V	$36 + (3 * t_{HFCOR-ECLK})$	—	—	ns
Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid	t_{H_ARDY}	IOVDD \geq 1.62 V	-9	—	—	ns

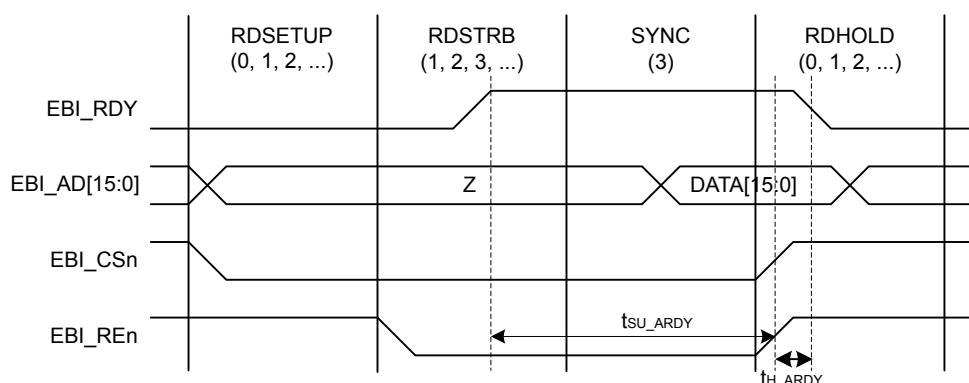


Figure 4.8. EBI Ready/Wait Timing Requirements

RMII Receive Timing

Timing is specified with $3.0\text{ V} \leq \text{IOVDD} \leq 3.8\text{ V}$, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.45. Ethernet RMII Receive Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REF_CLK frequency	$F_{\text{REF_CLK}}$	Output slew rate set to 7	—	50	—	MHz
REF_CLK duty cycle	$DC_{\text{REF_CLK}}$		35	—	65	%
Setup time, RXD[1:0], CRS_DV, RX_ER valid to REF_CLK	t_{SU}		4	—	—	ns
Hold time, REF_CLK to RXD[1:0], CRS_DV, RX_ER change	t_{HD}		2	—	—	ns

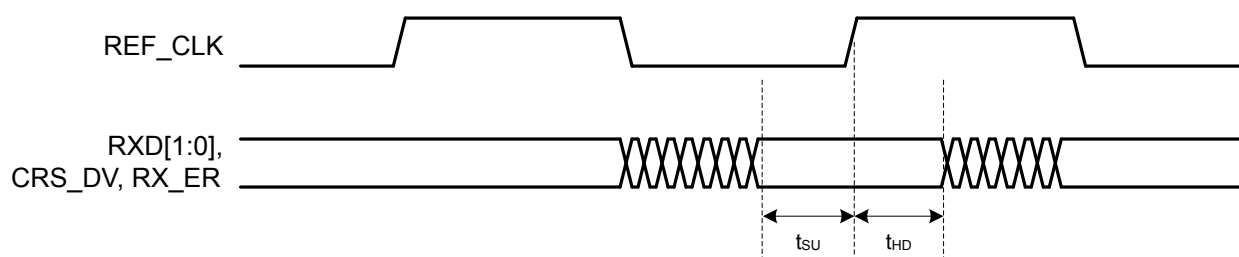


Figure 4.12. Ethernet RMII Receive Timing

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 μ H, CDCDC = 4.7 μ F, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

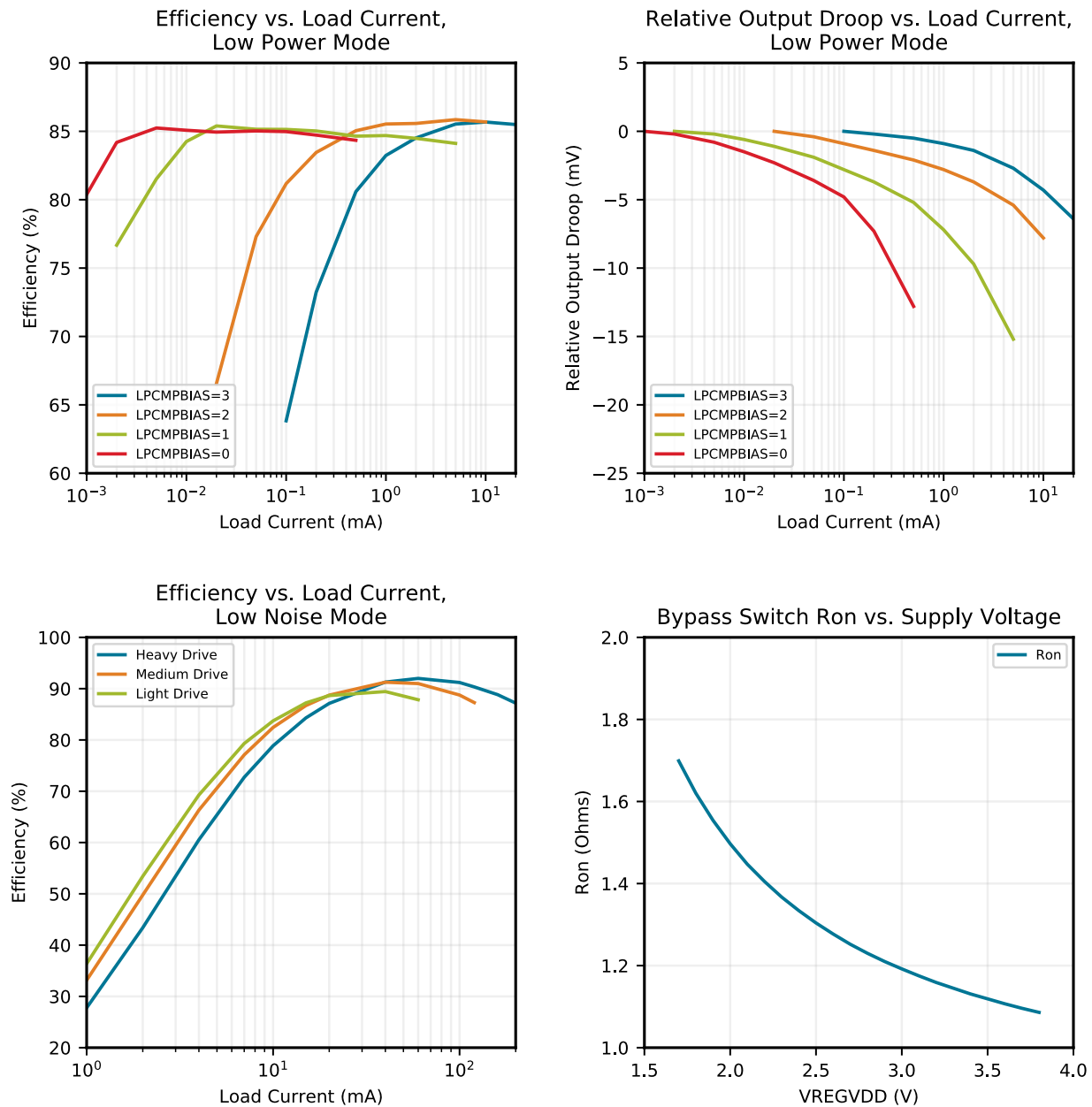


Figure 4.29. DC-DC Converter Typical Performance Characteristics

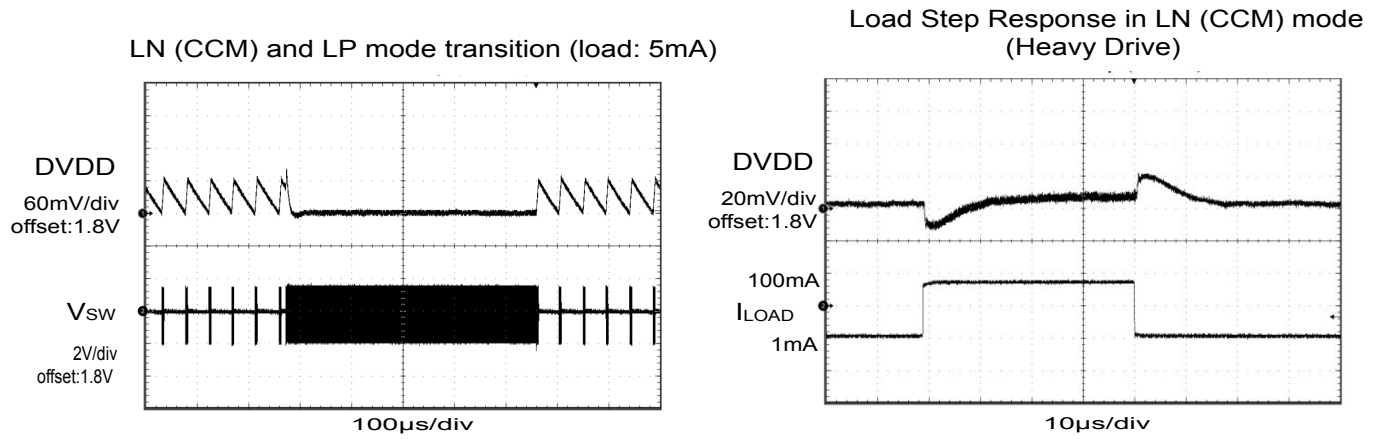


Figure 4.30. DC-DC Converter Transition Waveforms

5.3 EFM32GG11B8xx in BGA120 Device Pinout

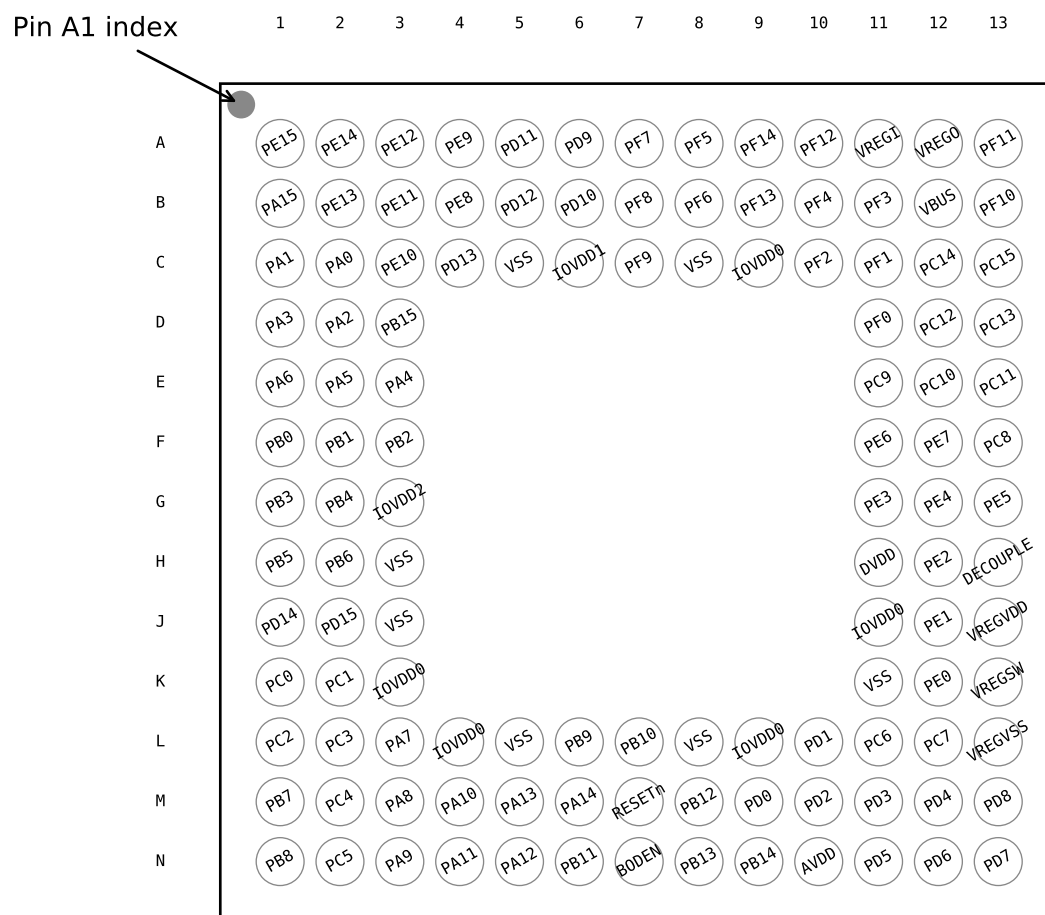


Figure 5.3. EFM32GG11B8xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.3. EFM32GG11B8xx in BGA120 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF14	A9	GPIO (5V)	PF12	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 58 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB9	37	GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41 45	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	46	GPIO (5V)	PD1	47	GPIO
PD2	48	GPIO (5V)	PD3	49	GPIO
PD4	50	GPIO	PD5	51	GPIO
PD6	52	GPIO	PD7	53	GPIO
PD8	54	GPIO	PC6	55	GPIO
PC7	56	GPIO	DVDD	57	Digital power supply.
DECOUPLE	59	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE0	60	GPIO (5V)
PE1	61	GPIO (5V)	PE2	62	GPIO
PE3	63	GPIO	PE4	64	GPIO
PE5	65	GPIO	PE6	66	GPIO
PE7	67	GPIO	PC8	68	GPIO (5V)
PC9	69	GPIO (5V)	PC10	70	GPIO (5V)
PC11	71	GPIO (5V)	PC12	72	GPIO (5V)
PC13	73	GPIO (5V)	PC14	74	GPIO (5V)
PC15	75	GPIO (5V)	PF0	76	GPIO (5V)
PF1	77	GPIO (5V)	PF2	78	GPIO

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
DBG_SWO	0: PF2 1: PC15 2: PD1 3: PD2		Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF5		Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2		Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
EBI_A00	0: PA12 1: PB9 2: PE0 3: PC5		External Bus Interface (EBI) address output pin 00.
EBI_A01	0: PA13 1: PB10 2: PE1 3: PA7		External Bus Interface (EBI) address output pin 01.
EBI_A02	0: PA14 1: PB11 2: PI0 3: PA8		External Bus Interface (EBI) address output pin 02.
EBI_A03	0: PB9 1: PB12 2: PI1 3: PA9		External Bus Interface (EBI) address output pin 03.
EBI_A04	0: PB10 1: PD0 2: PI2 3: PA10		External Bus Interface (EBI) address output pin 04.
EBI_A05	0: PC6 1: PD1 2: PI3 3: PA11		External Bus Interface (EBI) address output pin 05.
EBI_A06	0: PC7 1: PD2 2: PI4 3: PA12		External Bus Interface (EBI) address output pin 06.
EBI_A07	0: PE0 1: PD3 2: PI5 3: PA13		External Bus Interface (EBI) address output pin 07.
EBI_A08	0: PE1 1: PD4 2: PC8 3: PA14		External Bus Interface (EBI) address output pin 08.
EBI_A09	0: PE2 1: PD5 2: PC9 3: PB9		External Bus Interface (EBI) address output pin 09.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A10	0: PE3 1: PD6 2: PC10 3: PB10		External Bus Interface (EBI) address output pin 10.
EBI_A11	0: PE4 1: PD7 2: PI6 3: PB11		External Bus Interface (EBI) address output pin 11.
EBI_A12	0: PE5 1: PD8 2: PI7 3: PB12		External Bus Interface (EBI) address output pin 12.
EBI_A13	0: PE6 1: PC7 2: PI8 3: PD0		External Bus Interface (EBI) address output pin 13.
EBI_A14	0: PE7 1: PE2 2: PI9 3: PD1		External Bus Interface (EBI) address output pin 14.
EBI_A15	0: PC8 1: PE3 2: PI10 3: PD2		External Bus Interface (EBI) address output pin 15.
EBI_A16	0: PB0 1: PE4 2: PH4 3: PD3		External Bus Interface (EBI) address output pin 16.
EBI_A17	0: PB1 1: PE5 2: PH5 3: PD4		External Bus Interface (EBI) address output pin 17.
EBI_A18	0: PB2 1: PE6 2: PH6 3: PD5		External Bus Interface (EBI) address output pin 18.
EBI_A19	0: PB3 1: PE7 2: PH7 3: PD6		External Bus Interface (EBI) address output pin 19.
EBI_A20	0: PB4 1: PC8 2: PH8 3: PD7		External Bus Interface (EBI) address output pin 20.
EBI_A21	0: PB5 1: PC9 2: PH9 3: PC7		External Bus Interface (EBI) address output pin 21.
EBI_A22	0: PB6 1: PC10 2: PH10 3: PE4		External Bus Interface (EBI) address output pin 22.

7. BGA152 Package Specifications

7.1 BGA152 Package Dimensions

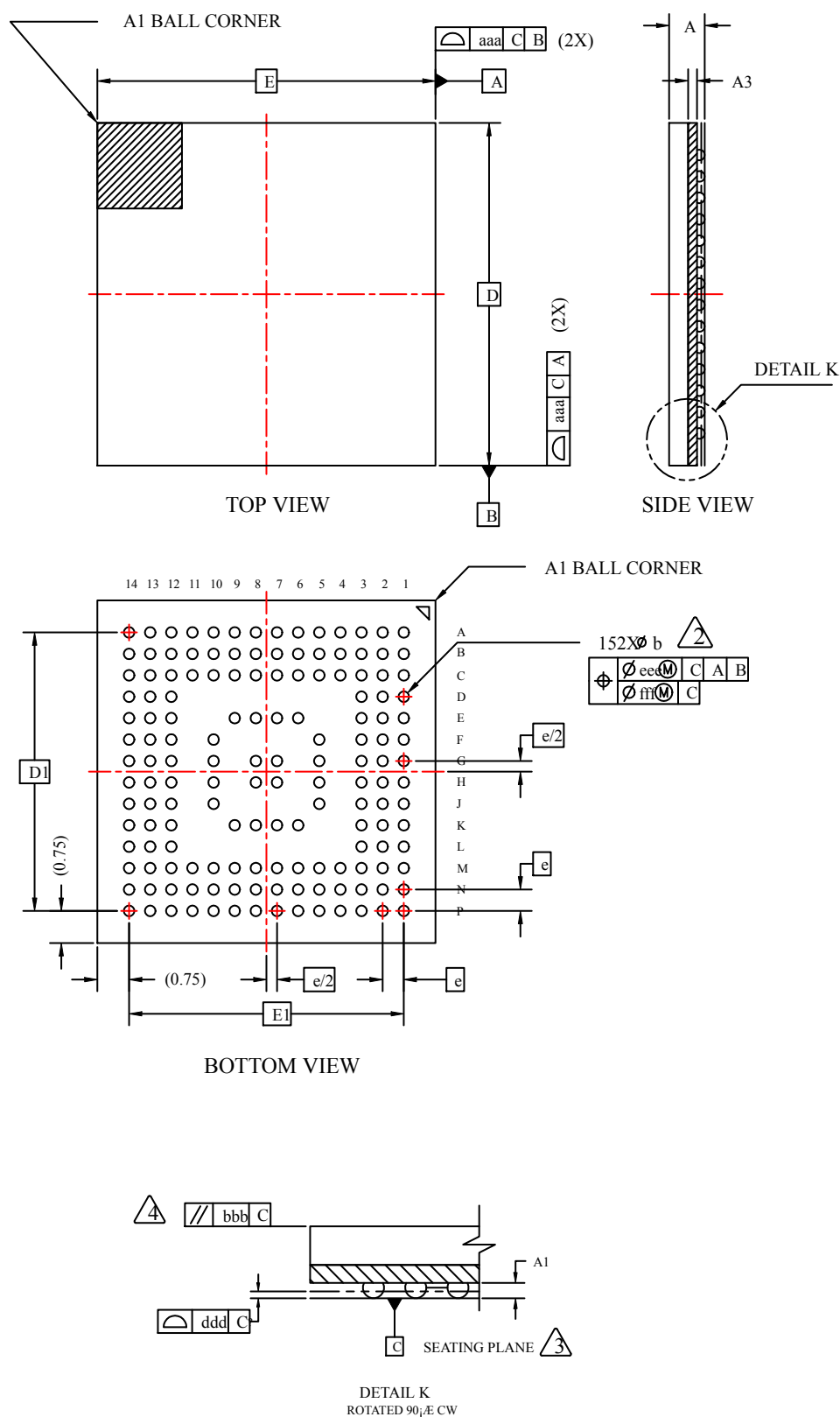


Table 9.2. BGA112 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.45	
C1		8.00	
C2		8.00	
E1		0.8	
E2		0.8	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

12.2 QFN64 PCB Land Pattern

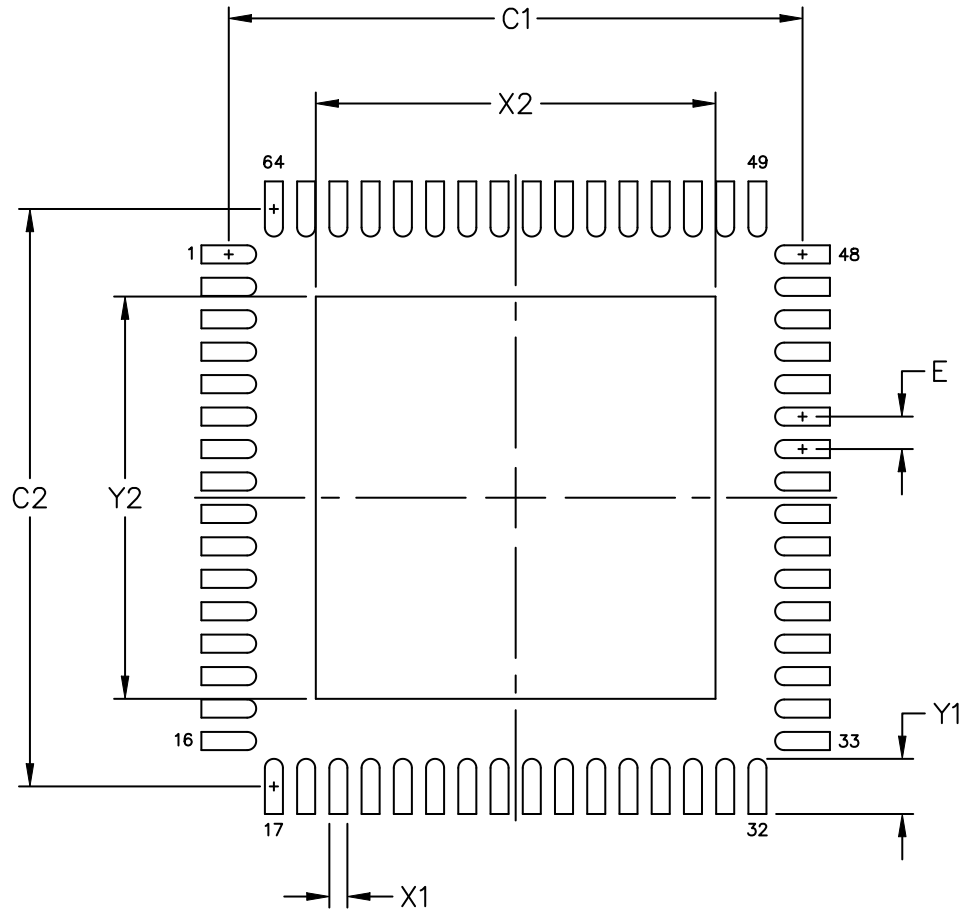


Figure 12.2. QFN64 PCB Land Pattern Drawing

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SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>