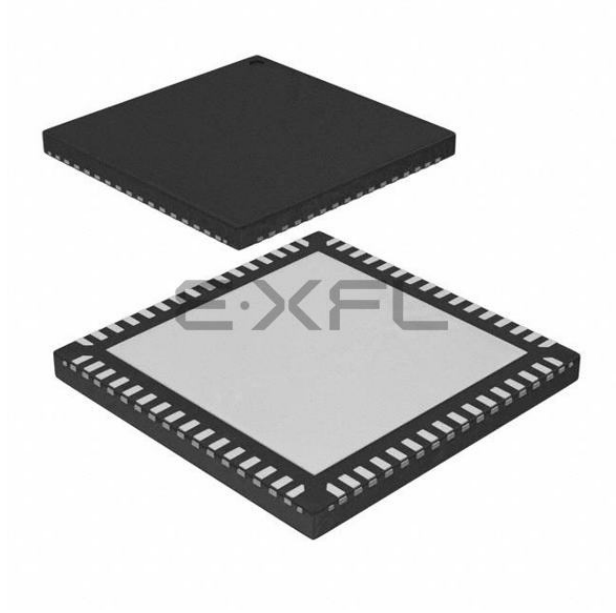
Silicon Labs - EFM32GG11B840F1024GM64-AR Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024gm64-ar

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.10.4 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed. More information about the bootloader protocol and usage can be found in *AN0003: UART Bootloader*. Application notes can be found on the Silicon Labs website (www.silabs.com/32bit-appnotes) or within Simplicity Studio in the [**Documentation**] area.

4.1.6 Backup Supply Domain

Table 4.6. Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Backup supply voltage range	V_{BU_VIN}		1.8	—	3.8	V
PWRRES resistor	R_{PWRRES}	EMU_BUCTRL_PWRRES = RES0	3400	3900	4400	Ω
		EMU_BUCTRL_PWRRES = RES1	1450	1800	2150	Ω
		EMU_BUCTRL_PWRRES = RES2	1000	1350	1700	Ω
		EMU_BUCTRL_PWRRES = RES3	525	815	1100	Ω
Output impedance between BU_VIN and BU_VOUT [2]	R_{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	35	110	185	Ω
		EMU_BUCTRL_VOUTRES = MED	475	775	1075	Ω
		EMU_BUCTRL_VOUTRES = WEAK	5600	6500	7400	Ω
Supply current	I_{BU_VIN}	BU_VIN not powering backup domain	—	11	TBD	nA
		BU_VIN powering backup domain[1]	—	550	TBD	nA

Note:

1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.
2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency limits	f_{HFRCO_BAND}	FREQRANGE = 0, FINETUNINGEN = 0	1	—	10	MHz
		FREQRANGE = 3, FINETUNINGEN = 0	2	—	17	MHz
		FREQRANGE = 6, FINETUNINGEN = 0	4	—	30	MHz
		FREQRANGE = 7, FINETUNINGEN = 0	5	—	34	MHz
		FREQRANGE = 8, FINETUNINGEN = 0	7	—	42	MHz
		FREQRANGE = 10, FINETUNINGEN = 0	12	—	58	MHz
		FREQRANGE = 11, FINETUNINGEN = 0	15	—	68	MHz
		FREQRANGE = 12, FINETUNINGEN = 0	18	—	83	MHz
		FREQRANGE = 13, FINETUNINGEN = 0	24	—	100	MHz
		FREQRANGE = 14, FINETUNINGEN = 0	28	—	119	MHz
		FREQRANGE = 15, FINETUNINGEN = 0	33	—	138	MHz
		FREQRANGE = 16, FINETUNINGEN = 0	43	—	163	MHz

Note:

1. Maximum DPLL lock time ~= 6 x (M+1) x t_{REF}, where t_{REF} is the reference clock period.

EBI Address Latch Enable Output Timing

Timing applies to multiplexed addressing modes D8A24ALE and D16A16ALE for both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.37. EBI Address Latch Enable Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_ALE edge to EBI_AD invalid[1] [2]	t_{OH_ALEn}	IOVDD ≥ 1.62 V	-22 + (ADDRHOLD * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-11 + (ADDRHOLD * $t_{HFCORECLK}$)	—	—	ns
Output setup time, from EBI_AD valid to leading EBI_ALE edge	t_{OSU_ALEn}	IOVDD ≥ 1.62 V	-12	—	—	ns
		IOVDD ≥ 3.0 V	-9	—	—	ns
EBI_ALEn pulse width[1]	t_{WIDTH_ALEn}	IOVDD ≥ 1.62 V	-4 + ((ADDRSETUP + 1) * $t_{\{\}HFCORECLK\{\}}$)	—	—	ns
		IOVDD ≥ 3.0 V	-3 + ((ADDRSETUP + 1) * $t_{\{\}HFCORECLK\{\}}$)	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALEn can be moved to the left by setting HALFALE=1. This decreases the length of t_{WIDTH_ALEn} and increases the length of t_{OSU_ALEn} by $t_{HFCORECLK}$ - 1/2 * $t_{HFCLKNODIV}$.
2. The figure shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

4.1.27 Serial Data I/O Host Controller (SDIO)

SDIO DS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.46. SDIO DS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	23	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.69	3.23	—	ns
Clock fall time	t_F		1.42	2.79	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}		0	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}		0	—	14	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}		5	—	—	ns

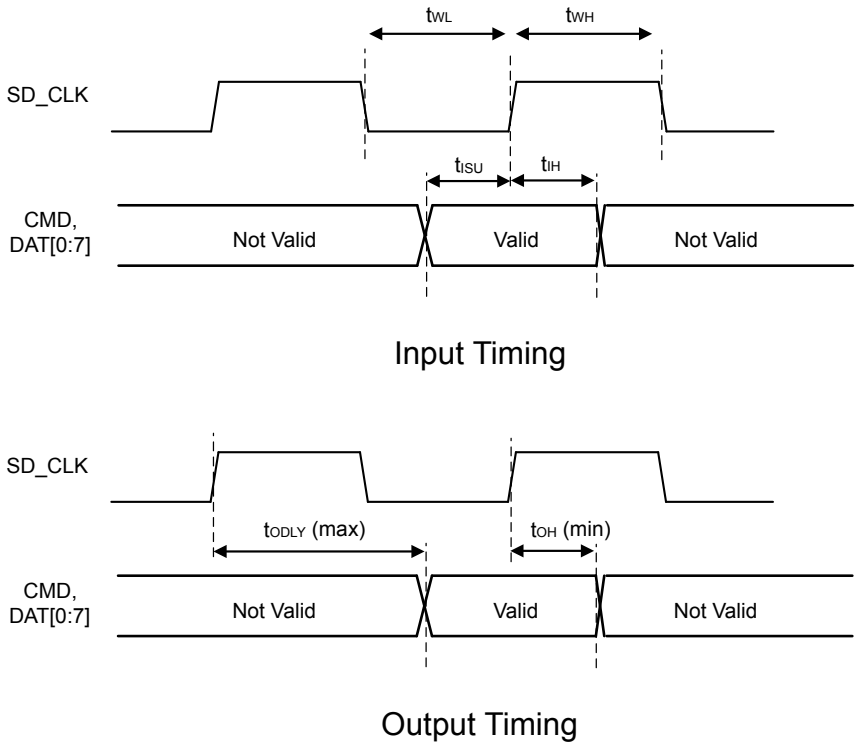

Figure 4.14. SDIO HS Mode Timing

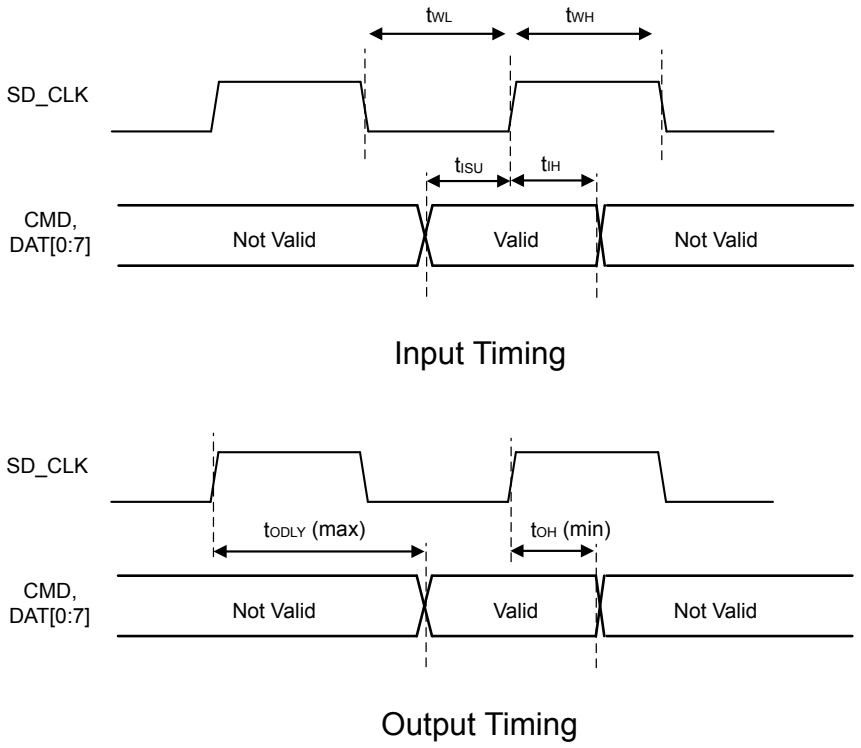

Figure 4.17. SDIO MMC SDR Mode Timing

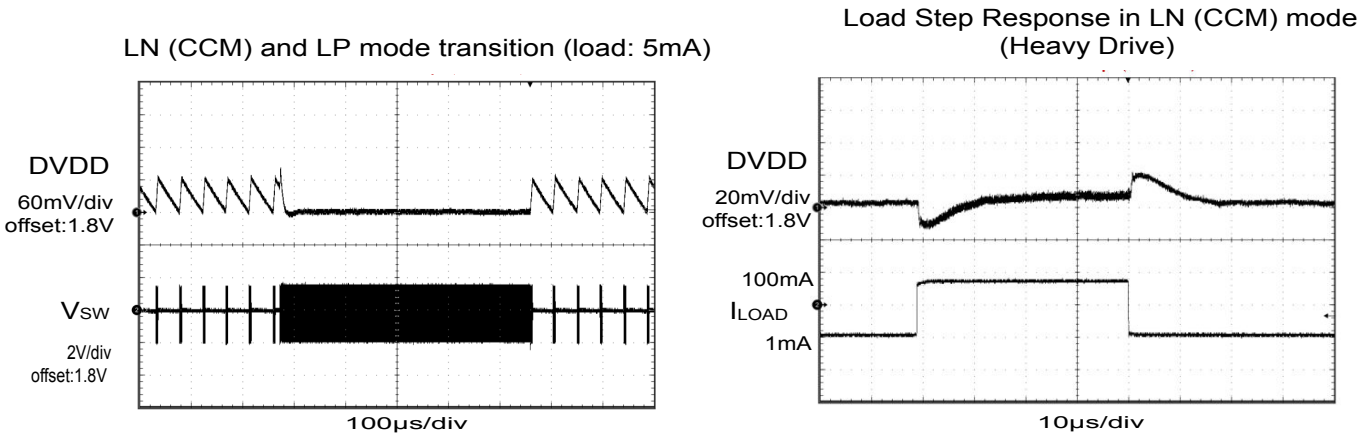

Figure 4.30. DC-DC Converter Transition Waveforms

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
IOVDD1	F7 G7	Digital IO power supply 1.	VSS	F8 G8 G9 H6 H7 H8 H9 H10 H11 J6 J7 J8 J9 J10 J11 K8 K9 L8 L9	Ground
NC	F9	No Connect.	IOVDD0	F10 F11 G10 G11 K6 K7 K10 K11 L6 L7 L10 L11	Digital IO power supply 0.
PI5	F14	GPIO (5V)	PI4	F15	GPIO (5V)
PI3	F16	GPIO (5V)	PA5	G1	GPIO
PG6	G2	GPIO (5V)	PG5	G3	GPIO (5V)
PI2	G14	GPIO (5V)	PI1	G15	GPIO (5V)
PI0	G16	GPIO (5V)	PA6	H1	GPIO
PG8	H2	GPIO (5V)	PG7	H3	GPIO (5V)
PE5	H14	GPIO	PE6	H15	GPIO
PE7	H16	GPIO	PG11	J1	GPIO (5V)
PG10	J2	GPIO (5V)	PG9	J3	GPIO (5V)
PE3	J14	GPIO	PE4	J15	GPIO
DECOUPLE	J16	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PG14	K1	GPIO
PG13	K2	GPIO	PG12	K3	GPIO
PE1	K14	GPIO (5V)	PE2	K15	GPIO
DVDD	K16	Digital power supply.	PG15	L1	GPIO (5V)
PB15	L2	GPIO (5V)	PB0	L3	GPIO
PE0	L14	GPIO (5V)	PC7	L15	GPIO
VREGVDD	L16	Voltage regulator VDD input	PB1	M1	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA15	B1	GPIO	PE14	B2	GPIO
PE12	B3	GPIO	PE8	B4	GPIO
PD11	B5	GPIO	PD9	B6	GPIO
PF8	B7	GPIO	PF6	B8	GPIO
PF14	B9	GPIO (5V)	PF12	B10	GPIO
PF2	B11	GPIO	PF0	B12	GPIO (5V)
PC14	B13	GPIO (5V)	VREGO	B14	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PA1	C1	GPIO	PA0	C2	GPIO
PD13	C3	GPIO (5V)	PE10	C4	GPIO
PI8	C5	GPIO (5V)	PI7	C6	GPIO (5V)
PI6	C7	GPIO (5V)	PF5	C8	GPIO
PF15	C9	GPIO (5V)	PF4	C10	GPIO
PF3	C11	GPIO	PC13	C12	GPIO (5V)
PC12	C13	GPIO (5V)	VREGI	C14	Input to 5 V regulator.
PA3	D1	GPIO	PA2	D2	GPIO
PD14	D3	GPIO (5V)	PC11	D12	GPIO (5V)
PC10	D13	GPIO (5V)	PC9	D14	GPIO (5V)
PA5	E1	GPIO	PA4	E2	GPIO
PD15	E3	GPIO (5V)	IOVDD1	E6	Digital IO power supply 1.
VSS	E7 E8 G5 G7 G8 G10 H5 H7 H8 H10 K7 K8	Ground	IOVDD0	E9 F10 J5 J10 K6 K9	Digital IO power supply 0.
PC8	E12	GPIO (5V)	PI5	E13	GPIO (5V)
PI4	E14	GPIO (5V)	PG0	F1	GPIO (5V)
PA6	F2	GPIO	PG1	F3	GPIO (5V)
IOVDD2	F5	Digital IO power supply 2.	PI3	F12	GPIO (5V)
PI2	F13	GPIO (5V)	PI1	F14	GPIO (5V)
PG3	G1	GPIO (5V)	PG4	G2	GPIO (5V)
PG2	G3	GPIO (5V)	PE7	G12	GPIO
PI0	G13	GPIO (5V)	DECOUPLE	G14	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PD15	J2	GPIO (5V)	PC6	J12	GPIO
DECOUPLE	J13	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC0	K1	GPIO (5V)
PC1	K2	GPIO (5V)	PD8	K13	GPIO
PC2	L1	GPIO (5V)	PC3	L2	GPIO (5V)
PA7	L3	GPIO	PB9	L15	GPIO (5V)
PB10	L16	GPIO (5V)	PD0	L17	GPIO (5V)
PD1	L18	GPIO	PD4	L19	GPIO
PD7	L20	GPIO	PB7	M1	GPIO
PC4	M2	GPIO	PA8	M3	GPIO
PA10	M4	GPIO	PA13	M5	GPIO (5V)
PA14	M6	GPIO	RESETn	M7	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	M9 M10 N11	Analog power supply.	PD3	M12	GPIO
PD6	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	PB12	N7	GPIO
PB13	N9	GPIO	PB14	N10	GPIO
PD2	N12	GPIO (5V)	PD5	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.6 EFM32GG11B4xx in BGA112 Device Pinout

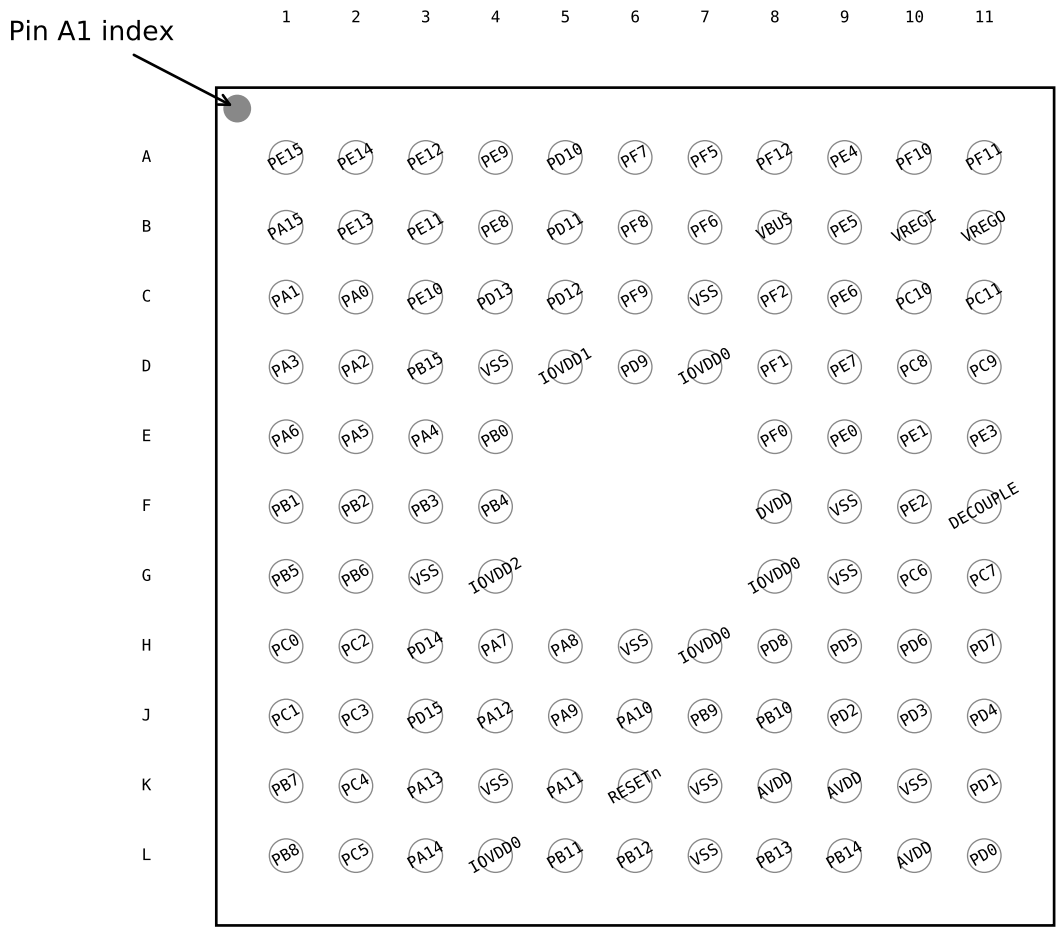

Figure 5.6. EFM32GG11B4xx in BGA112 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.6. EFM32GG11B4xx in BGA112 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD10	A5	GPIO	PF7	A6	GPIO
PF5	A7	GPIO	PF12	A8	GPIO
PE4	A9	GPIO	PF10	A10	GPIO (5V)
PF11	A11	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF2	78	GPIO	NC	79	No Connect.
PF12	80	GPIO	PF5	81	GPIO
PF6	84	GPIO	PF7	85	GPIO
PF8	86	GPIO	PF9	87	GPIO
PD9	88	GPIO	PD10	89	GPIO
PD11	90	GPIO	PD12	91	GPIO
PE8	92	GPIO	PE9	93	GPIO
PE10	94	GPIO	PE11	95	GPIO
PE12	96	GPIO	PE13	97	GPIO
PE14	98	GPIO	PE15	99	GPIO
PA15	100	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.14 EFM32GG11B4xx in QFP64 Device Pinout

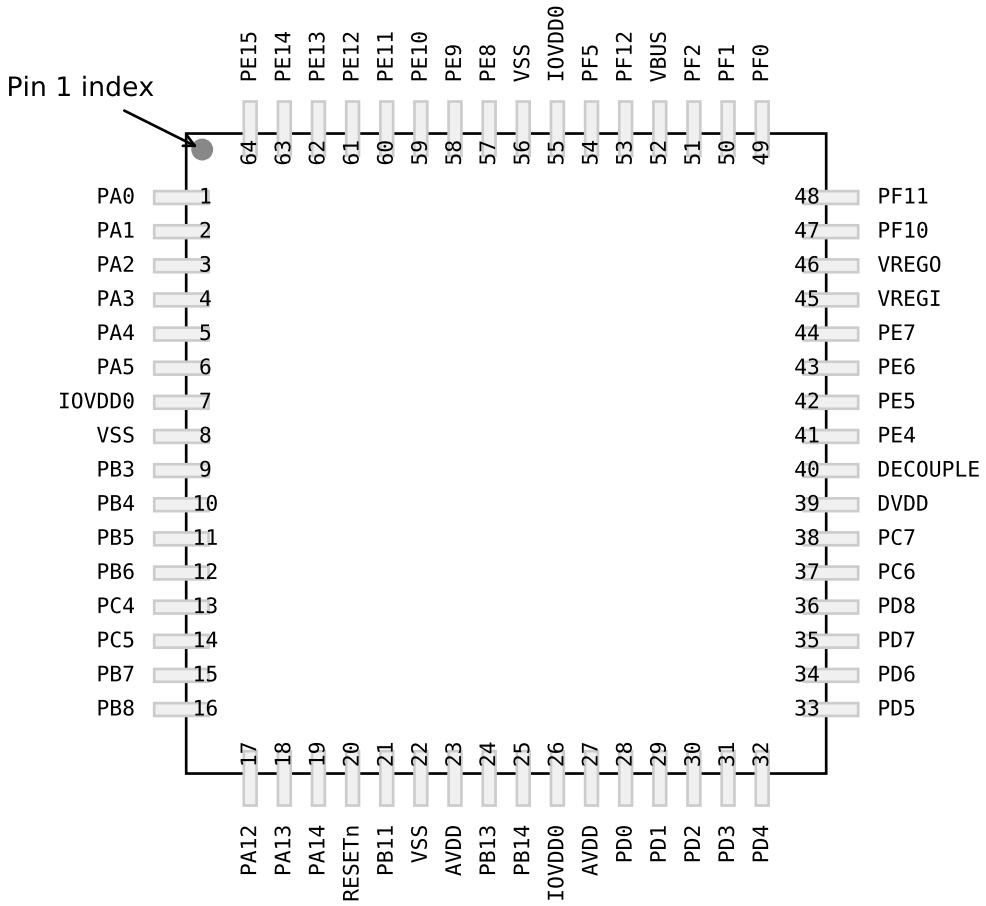

Figure 5.14. EFM32GG11B4xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.14. EFM32GG11B4xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO (5V)
PC9	42	GPIO (5V)	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PB13	BUSAY BUSBX HFXTAL_P		TIM6_CC0 #5 WTIM1_CC0 #0 PCNT2_S0IN #2	US0_CLK #4 US1_CTS #5 US5_CS #0 LEU0_TX #1	CMU_CLKI0 #3 PRS_CH7 #0
PB14	BUSBY BUSAX HFXTAL_N		TIM6_CC1 #5 WTIM1_CC1 #0 PCNT2_S1IN #2	US0_CS #4 US1_RTS #5 US5_CTS #0 LEU0_RX #1	PRS_CH6 #1
PD1	VDAC0_OUT1ALT / OPA1_OUTALT #4 BUSADC0Y BUSADC0X OPA3_OUT	EBI_A05 #1 EBI_A14 #3	TIM4_CDTI1 TIM0_CC0 #2 TIM6_CC0 #6 WTIM1_CC3 #0 PCNT2_S1IN #0	CAN0_TX #2 US1_RX #1	DBG_SWO #2
PD6	BUSADC0Y BUSADC0X ADC0_EXTP VDAC0_EXT ADC1_EXTP OPA1_P	EBI_A10 #1 EBI_A19 #3	TIM1_CC0 #4 TIM6_CC2 #7 WTIM0_CDTI2 #4 WTIM1_CC0 #2 LETIM0_OUT0 #0 PCNT0_S0IN #3	US0_RTS #5 US1_RX #2 US2_CTS #5 US3_CTS #2 U0_RTS #5 I2C0_SDA #1	CMU_CLK2 #2 LES_ALTEX0 PRS_CH5 #2 ACMP0_O #2 ETM_TD0 #0

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_AD08	0: PA15 1: PC1 2: PG8		External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	0: PA0 1: PC2 2: PG9		External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	0: PA1 1: PC3 2: PG10		External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	0: PA2 1: PC4 2: PG11		External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	0: PA3 1: PC5 2: PG12		External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	0: PA4 1: PA7 2: PG13		External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	0: PA5 1: PA8 2: PG14		External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	0: PA6 1: PA9 2: PG15		External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	0: PF3 1: PB9 2: PC4 3: PB5	4: PC11 5: PC11	External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	0: PF2 1: PD13 2: PB15 3: PB4	4: PC13 5: PF10	External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	0: PF6 1: PF8 2: PB10 3: PC1	4: PF6 5: PF6	External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	0: PF7 1: PF9 2: PB11 3: PC3	4: PF7 5: PF7	External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	0: PD9 1: PA10 2: PC0 3: PB0	4: PE8	External Bus Interface (EBI) Chip Select output 0.

7. BGA152 Package Specifications

7.1 BGA152 Package Dimensions

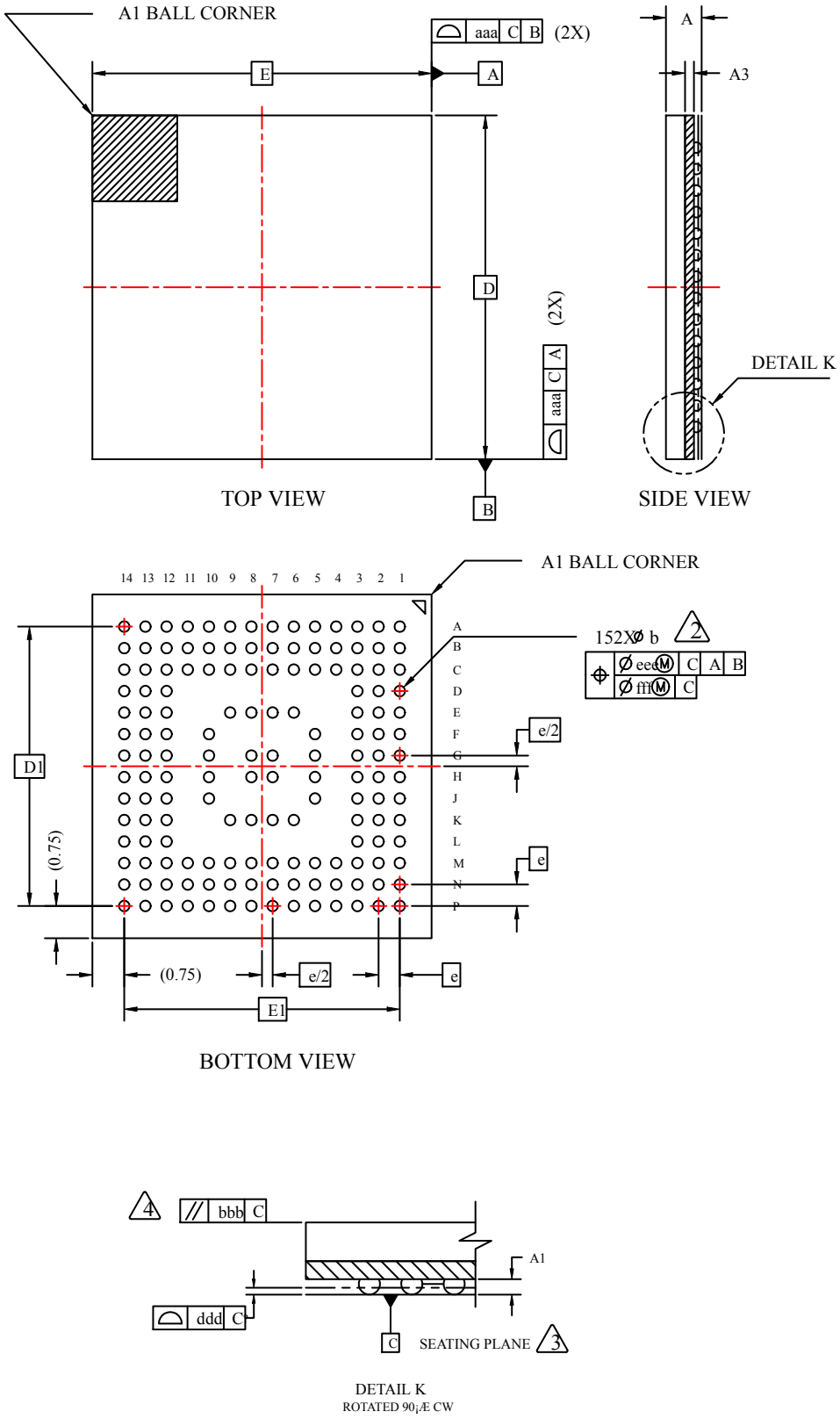

Figure 7.1. BGA152 Package Drawing

8.3 BGA120 Package Marking

Figure 8.3. BGA120 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

9.3 BGA112 Package Marking

Figure 9.3. BGA112 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.