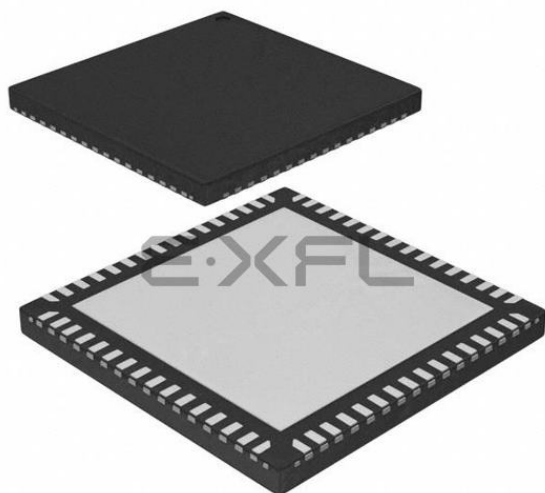




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024gm64-b

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	USB	Ethernet	QSPI	SDIO	LCD	GPIO	Package	Temp Range
EFM32GG11B520F2048GQ64-A	2048	512	Yes	No	No	No	No	Yes	50	QFP64	-40 to +85°C
EFM32GG11B510F2048GQ64-A	2048	384	Yes	No	No	No	No	Yes	50	QFP64	-40 to +85°C
EFM32GG11B520F2048GM64-A	2048	512	Yes	No	No	No	No	Yes	53	QFN64	-40 to +85°C
EFM32GG11B510F2048GM64-A	2048	384	Yes	No	No	No	No	Yes	53	QFN64	-40 to +85°C
EFM32GG11B520F2048IQ64-A	2048	512	Yes	No	No	No	No	Yes	50	QFP64	-40 to +125°C
EFM32GG11B510F2048IQ64-A	2048	384	Yes	No	No	No	No	Yes	50	QFP64	-40 to +125°C
EFM32GG11B520F2048IM64-A	2048	512	Yes	No	No	No	No	Yes	53	QFN64	-40 to +125°C
EFM32GG11B510F2048IM64-A	2048	384	Yes	No	No	No	No	Yes	53	QFN64	-40 to +125°C
EFM32GG11B420F2048GL120-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	93	BGA120	-40 to +85°C
EFM32GG11B420F2048IL120-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	93	BGA120	-40 to +125°C
EFM32GG11B420F2048GL112-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	87	BGA112	-40 to +85°C
EFM32GG11B420F2048IL112-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	87	BGA112	-40 to +125°C
EFM32GG11B420F2048GQ100-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	83	QFP100	-40 to +85°C
EFM32GG11B420F2048IQ100-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	83	QFP100	-40 to +125°C
EFM32GG11B420F2048GQ64-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	50	QFP64	-40 to +85°C
EFM32GG11B420F2048GM64-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	53	QFN64	-40 to +85°C
EFM32GG11B420F2048IQ64-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	50	QFP64	-40 to +125°C
EFM32GG11B420F2048IM64-A	2048	512	No	Yes	Yes	Yes	Yes	Yes	53	QFN64	-40 to +125°C
EFM32GG11B320F2048GL112-A	2048	512	No	No	No	No	No	Yes	90	BGA112	-40 to +85°C
EFM32GG11B310F2048GL112-A	2048	384	No	No	No	No	No	Yes	90	BGA112	-40 to +85°C
EFM32GG11B320F2048GQ100-A	2048	512	No	No	No	No	No	Yes	86	QFP100	-40 to +85°C
EFM32GG11B310F2048GQ100-A	2048	384	No	No	No	No	No	Yes	86	QFP100	-40 to +85°C
EFM32GG11B120F2048GQ64-A	2048	512	No	No	No	No	No	No	53	QFP64	-40 to +85°C
EFM32GG11B110F2048GQ64-A	2048	384	No	No	No	No	No	No	53	QFP64	-40 to +85°C
EFM32GG11B120F2048GM64-A	2048	512	No	No	No	No	No	No	56	QFN64	-40 to +85°C
EFM32GG11B110F2048GM64-A	2048	384	No	No	No	No	No	No	56	QFN64	-40 to +85°C
EFM32GG11B120F2048IQ64-A	2048	512	No	No	No	No	No	No	53	QFP64	-40 to +125°C
EFM32GG11B110F2048IQ64-A	2048	384	No	No	No	No	No	No	53	QFP64	-40 to +125°C
EFM32GG11B120F2048IM64-A	2048	512	No	No	No	No	No	No	56	QFN64	-40 to +125°C
EFM32GG11B110F2048IM64-A	2048	384	No	No	No	No	No	No	56	QFN64	-40 to +125°C

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3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such as switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μA and 64 μA with several ranges consisting of various step sizes.

3.8.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksp/s, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.8 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x36 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32GG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor with FPU achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 2048 kB flash program memory
 - Dual-bank memory with read-while-write support
- Up to 512 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire or 4-pin JTAG debug interface

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive ² , $T \leq 85\text{ }^{\circ}\text{C}$	—	—	200	mA
		Low noise (LN) mode, Heavy Drive ² , $T > 85\text{ }^{\circ}\text{C}$	—	—	100	mA
		Low noise (LN) mode, Medium Drive ²	—	—	100	mA
		Low noise (LN) mode, Light Drive ²	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 0	—	—	75	μA
		Low power (LP) mode, LPCMPBIASEMxx ³ = 3	—	—	10	mA
DCDC nominal output capacitor ⁵	C_{DCDC}	25% tolerance	1	4.7	4.7	μF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	μH
Resistance in Bypass mode	R_{BYP}		—	1.2	2.5	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF . Different settings for DCDCLNCOMPCTRL must be used if C_{DCDC} is lower than 4.7 μF . See Application Note AN0948 for details.

4.1.11 Flash Memory Characteristics⁵

Table 4.19. Flash Memory Characteristics⁵

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC _{FLASH}		10000	—	—	cycles
Flash data retention	RET _{FLASH}	T ≤ 85 °C	10	—	—	years
		T ≤ 125 °C	10	—	—	years
Word (32-bit) programming time	t _{W_PROG}	Burst write, 128 words, average time per word	20	26.2	32	μs
		Single word	59	68.7	83	μs
Page erase time ⁴	t _{PERASE}		20	26.8	35	ms
Mass erase time ¹	t _{MERASE}		20	26.9	35	ms
Device erase time ^{2 3}	t _{DERASE}	T ≤ 85 °C	—	80.7	95	ms
		T ≤ 125 °C	—	80.7	100	ms
Erase current ⁶	I _{ERASE}	Page Erase	—	—	1.7	mA
		Mass or Device Erase	—	—	2.1	mA
Write current ⁶	I _{WRITE}		—	—	3.9	mA
Supply voltage during flash erase and write	V _{FLASH}		1.62	—	3.6	V

Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
5. Flash data retention information is published in the Quarterly Quality and Reliability Report.
6. Measured at 25 °C.

4.1.23.2 I2C Fast-mode (Fm)¹

Table 4.32. I2C Fast-mode (Fm)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f _{SCL}		0	—	400	kHz
SCL clock low time	t _{LOW}		1.3	—	—	μs
SCL clock high time	t _{HIGH}		0.6	—	—	μs
SDA set-up time	t _{SU_DAT}		100	—	—	ns
SDA hold time ³	t _{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t _{SU_STA}		0.6	—	—	μs
(Repeated) START condition hold time	t _{HD_STA}		0.6	—	—	μs
STOP condition set-up time	t _{SU_STO}		0.6	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		1.3	—	—	μs

Note:

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD,DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

SDIO MMC DDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Table 4.53. SDIO MMC DDR Mode Timing (Location 0, 3V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F _{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t _{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t _{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t _R		1.13	2.37	—	ns
Clock fall time	t _F		1.01	2.02	—	ns
Input setup time, CMD valid to SD_CLK	t _{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD change	t _{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD valid	t _{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t _{OH}		3	—	—	ns
Input setup time, DAT[0:7] valid to SD_CLK	t _{ISU2X}		5.3	—	—	ns
Input hold time, SD_CLK to DAT[0:7] change	t _{IH2X}		2.5	—	—	ns
Output delay time, SD_CLK to DAT[0:7] valid	t _{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:7] change	t _{OH2X}		3	—	—	ns

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA15	B1	GPIO	PE14	B2	GPIO
PE12	B3	GPIO	PE8	B4	GPIO
PD11	B5	GPIO	PD9	B6	GPIO
PF8	B7	GPIO	PF6	B8	GPIO
PF14	B9	GPIO (5V)	PF12	B10	GPIO
PF2	B11	GPIO	PF0	B12	GPIO (5V)
PC14	B13	GPIO (5V)	VREG0	B14	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PA1	C1	GPIO	PA0	C2	GPIO
PD13	C3	GPIO (5V)	PE10	C4	GPIO
PI8	C5	GPIO (5V)	PI7	C6	GPIO (5V)
PI6	C7	GPIO (5V)	PF5	C8	GPIO
PF15	C9	GPIO (5V)	PF4	C10	GPIO
PF3	C11	GPIO	PC13	C12	GPIO (5V)
PC12	C13	GPIO (5V)	VREG1	C14	Input to 5 V regulator.
PA3	D1	GPIO	PA2	D2	GPIO
PD14	D3	GPIO (5V)	PC11	D12	GPIO (5V)
PC10	D13	GPIO (5V)	PC9	D14	GPIO (5V)
PA5	E1	GPIO	PA4	E2	GPIO
PD15	E3	GPIO (5V)	IOVDD1	E6	Digital IO power supply 1.
VSS	E7 E8 G5 G7 G8 G10 H5 H7 H8 H10 K7 K8	Ground	IOVDD0	E9 F10 J5 J10 K6 K9	Digital IO power supply 0.
PC8	E12	GPIO (5V)	PI5	E13	GPIO (5V)
PI4	E14	GPIO (5V)	PG0	F1	GPIO (5V)
PA6	F2	GPIO	PG1	F3	GPIO (5V)
IOVDD2	F5	Digital IO power supply 2.	PI3	F12	GPIO (5V)
PI2	F13	GPIO (5V)	PI1	F14	GPIO (5V)
PG3	G1	GPIO (5V)	PG4	G2	GPIO (5V)
PG2	G3	GPIO (5V)	PE7	G12	GPIO
PI0	G13	GPIO (5V)	DECOUPLE	G14	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA12	18	GPIO (5V)	PA13	19	GPIO (5V)
PA14	20	GPIO	RESETn	21	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB11	22	GPIO	PB12	23	GPIO
AVDD	24	Analog power supply.	PB13	25	GPIO
PB14	26	GPIO	PD0	28	GPIO (5V)
PD1	29	GPIO	PD2	30	GPIO (5V)
PD3	31	GPIO	PD4	32	GPIO
PD5	33	GPIO	PD6	34	GPIO
PD7	35	GPIO	PD8	36	GPIO
PC7	37	GPIO	VREGVSS	38	Voltage regulator VSS
VREGSW	39	DCDC regulator switching node	VREGVDD	40	Voltage regulator VDD input
DVDD	41	Digital power supply.	DECOUPLE	42	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PE4	43	GPIO	PE5	44	GPIO
PE6	45	GPIO	PE7	46	GPIO
PC12	47	GPIO (5V)	PC13	48	GPIO (5V)
PF0	49	GPIO (5V)	PF1	50	GPIO (5V)
PF2	51	GPIO	PF3	52	GPIO
PF4	53	GPIO	PF5	54	GPIO
PE8	56	GPIO	PE9	57	GPIO
PE10	58	GPIO	PE11	59	GPIO
PE12	60	GPIO	PE13	61	GPIO
PE14	62	GPIO	PE15	63	GPIO
PA15	64	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PH11	BUSACMP3Y BU-SACMP3X	EBI_A23 #2	TIM5_CC1 #1 WTIM1_CC3 #6	US5_RX #3 U1_TX #5 I2C1_SDA #5	
PH13	BUSACMP3Y BU-SACMP3X	EBI_A25 #2	TIM5_CC0 #2 WTIM1_CC1 #7 PCNT2_S1IN #7	US5_CS #3 U1_CTS #5 I2C1_SDA #6	
PD0	VDAC0_OUT0ALT / OPA0_OUTALT #4 OPA2_OUTALT BU-SADC0Y BUSADC0X	EBI_A04 #1 EBI_A13 #3	TIM4_CDTI0 TIM6_CC2 #5 WTIM1_CC2 #0 PCNT2_S0IN #0	CAN0_RX #2 US1_TX #1	
PD3	BUSADC0Y BU-SADC0X OPA2_N	EBI_A07 #1 EBI_A16 #3	TIM4_CDTI2 TIM0_CC2 #2 TIM6_CC2 #6 WTIM1_CC1 #1 WTIM2_CC0 #5	CAN1_RX #2 US1_CS #1 LEU1_RX #2	ETM_TD1 #0 ETM_TD1 #2
PD8	BU_VIN	EBI_A12 #1	WTIM1_CC2 #2	US2_RTS #5	CMU_CLK1 #1 PRS_CH12 #2 ACMP2_O #0
PB7	LFXTAL_P		TIM0_CDTI0 #4 TIM1_CC0 #3	US0_TX #4 US1_CLK #0 US3_RX #2 US4_TX #0 U0_CTS #4	PRS_CH22 #0
PC3	VDAC0_OUT0ALT / OPA0_OUTALT #3 BUSACMP0Y BU-SACMP0X	EBI_AD10 #1 EBI_CS3 #2 EBI_BL1 #3 EBI_NANDREN #0	TIM0_CDTI1 #3 TIM2_CC1 #5 WTIM0_CC2 #7 LE-TIM1_OUT1 #3	ETH_TSUTMRTOG #2 CAN1_TX #0 US1_CLK #4 US2_RX #0	LES_CH3 PRS_CH11 #1
PC5	BUSACMP0Y BU-SACMP0X OPA0_N	EBI_AD12 #1 EBI_WEN #2 EBI_NANDWEN #0 EBI_A00 #3	TIM0_CC1 #5 LE-TIM0_OUT1 #3 PCNT1_S1IN #3	SDIO_WP #1 US2_CS #0 US4_CS #0 U0_RX #4 U1_RTS #4 I2C1_SCL #0	LES_CH5 PRS_CH19 #2
PA9	BUSAY BUSBX LCD_SEG37	EBI_AD15 #1 EBI_A03 #3 EBI_DTEN #0	TIM2_CC1 #0 TIM0_CC1 #6 WTIM2_CC0 #0 LE-TIM0_OUT1 #6	US2_CLK #2	PRS_CH9 #0
PB10	BUSBY BUSAX	EBI_BL0 #2 EBI_A01 #1 EBI_A04 #0 EBI_A10 #3	WTIM2_CC1 #2 LE-TIM0_OUT1 #7	SDIO_CD #3 CAN0_TX #3 US1_RTS #0 US2_CTS #3 U1_RX #2	PRS_CH9 #2 ACMP1_O #6
PH0	BUSADC1Y BU-SADC1X	EBI_DCLK #2	WTIM2_CC2 #4	US0_CTS #6 LEU1_TX #5	
PH3	BUSADC1Y BU-SADC1X	EBI_HSNC #2	TIM6_CC1 #3	US1_RTS #6	
PH6	BUSADC1Y BU-SADC1X	EBI_A18 #2	TIM6_CDTI1 #3 WTIM2_CC2 #6	US4_CLK #4	
PH9	BUSACMP3Y BU-SACMP3X	EBI_A21 #2	TIM6_CC1 #4 WTIM1_CC1 #6 WTIM2_CC2 #7	US4_RTS #4	
PH12	BUSACMP3Y BU-SACMP3X	EBI_A24 #2	TIM5_CC2 #1 WTIM1_CC0 #7	US5_CLK #3 U1_RX #5 I2C1_SCL #5	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A10	0: PE3 1: PD6 2: PC10 3: PB10		External Bus Interface (EBI) address output pin 10.
EBI_A11	0: PE4 1: PD7 2: PI6 3: PB11		External Bus Interface (EBI) address output pin 11.
EBI_A12	0: PE5 1: PD8 2: PI7 3: PB12		External Bus Interface (EBI) address output pin 12.
EBI_A13	0: PE6 1: PC7 2: PI8 3: PD0		External Bus Interface (EBI) address output pin 13.
EBI_A14	0: PE7 1: PE2 2: PI9 3: PD1		External Bus Interface (EBI) address output pin 14.
EBI_A15	0: PC8 1: PE3 2: PI10 3: PD2		External Bus Interface (EBI) address output pin 15.
EBI_A16	0: PB0 1: PE4 2: PH4 3: PD3		External Bus Interface (EBI) address output pin 16.
EBI_A17	0: PB1 1: PE5 2: PH5 3: PD4		External Bus Interface (EBI) address output pin 17.
EBI_A18	0: PB2 1: PE6 2: PH6 3: PD5		External Bus Interface (EBI) address output pin 18.
EBI_A19	0: PB3 1: PE7 2: PH7 3: PD6		External Bus Interface (EBI) address output pin 19.
EBI_A20	0: PB4 1: PC8 2: PH8 3: PD7		External Bus Interface (EBI) address output pin 20.
EBI_A21	0: PB5 1: PC9 2: PH9 3: PC7		External Bus Interface (EBI) address output pin 21.
EBI_A22	0: PB6 1: PC10 2: PH10 3: PE4		External Bus Interface (EBI) address output pin 22.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A23	0: PC0 1: PC11 2: PH11 3: PE5		External Bus Interface (EBI) address output pin 23.
EBI_A24	0: PC1 1: PF0 2: PH12 3: PE6		External Bus Interface (EBI) address output pin 24.
EBI_A25	0: PC2 1: PF1 2: PH13 3: PE7		External Bus Interface (EBI) address output pin 25.
EBI_A26	0: PC4 1: PF2 2: PH14 3: PC8		External Bus Interface (EBI) address output pin 26.
EBI_A27	0: PD2 1: PF5 2: PH15 3: PC9		External Bus Interface (EBI) address output pin 27.
EBI_AD00	0: PE8 1: PB0 2: PG0		External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	0: PE9 1: PB1 2: PG1		External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	0: PE10 1: PB2 2: PG2		External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	0: PE11 1: PB3 2: PG3		External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	0: PE12 1: PB4 2: PG4		External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	0: PE13 1: PB5 2: PG5		External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	0: PE14 1: PB6 2: PG6		External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	0: PE15 1: PC0 2: PG7		External Bus Interface (EBI) address and data input / output pin 07.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_TSUTMR-TOG	0: PB6 1: PB15 2: PC3 3: PF9		Ethernet IEEE1588 Timer Toggle.
ETM_TCLK	0: PD7 1: PF8 2: PC6 3: PA6	4: PE11 5: PG15	Embedded Trace Module ETM clock .
ETM_TD0	0: PD6 1: PF9 2: PC7 3: PA2	4: PE12 5: PG14	Embedded Trace Module ETM data 0.
ETM_TD1	0: PD3 1: PD13 2: PD3 3: PA3	4: PE13 5: PG13	Embedded Trace Module ETM data 1.
ETM_TD2	0: PD4 1: PB15 2: PD4 3: PA4	4: PE14 5: PG12	Embedded Trace Module ETM data 2.
ETM_TD3	0: PD5 1: PF3 2: PD5 3: PA5	4: PE15 5: PG11	Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM0_CC2	0: PE6 1: PD14 2: PG4 3: PG10	4: PF1 5: PB2 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0	0: PE10 1: PD15 2: PA12 3: PG11	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1	0: PE11 1: PG0 2: PA13 3: PG12	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	0: PE12 1: PG1 2: PA14 3: PG13	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	4: PE3 5: PE7 6: PH8 7: PH12	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14 1: PD3 2: PD7 3: PE0	4: PE4 5: PI0 6: PH9 7: PH13	Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	0: PD0 1: PD4 2: PD8 3: PE1	4: PE5 5: PI1 6: PH10 7: PH14	Wide timer 1 Capture Compare input / output channel 2.
WTIM1_CC3	0: PD1 1: PD5 2: PC6 3: PE2	4: PE6 5: PI2 6: PH11 7: PH15	Wide timer 1 Capture Compare input / output channel 3.
WTIM2_CC0	0: PA9 1: PA12 2: PB9 3: PB12	4: PG14 5: PD3 6: PH4 7: PH7	Wide timer 2 Capture Compare input / output channel 0.
WTIM2_CC1	0: PA10 1: PA13 2: PB10 3: PG12	4: PG15 5: PD4 6: PH5 7: PH8	Wide timer 2 Capture Compare input / output channel 1.
WTIM2_CC2	0: PA11 1: PA14 2: PB11 3: PG13	4: PH0 5: PD5 6: PH6 7: PH9	Wide timer 2 Capture Compare input / output channel 2.
WTIM3_CC0	0: PD9 1: PC8 2: PC11 3: PC14	4: PI3 5: PI6 6: PB6 7: PF13	Wide timer 3 Capture Compare input / output channel 0.
WTIM3_CC1	0: PD10 1: PC9 2: PC12 3: PF10	4: PI4 5: PI7 6: PF4 7: PF14	Wide timer 3 Capture Compare input / output channel 1.

Table 5.24. ACMP1 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP1Y	BUSACMP1X	Bus
PF14	PF15	PF15	PF14	PB14	PB15	PB15	PB14			CH31
	PF13	PF13			PB13	PB13				CH30
PF12			PF12	PB12			PB12			CH29
	PF11	PF11			PB11	PB11				CH28
PF10			PF10	PB10			PB10			CH27
	PF9	PF9			PB9	PB9				CH26
PF8			PF8							CH25
	PF7	PF7								CH24
PF6			PF6	PB6			PB6			CH23
	PF5	PF5			PB5	PB5				CH22
PF4			PF4	PB4			PB4			CH21
	PF3	PF3			PB3	PB3				CH20
PF2			PF2	PB2			PB2			CH19
	PF1	PF1			PB1	PB1				CH18
PF0			PF0	PB0			PB0			CH17
	PE15	PE15			PA15	PA15				CH16
PE14			PE14	PA14			PA14			CH15
	PE13	PE13			PA13	PA13				CH14
PE12			PE12	PA12			PA12			CH13
	PE11	PE11			PA11	PA11				CH12
PE10			PE10	PA10			PA10			CH11
	PE9	PE9			PA9	PA9				CH10
PE8			PE8	PA8			PA8			CH9
	PE7	PE7			PA7	PA7				CH8
PE6			PE6	PA6			PA6	PC15	PC15	CH7
	PE5	PE5			PA5	PA5		PC14	PC14	CH6
PE4			PE4	PA4			PA4	PC13	PC13	CH5
					PA3	PA3		PC12	PC12	CH4
				PA2			PA2	PC11	PC11	CH3
	PE1	PE1			PA1	PA1		PC10	PC10	CH2
PE0			PE0	PA0			PA0	PC9	PC9	CH1
								PC8	PC8	CH0

Table 5.26. ACMP3 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP3Y	BUSACMP3X	Bus
PF14	PF15	PF15	PF14	PB14	PB15	PB15	PB14			CH31
	PF13	PF13			PB13	PB13				CH30
PF12			PF12	PB12			PB12			CH29
	PF11	PF11			PB11	PB11				CH28
PF10			PF10	PB10			PB10			CH27
	PF9	PF9			PB9	PB9				CH26
PF8			PF8							CH25
	PF7	PF7								CH24
PF6			PF6	PB6			PB6			CH23
	PF5	PF5			PB5	PB5				CH22
PF4			PF4	PB4			PB4			CH21
	PF3	PF3			PB3	PB3				CH20
PF2			PF2	PB2			PB2			CH19
	PF1	PF1			PB1	PB1				CH18
PF0			PF0	PB0			PB0			CH17
	PE15	PE15			PA15	PA15				CH16
PE14			PE14	PA14			PA14			CH15
	PE13	PE13			PA13	PA13				CH14
PE12			PE12	PA12			PA12			CH13
	PE11	PE11			PA11	PA11				CH12
PE10			PE10	PA10			PA10			CH11
	PE9	PE9			PA9	PA9				CH10
PE8			PE8	PA8			PA8			CH9
	PE7	PE7			PA7	PA7				CH8
PE6			PE6	PA6			PA6	PH15	PH15	CH7
	PE5	PE5			PA5	PA5		PH14	PH14	CH6
PE4			PE4	PA4			PA4	PH13	PH13	CH5
					PA3	PA3		PH12	PH12	CH4
				PA2			PA2	PH11	PH11	CH3
	PE1	PE1			PA1	PA1		PH10	PH10	CH2
PE0			PE0	PA0			PA0	PH9	PH9	CH1
								PH8	PH8	CH0

6.2 BGA192 PCB Land Pattern

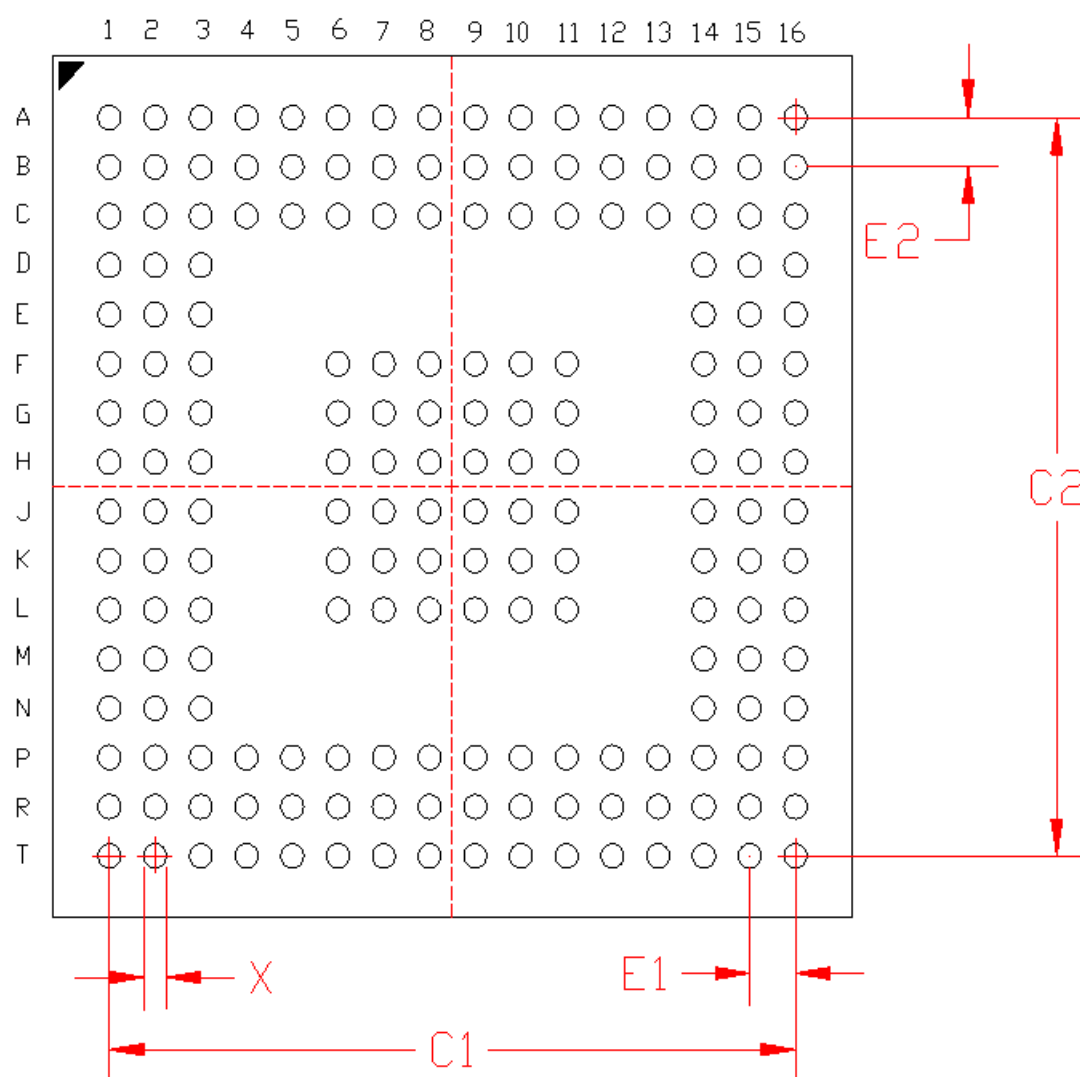


Figure 6.2. BGA192 PCB Land Pattern Drawing

10.2 TQFP100 PCB Land Pattern

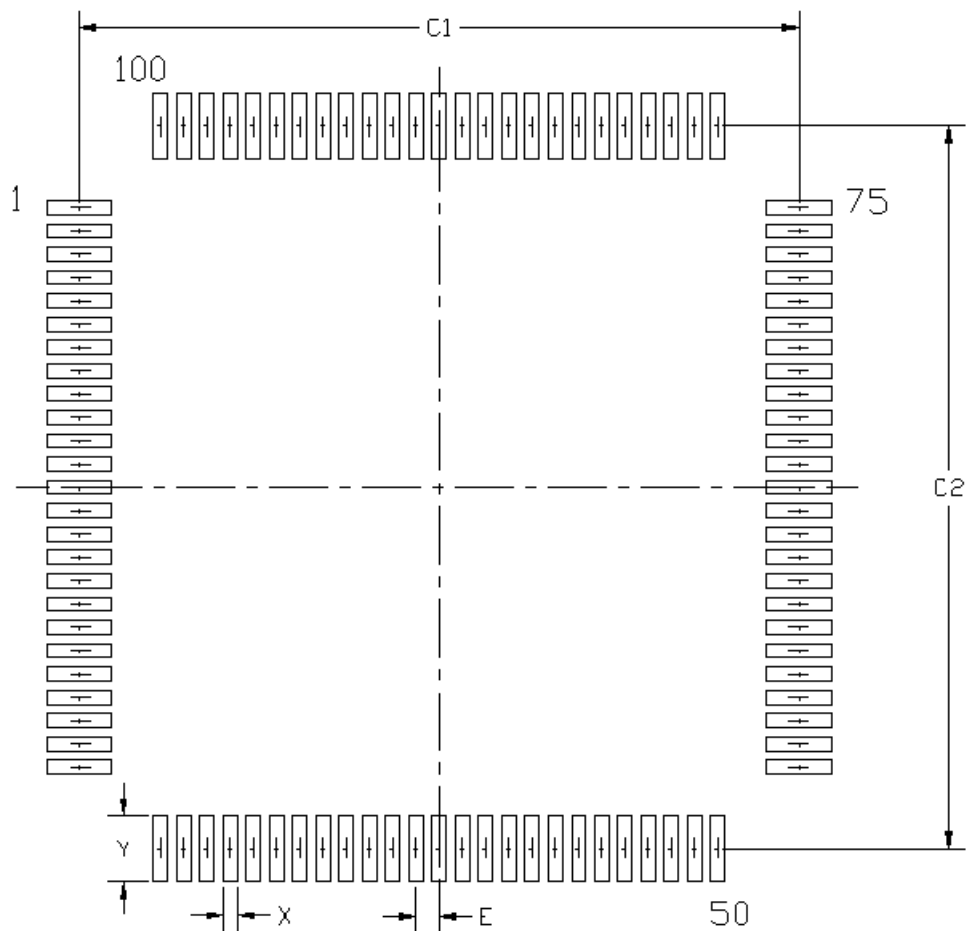


Figure 10.2. TQFP100 PCB Land Pattern Drawing