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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I <sup>2</sup> C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024gm64-br">https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024gm64-br</a>

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## 3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

### 3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

### 3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

### 3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

### 3.6.6 Quad-SPI Flash Controller (QSPI)

The QSPI provides access to a wide range of flash devices with wide I/O busses. The I/O and clocking configuration is flexible and supports many types of devices. Up to 8-bit wide interfaces are supported. The QSPI handles opcodes, status flag polling, and timing configuration automatically.

The external flash memory is mapped directly to internal memory to allow random access to any word in the flash and direct code execution. An integrated instruction cache minimizes latency and allows efficient code execution. Execute in Place (XIP) is supported for devices with this feature.

Large data chunks can be transferred with DMA as efficiently as possible with high throughput and minimal bus load, utilizing an integrated 1 kB SRAM FIFO.

### 3.6.7 SDIO Host Controller (SDIO)

The SDIO is an SD3.01 / SDIO3.0 / eMMC4.51-compliant Host Controller interface for transferring data to and from SD/MMC/SDIO devices. The module conforms to the SD Host Controller Standard Specification Version 3.00. The Host Controller handles SDIO/SD/MMC Protocol at the transmission level, packing data, adding cyclic redundancy check (CRC), Start/End bits, and checking for transaction format correctness.

### 3.6.8 Universal Serial Bus (USB)

The USB is a full-speed/low-speed USB 2.0 compliant host/device controller. The USB can be used in device and host-only configurations, while a clock recovery mechanism allows crystal-less operation in device mode. The USB block supports both full speed (12 MBit/s) and low speed (1.5 MBit/s) operation. When operating as a device, a special Low Energy Mode ensures the current consumption is optimized, enabling USB communications on a strict power budget. The USB device includes an internal dedicated Descriptor-Based Scatter/Gather DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes internal pull-up and pull-down resistors, as well as voltage comparators for monitoring the VBUS voltage and A/B device identification using the ID line.

### 3.6.9 Ethernet (ETH)

The Ethernet peripheral is compliant with IEEE 802.3-2002 for Ethernet MAC. It supports 802.1AS and IEEE 1588 precision clock synchronization protocol, as well as 802.3az Energy Efficient Ethernet. The ETH supports a wide variety of frame formats and standard operating modes such as MII/RMII. Direct Memory Access (DMA) support makes it possible to transmit and receive large frames at high data rates with minimal CPU overhead. The Ethernet peripheral supports 10 Mbps and 100 Mbps operation, and includes a total of 8 kB of dedicated dual-port RAM FIFO (4 kB for TX and 4 kB for RX).

### 3.6.10 Controller Area Network (CAN)

The CAN peripheral provides support for communication at up to 1 Mbps over CAN protocol version 2.0 part A and B. It includes 32 message objects with independent identifier masks and retains message RAM in EM2. Automatic retransmission may be disabled in order to support Time Triggered CAN applications.

### 3.6.11 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

### 3.6.12 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE™ is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

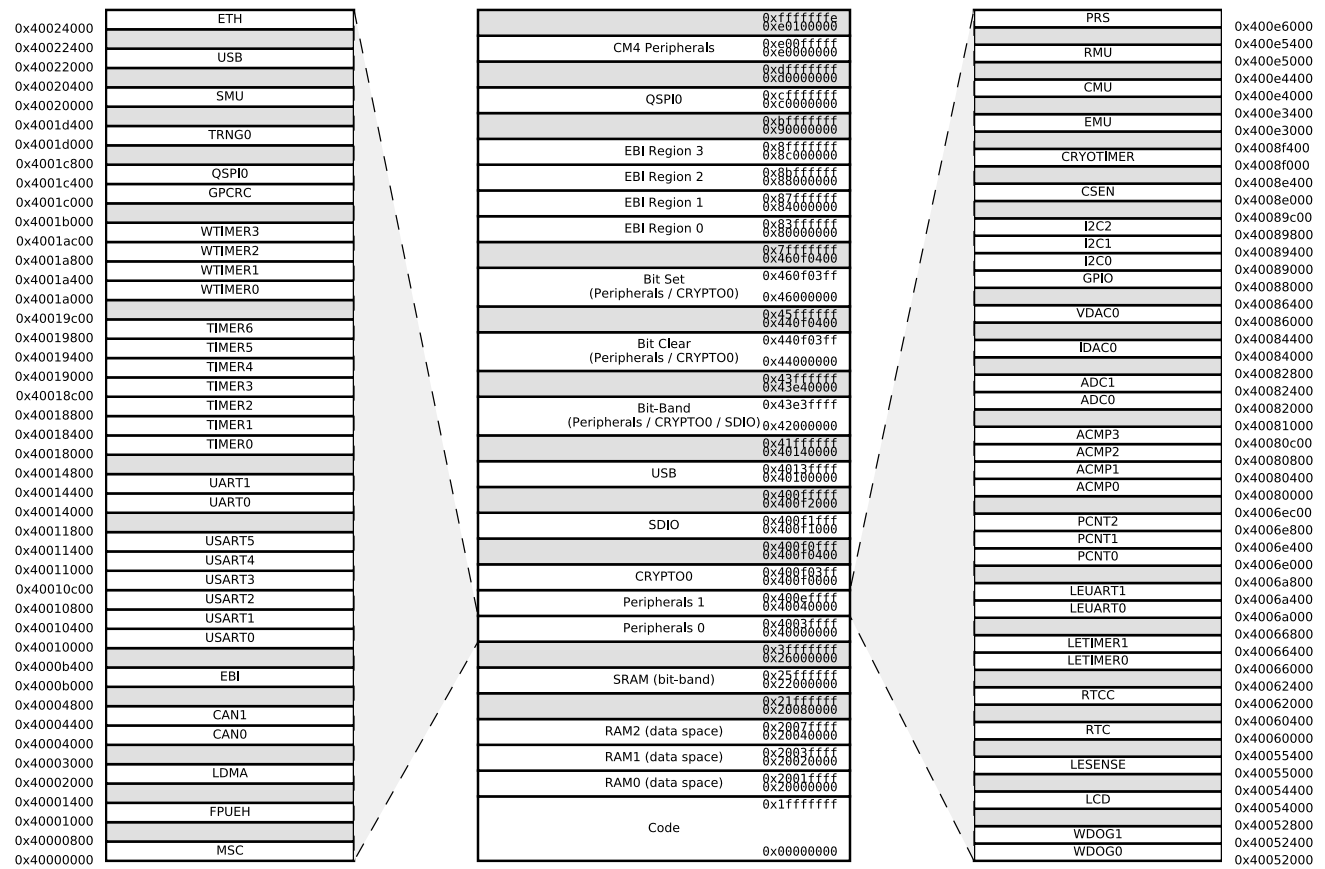


Figure 3.3. EFM32GG11 Memory Map — Peripherals

### 4.1.2.1 General Operating Conditions

**Table 4.2. General Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range <sup>6</sup>	$T_A$	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage <sup>2</sup>	$V_{AVDD}$		1.8	3.3	3.8	V
VREGVDD operating supply voltage <sup>2 1</sup>	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass, $T \leq 85^\circ\text{C}$	—	—	200	mA
		DCDC in bypass, $T > 85^\circ\text{C}$	—	—	100	mA
DVDD operating supply voltage	$V_{DVDD}$		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	$V_{IOVDD}$	All IOVDD pins <sup>5</sup>	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor <sup>3 4</sup>	$C_{DECOUPLE}$		0.75	1.0	2.75	μF
HFCORECLK frequency	$f_{CORE}$	VSCALE2, MODE = WS3	—	—	72	MHz
		VSCALE2, MODE = WS2	—	—	54	MHz
		VSCALE2, MODE = WS1	—	—	36	MHz
		VSCALE2, MODE = WS0	—	—	18	MHz
		VSCALE0, MODE = WS2	—	—	20	MHz
		VSCALE0, MODE = WS1	—	—	14	MHz
		VSCALE0, MODE = WS0	—	—	7	MHz
HFCLK frequency	$f_{HFCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFSRCCLK frequency	$f_{HFSRCCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFBUSCLK frequency	$f_{HFBUSCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERCLK frequency	$f_{HFPERCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERBCLK frequency	$f_{HFPERBCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFPERCCLK frequency	$f_{HFPERCCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz

#### 4.1.10.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Table 4.16. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{\text{AUXHFRCO\_ACC}}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	$t_{\text{AUXHFRCO}}$	$f_{\text{AUXHFRCO}} \geq 19 \text{ MHz}$	—	400	—	ns
		$4 < f_{\text{AUXHFRCO}} < 19 \text{ MHz}$	—	1.4	—	$\mu\text{s}$
		$f_{\text{AUXHFRCO}} \leq 4 \text{ MHz}$	—	2.5	—	$\mu\text{s}$
Current consumption on all supplies	$I_{\text{AUXHFRCO}}$	$f_{\text{AUXHFRCO}} = 50 \text{ MHz}$	—	289	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 48 \text{ MHz}$	—	276	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 38 \text{ MHz}$	—	227	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 32 \text{ MHz}$	—	186	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 26 \text{ MHz}$	—	158	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 19 \text{ MHz}$	—	126	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 16 \text{ MHz}$	—	114	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 13 \text{ MHz}$	—	88	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 7 \text{ MHz}$	—	59	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 4 \text{ MHz}$	—	33	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 2 \text{ MHz}$	—	28	TBD	$\mu\text{A}$
		$f_{\text{AUXHFRCO}} = 1 \text{ MHz}$	—	26	TBD	$\mu\text{A}$
Coarse trim step size (% of period)	$SS_{\text{AUXHFRCO\_COARSE}}$		—	0.8	—	%
Fine trim step size (% of period)	$SS_{\text{AUXHFRCO\_FINE}}$		—	0.1	—	%
Period jitter	$PJ_{\text{AUXHFRCO}}$		—	0.2	—	% RMS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current, continuous conversions, WARMUP-MODE=KEEPCSENWARM	I <sub>CSEN_ACTIVE</sub>	SAR or Delta Modulation conversions of 33 pF capacitor, CS0CG=0 (Gain = 10x), always on	—	90.5	—	μA
HFPERCLK supply current	I <sub>CSEN_HFPERCLK</sub>	Current contribution from HFPERCLK when clock to CSEN block is enabled.	—	2.25	—	μA/MHz

**Note:**

- Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period ( $\text{total\_current} = \text{single\_sample\_current} * (\text{number\_of\_channels} * \text{accumulation})$ ).



#### 4.1.25 External Bus Interface (EBI)

##### EBI Write Enable Output Timing

Timing applies to both EBI\_WEn and EBI\_NANDWEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.36. EBI Write Enable Timing**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_WEn / EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CS <sub>n</sub> , EBI_BL <sub>n</sub> invalid	t <sub>OH_WEn</sub>	IOVDD ≥ 1.62 V	-22 + (WRHOLD * t <sub>HFCOR-ECLK</sub> )	—	—	ns
		IOVDD ≥ 3.0 V	-13 + (WRHOLD * t <sub>HFCOR-ECLK</sub> )	—	—	ns
Output setup time, from EBI_AD, EBI_A, EBI_CS <sub>n</sub> , EBI_BL <sub>n</sub> valid to leading EBI_WEn / EBI_NANDWEn edge <sup>1</sup>	t <sub>OSU_WEn</sub>	IOVDD ≥ 1.62 V	-12 + (WRSET-UP * t <sub>HFCOR-ECLK</sub> )	—	—	ns
		IOVDD ≥ 3.0 V	-10 + (WRSET-UP * t <sub>HFCOR-ECLK</sub> )	—	—	ns
EBI_WEn / EBI_NANDWEn pulse width <sup>1</sup>	t <sub>WIDTH_WEn</sub>	IOVDD ≥ 1.62 V	-6 + (MAX(1, WRSTRB) * t <sub>HFCOR-ECLK</sub> )	—	—	ns
		IOVDD ≥ 3.0 V	-5 + (MAX(1, WRSTRB) * t <sub>HFCOR-ECLK</sub> )	—	—	ns

**Note:**

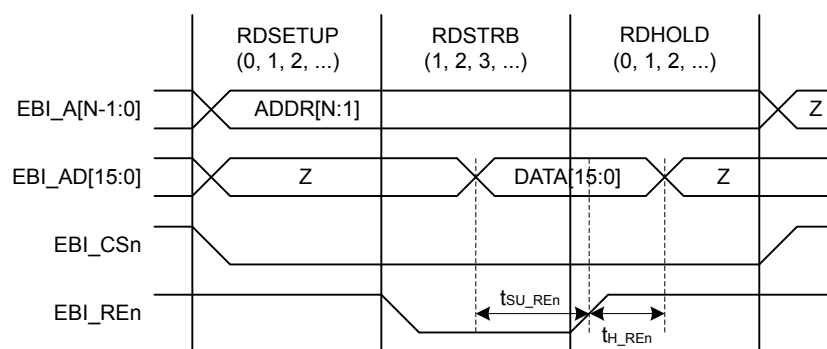
1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI\_WEn can be moved to the right by setting HALFWE=1. This decreases the length of t<sub>WIDTH\_WEn</sub> and increases the length of t<sub>OSU\_WEn</sub> by 1/2 \* t<sub>HFCLKNODIV</sub>.

## EBI Read Enable Timing Requirements

Timing applies to both EBI\_REn and EBI\_NANDREn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.40. EBI Read Enable Timing Requirements**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Setup time, from EBI_AD valid to trailing EBI_REn edge	$t_{SU\_REn}$	IOVDD $\geq$ 1.62 V	55	—	—	ns
		IOVDD $\geq$ 3.0 V	36	—	—	ns
Hold time, from trailing EBI_REn edge to EBI_AD invalid	$t_{H\_REn}$	IOVDD $\geq$ 1.62 V	-9	—	—	ns



**Figure 4.7. EBI Read Enable Timing Requirements**

## 5.9 EFM32GG11B5xx in QFP100 Device Pinout

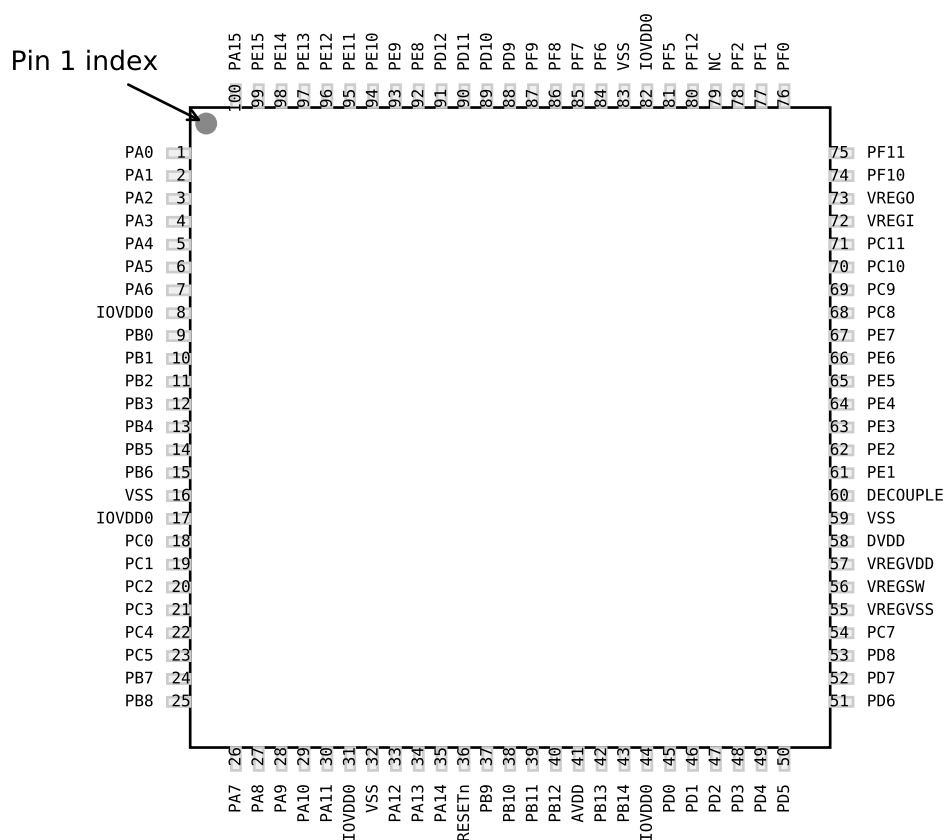


Figure 5.9. EFM32GG11B5xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.9. EFM32GG11B5xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 58 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB9	37	GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41 45	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	46	GPIO (5V)	PD1	47	GPIO
PD2	48	GPIO (5V)	PD3	49	GPIO
PD4	50	GPIO	PD5	51	GPIO
PD6	52	GPIO	PD7	53	GPIO
PD8	54	GPIO	PC6	55	GPIO
PC7	56	GPIO	DVDD	57	Digital power supply.
DECOUPLE	59	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE0	60	GPIO (5V)
PE1	61	GPIO (5V)	PE2	62	GPIO
PE3	63	GPIO	PE4	64	GPIO
PE5	65	GPIO	PE6	66	GPIO
PE7	67	GPIO	PC8	68	GPIO (5V)
PC9	69	GPIO (5V)	PC10	70	GPIO (5V)
PC11	71	GPIO (5V)	PC12	72	GPIO (5V)
PC13	73	GPIO (5V)	PC14	74	GPIO (5V)
PC15	75	GPIO (5V)	PF0	76	GPIO (5V)
PF1	77	GPIO (5V)	PF2	78	GPIO



Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC3	12	GPIO (5V)	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA8	17	GPIO
PA9	18	GPIO	PA10	19	GPIO
RESETn	20	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PC8	41	GPIO (5V)
PC9	42	GPIO (5V)	PC10	43	GPIO (5V)
PC11	44	GPIO (5V)	PC12	45	GPIO (5V)
PC13	46	GPIO (5V)	PC14	47	GPIO (5V)
PC15	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
PF3	52	GPIO	PF4	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A23	0: PC0 1: PC11 2: PH11 3: PE5		External Bus Interface (EBI) address output pin 23.
EBI_A24	0: PC1 1: PF0 2: PH12 3: PE6		External Bus Interface (EBI) address output pin 24.
EBI_A25	0: PC2 1: PF1 2: PH13 3: PE7		External Bus Interface (EBI) address output pin 25.
EBI_A26	0: PC4 1: PF2 2: PH14 3: PC8		External Bus Interface (EBI) address output pin 26.
EBI_A27	0: PD2 1: PF5 2: PH15 3: PC9		External Bus Interface (EBI) address output pin 27.
EBI_AD00	0: PE8 1: PB0 2: PG0		External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	0: PE9 1: PB1 2: PG1		External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	0: PE10 1: PB2 2: PG2		External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	0: PE11 1: PB3 2: PG3		External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	0: PE12 1: PB4 2: PG4		External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	0: PE13 1: PB5 2: PG5		External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	0: PE14 1: PB6 2: PG6		External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	0: PE15 1: PC0 2: PG7		External Bus Interface (EBI) address and data input / output pin 07.

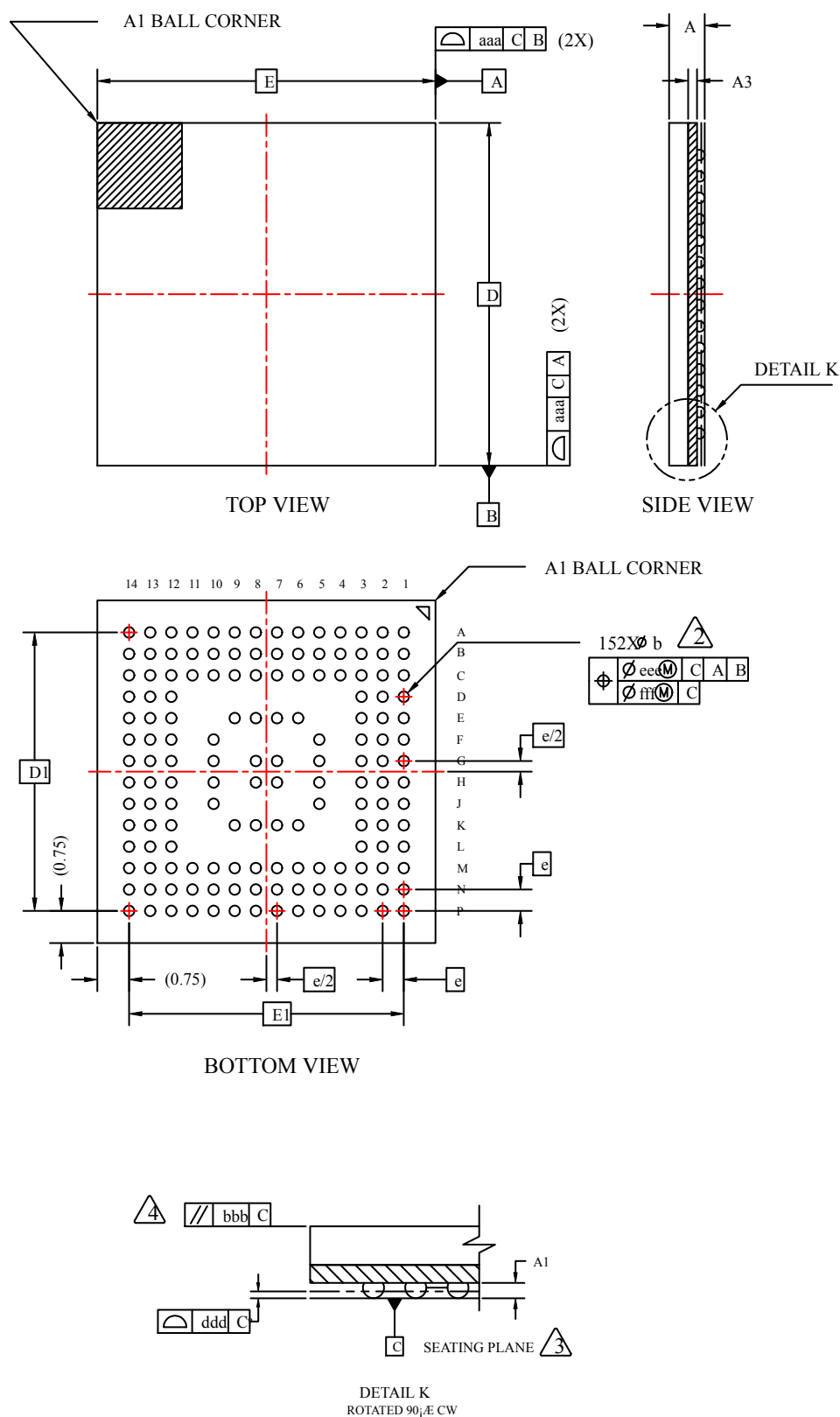
Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_CH11	0: PC11		LESENSE channel 11.
LES_CH12	0: PC12		LESENSE channel 12.
LES_CH13	0: PC13		LESENSE channel 13.
LES_CH14	0: PC14		LESENSE channel 14.
LES_CH15	0: PC15		LESENSE channel 15.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8 7: PB9	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9 7: PB10	Low Energy Timer LETIM0, output channel 1.
LETIM1_OUT0	0: PA7 1: PA11 2: PA12 3: PC2	4: PB5 5: PB2 6: PG0 7: PG2	Low Energy Timer LETIM1, output channel 0.
LETIM1_OUT1	0: PA6 1: PA13 2: PA14 3: PC3	4: PB6 5: PB1 6: PG1 7: PG3	Low Energy Timer LETIM1, output channel 1.
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	0: PC7 1: PA6 2: PD3 3: PB1	4: PB5 5: PH1	LEUART1 Receive input.
LEU1_TX	0: PC6 1: PA5 2: PD2 3: PB0	4: PB4 5: PH0	LEUART1 Transmit output. Also used as receive input in half duplex communication.



Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
U0_TX	0: PF6 1: PE0 2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.
U1_CTS	0: PC14 1: PF9 2: PB11 3: PE4	4: PC4 5: PH13	UART1 Clear To Send hardware flow control input.
U1_RTS	0: PC15 1: PF8 2: PB12 3: PE5	4: PC5 5: PH14	UART1 Request To Send hardware flow control output.
U1_RX	0: PC13 1: PF11 2: PB10 3: PE3	4: PE13 5: PH12	UART1 Receive input.
U1_TX	0: PC12 1: PF10 2: PB9 3: PE2	4: PE12 5: PH11	UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12 6: PG14	USART0 clock input / output.
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13 6: PG15	USART0 chip select input / output.
US0_CTS	0: PE14 1: PE3 2: PC7 3: PC13	4: PB6 5: PB11 6: PH0	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PE15 1: PE2 2: PC6 3: PC12	4: PB5 5: PD6 6: PH1	USART0 Request To Send hardware flow control output.
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1 6: PG13	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0 6: PG12	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4 6: PB2	USART1 chip select input / output.

## 7. BGA152 Package Specifications

## 7.1 BGA152 Package Dimensions



**Figure 7.1. BGA152 Package Drawing**

Table 8.2. BGA120 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.20	
C1		6.00	
C2		6.00	
E1		0.5	
E2		0.5	

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

**Table 9.2. BGA112 PCB Land Pattern Dimensions**

Dimension	Min	Nom	Max
X		0.45	
C1		8.00	
C2		8.00	
E1		0.8	
E2		0.8	

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Table 10.2. TQFP100 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
C1		15.4	
C2		15.4	
E		0.50 BSC	
X		0.30	
Y		1.50	

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This Land Pattern Design is based on the IPC-7351 guidelines.

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

5. The stencil thickness should be 0.125 mm (5 mils).

6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

7. A No-Clean, Type-3 solder paste is recommended.

8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10.3 TQFP100 Package Marking



Figure 10.3. TQFP100 Package Marking

- The package marking consists of:
- P P P P P P P P P P – The part number designation.
  - T T T T T T – A trace or manufacturing code. The first letter is the device revision.
  - Y Y – The last 2 digits of the assembly year.
  - W W – The 2-digit workweek when the device was assembled.