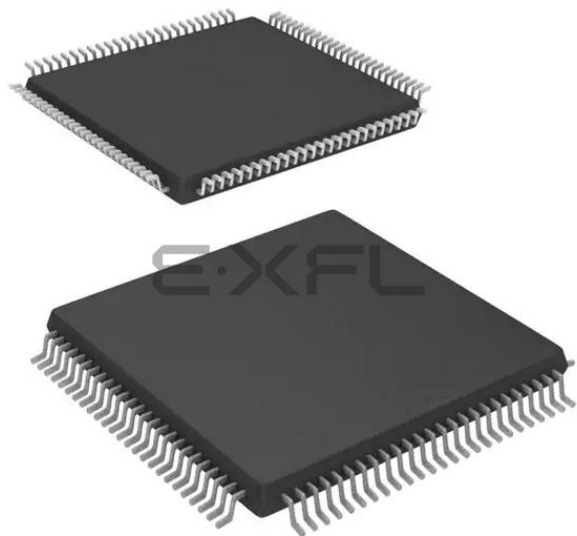




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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024gq100-a

4.1.24 USART SPI

SPI Master Timing

Table 4.34. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period ^{1 3 2}	t _{SCLK}	All USARTs except USART2	2 * t _{HFPERCLK}	—	—	ns
		USART2	2 * t _{HFPERBCLK}	—	—	ns
CS to MOSI ^{1 3}	t _{CS_MO}	USART2, location 4, IOVDD = 1.8 V	-3.2	—	6.8	ns
		USART2, location 4, IOVDD = 3.0 V	-2.3	—	6.0	ns
		USART2, location 5, IOVDD = 1.8 V	-8.1	—	6.3	ns
		USART2, location 5, IOVDD = 3.0 V	-7.3	—	4.4	ns
		All other USARTs and locations, IOVDD = 1.8 V	-15	—	13	ns
		All other USARTs and locations, IOVDD = 3.0 V	-13	—	11	ns
SCLK to MOSI ^{1 3}	t _{SCLK_MO}	USART2, location 4, IOVDD = 1.8 V	-0.3	—	9.2	ns
		USART2, location 4, IOVDD = 3.0 V	-0.3	—	8.6	ns
		USART2, location 5, IOVDD = 1.8 V	-3.6	—	5.0	ns
		USART2, location 5, IOVDD = 3.0 V	-3.4	—	3.2	ns
		All other USARTs and locations, IOVDD = 1.8 V	-10	—	11	ns
		All other USARTs and locations, IOVDD = 3.0 V	-9	—	11	ns
MISO setup time ^{1 3}	t _{SU_MI}	USART2, location 4, IOVDD = 1.8 V	39.7	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	22.4	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	49.2	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	30.0	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	55	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	36	—	—	ns

4.1.25 External Bus Interface (EBI)

EBI Write Enable Output Timing

Timing applies to both EBI_WEn and EBI_NANDWEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.36. EBI Write Enable Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_WEn / EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CS _n , EBI_BL _n invalid	t _{OH_WEn}	IOVDD ≥ 1.62 V	-22 + (WRHOLD * t _{HFCOR-ECLK})	—	—	ns
		IOVDD ≥ 3.0 V	-13 + (WRHOLD * t _{HFCOR-ECLK})	—	—	ns
Output setup time, from EBI_AD, EBI_A, EBI_CS _n , EBI_BL _n valid to leading EBI_WEn / EBI_NANDWEn edge ¹	t _{OSU_WEn}	IOVDD ≥ 1.62 V	-12 + (WRSET-UP * t _{HFCOR-ECLK})	—	—	ns
		IOVDD ≥ 3.0 V	-10 + (WRSET-UP * t _{HFCOR-ECLK})	—	—	ns
EBI_WEn / EBI_NANDWEn pulse width ¹	t _{WIDTH_WEn}	IOVDD ≥ 1.62 V	-6 + (MAX(1, WRSTRB) * t _{HFCOR-ECLK})	—	—	ns
		IOVDD ≥ 3.0 V	-5 + (MAX(1, WRSTRB) * t _{HFCOR-ECLK})	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of t_{WIDTH_WEn} and increases the length of t_{OSU_WEn} by 1/2 * t_{HFCLKNODIV}.

4.1.26 Ethernet (ETH)

MII Transmit Timing

Timing is specified with $3.0\text{ V} \leq \text{IOVDD} \leq 3.8\text{ V}$, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.42. Ethernet MII Transmit Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX_CLK frequency	$F_{\text{TX_CLK}}$	Output slew rate set to 7	—	25	—	MHz
TX_CLK duty cycle	$DC_{\text{TX_CLK}}$		35	—	65	%
Output delay, TX_CLK to TXD[3:0], TX_EN, TX_ER	t_{OUT}		0	—	25	ns

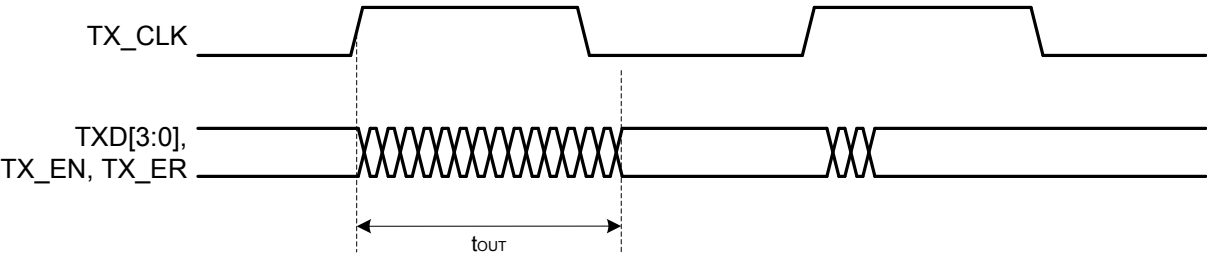
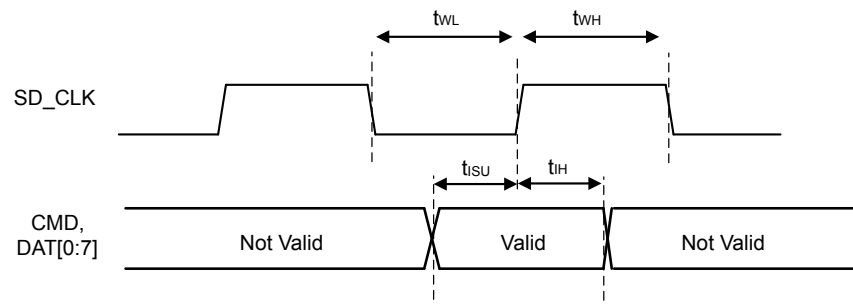
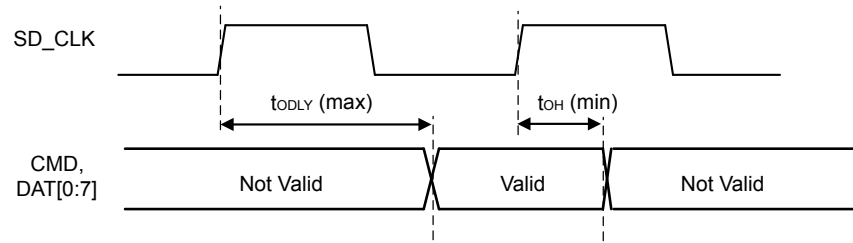


Figure 4.9. Ethernet MII Transmit Timing



Input Timing



Output Timing

Figure 4.15. SDIO SDR Mode Timing

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
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Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE8	B4	GPIO	PD11	B5	GPIO
PF8	B6	GPIO	PF6	B7	GPIO
PF3	B8	GPIO	PE5	B9	GPIO
PC12	B10	GPIO (5V)	PC13	B11	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
PD12	C5	GPIO	PF9	C6	GPIO
VSS	C7 D4 F9 G3 G9 H6 K4 K7 K10 L7	Ground	PF2	C8	GPIO
PE6	C9	GPIO	PC10	C10	GPIO (5V)
PC11	C11	GPIO (5V)	PA3	D1	GPIO
PA2	D2	GPIO	PB15	D3	GPIO (5V)
IOVDD1	D5	Digital IO power supply 1.	PD9	D6	GPIO
IOVDD0	D7 G8 H7 L4	Digital IO power supply 0.	PF1	D8	GPIO (5V)
PE7	D9	GPIO	PC8	D10	GPIO (5V)
PC9	D11	GPIO (5V)	PA6	E1	GPIO
PA5	E2	GPIO	PA4	E3	GPIO
PB0	E4	GPIO	PF0	E8	GPIO (5V)
PE0	E9	GPIO (5V)	PE1	E10	GPIO (5V)
PE3	E11	GPIO	PB1	F1	GPIO
PB2	F2	GPIO	PB3	F3	GPIO
PB4	F4	GPIO	DVDD	F8	Digital power supply.
PE2	F10	GPIO	DECOUPLE	F11	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
PB5	G1	GPIO	PB6	G2	GPIO
IOVDD2	G4	Digital IO power supply 2.	PC6	G10	GPIO
PC7	G11	GPIO	PC0	H1	GPIO (5V)
PC2	H2	GPIO (5V)	PD14	H3	GPIO (5V)
PA7	H4	GPIO	PA8	H5	GPIO
PD8	H8	GPIO	PD5	H9	GPIO
PD6	H10	GPIO	PD7	H11	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF2	78	GPIO	VBUS	79	USB VBUS signal and auxiliary input to 5 V regulator.
PF12	80	GPIO	PF5	81	GPIO
PF6	84	GPIO	PF7	85	GPIO
PF8	86	GPIO	PF9	87	GPIO
PD9	88	GPIO	PD10	89	GPIO
PD11	90	GPIO	PD12	91	GPIO
PE8	92	GPIO	PE9	93	GPIO
PE10	94	GPIO	PE11	95	GPIO
PE12	96	GPIO	PE13	97	GPIO
PE14	98	GPIO	PE15	99	GPIO
PA15	100	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.9 EFM32GG11B5xx in QFP100 Device Pinout

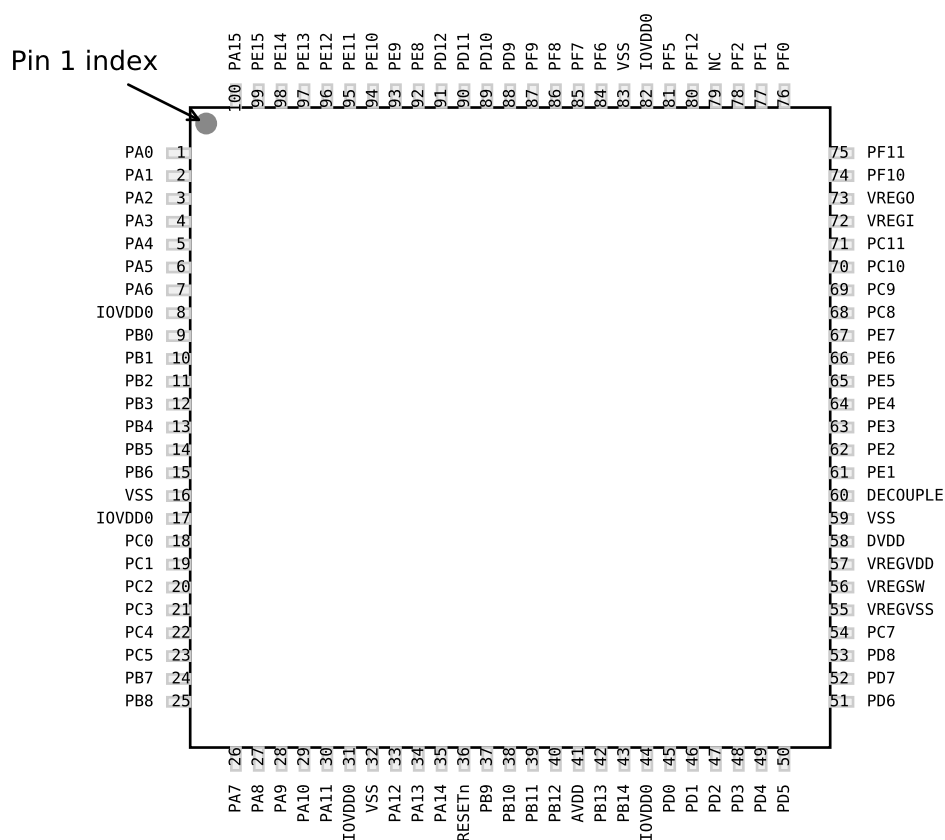


Figure 5.9. EFM32GG11B5xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.9. EFM32GG11B5xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

5.18 EFM32GG11B4xx in QFN64 Device Pinout

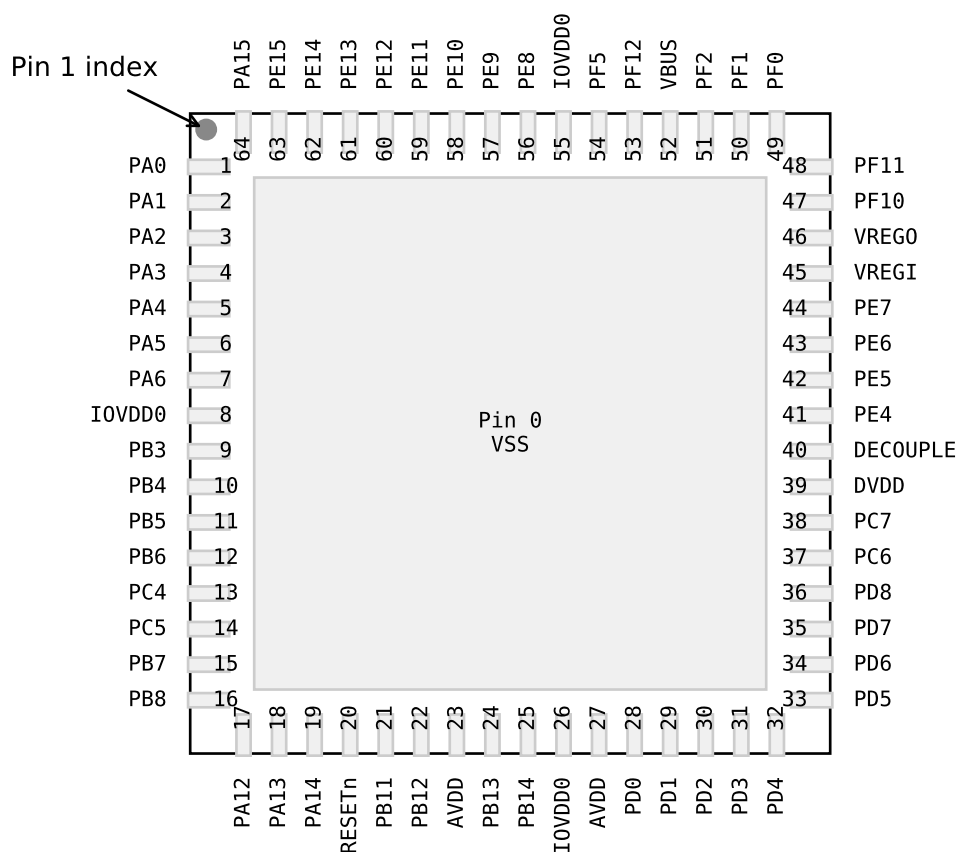


Figure 5.18. EFM32GG11B4xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.18. EFM32GG11B4xx in QFN64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 26 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD4	BUSADC0Y BU-SADC0X OPA2_P	EBI_A08 #1 EBI_A17 #3	TIM6_CC0 #7 WTIM0_CDTI0 #4 WTIM1_CC2 #1 WTIM2_CC1 #5	CAN1_TX #2 US1_CTS #1 US3_CLK #2 LEU0_TX #0 I2C1_SDA #3	CMU_CLKI0 #0 PRS_CH10 #2 ETM_TD2 #0 ETM_TD2 #2
PC0	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSACMP0Y BU-SACMP0X	EBI_AD07 #1 EBI_CS0 #2 EBI_REn #3 EBI_A23 #0	TIM0_CC1 #3 TIM2_CC1 #4 PCNT0_S0IN #2	ETH_MDIO #2 CAN0_RX #0 US0_TX #5 US1_TX #0 US1_CS #4 US2_RTS #0 US3_CS #3 I2C0_SDA #4	LES_CH0 PRS_CH2 #0
PC1	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSACMP0Y BU-SACMP0X	EBI_AD08 #1 EBI_CS1 #2 EBI_BL0 #3 EBI_A24 #0	TIM0_CC2 #3 TIM2_CC2 #4 WTIM0_CC0 #7 PCNT0_S1IN #2	ETH_MDC #2 CAN0_TX #0 US0_RX #5 US1_TX #4 US1_RX #0 US2_CTS #0 US3_RTS #1 I2C0_SCL #4	LES_CH1 PRS_CH3 #0
PC2	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSACMP0Y BU-SACMP0X	EBI_AD09 #1 EBI_CS2 #2 EBI_NANDWEn #3 EBI_A25 #0	TIM0_CDTI0 #3 TIM2_CC0 #5 WTIM0_CC1 #7 LE-TIM1_OUT0 #3	ETH_TSUEXTCLK #2 CAN1_RX #0 US1_RX #4 US2_TX #0	LES_CH2 PRS_CH10 #1
PA8	BUSBY BUSAX LCD_SEG36	EBI_AD14 #1 EBI_A02 #3 EBI_DCLK #0	TIM2_CC0 #0 TIM0_CC0 #6 LE-TIM0_OUT0 #6 PCNT1_S1IN #4	US2_RX #2 US4_RTS #0	PRS_CH8 #0
PA11	BUSAY BUSBX LCD_SEG39	EBI_CS1 #1 EBI_A05 #3 EBI_HSNC #0	WTIM2_CC2 #0 LE-TIM1_OUT0 #1	US2_CTS #2	PRS_CH11 #0
PA13	BUSAY BUSBX	EBI_WEn #1 EBI_NANDWEn #2 EBI_A01 #0 EBI_A07 #3	TIM0_CC2 #7 TIM2_CC1 #1 WTIM0_CDTI1 #2 WTIM2_CC1 #1 LE-TIM1_OUT1 #1 PCNT1_S1IN #5	CAN1_TX #5 US0_CS #5 US2_TX #3	PRS_CH13 #0
PB9	BUSAY BUSBX	EBI_ALE #1 EBI_NANDREn #2 EBI_A00 #1 EBI_A03 #0 EBI_A09 #3	WTIM2_CC0 #2 LE-TIM0_OUT0 #7	SDIO_WP #3 CAN0_RX #3 US1_CTS #0 U1_TX #2	PRS_CH13 #1 ACMP1_O #5
PB12	BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT	EBI_A03 #1 EBI_A12 #3 EBI_CSTFT #2	TIM1_CC3 #3 WTIM2_CC0 #3 LE-TIM0_OUT1 #1 PCNT0_S0IN #7 PCNT1_S1IN #6	US2_CTS #1 US5_RTS #0 U1_RTS #2 I2C1_SCL #1	PRS_CH16 #1
PH2	BUSADC1Y BU-SADC1X	EBI_VSNC #2	TIM6_CC0 #3	US1_CTS #6	
PH5	BUSADC1Y BU-SADC1X	EBI_A17 #2	TIM6_CDTI0 #3 WTIM2_CC1 #6	US4_RX #4	
PH8	BUSACMP3Y BU-SACMP3X	EBI_A20 #2	TIM6_CC0 #4 WTIM1_CC0 #6 WTIM2_CC1 #7	US4_CTS #4	

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_MIITXD2	0: PA2 1: PG2		Ethernet MII Transmit Data Bit 2.
ETH_MIITXD3	0: PA1 1: PG1		Ethernet MII Transmit Data Bit 3.
ETH_MIITXEN	0: PA5 1: PG5		Ethernet MII Transmit Enable.
ETH_MIITXER	0: PA6 1: PG6		Ethernet MII Transmit Error.
ETH_RMIICRSDV	0: PA4 1: PD11		Ethernet RMII Carrier Sense / Data Valid.
ETH_RMIIREFCLK	0: PA3 1: PD10		Ethernet RMII Reference Clock.
ETH_RMIIRXD0	0: PA2 1: PD9		Ethernet RMII Receive Data Bit 0.
ETH_RMIIRXD1	0: PA1 1: PF9		Ethernet RMII Receive Data Bit 1.
ETH_RMIIRXER	0: PA5 1: PD12		Ethernet RMII Receive Error.
ETH_RMIITXD0	0: PE15 1: PF7		Ethernet RMII Transmit Data Bit 0.
ETH_RMIITXD1	0: PE14 1: PF6		Ethernet RMII Transmit Data Bit 1.
ETH_RMIITXEN	0: PA0 1: PF8		Ethernet RMII Transmit Enable.
ETH_TSUEXTCLK	0: PB5 1: PD15 2: PC2 3: PF8		Ethernet IEEE1588 External Reference Clock.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM4_CDTI2	0: PD3		Timer 4 Complimentary Dead Time Insertion channel 2.
TIM5_CC0	0: PE4 1: PE7 2: PH13 3: PI0	4: PC8 5: PC11 6: PC14 7: PF12	Timer 5 Capture Compare input / output channel 0.
TIM5_CC1	0: PE5 1: PH11 2: PH14 3: PI1	4: PC9 5: PC12 6: PF10 7: PF13	Timer 5 Capture Compare input / output channel 1.
TIM5_CC2	0: PE6 1: PH12 2: PH15 3: PI2	4: PC10 5: PC13 6: PF11 7: PF14	Timer 5 Capture Compare input / output channel 2.
TIM6_CC0	0: PG0 1: PG6 2: PG12 3: PH2	4: PH8 5: PB13 6: PD1 7: PD4	Timer 6 Capture Compare input / output channel 0.
TIM6_CC1	0: PG1 1: PG7 2: PG13 3: PH3	4: PH9 5: PB14 6: PD2 7: PD5	Timer 6 Capture Compare input / output channel 1.
TIM6_CC2	0: PG2 1: PG8 2: PG14 3: PH4	4: PH10 5: PD0 6: PD3 7: PD6	Timer 6 Capture Compare input / output channel 2.
TIM6_CDTI0	0: PG3 1: PG9 2: PE4 3: PH5		Timer 6 Complimentary Dead Time Insertion channel 0.
TIM6_CDTI1	0: PG4 1: PG10 2: PE5 3: PH6		Timer 6 Complimentary Dead Time Insertion channel 1.
TIM6_CDTI2	0: PG5 1: PG11 2: PE6 3: PH7		Timer 6 Complimentary Dead Time Insertion channel 2.
U0_CTS	0: PF8 1: PE2 2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.
U0_RTS	0: PF9 1: PE3 2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	0: PF7 1: PE1 2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.

Table 5.25. ACMP2 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP2Y	BUSACMP2X	Bus
PF14	PF15	PF15	PF14	PB14	PB15	PB15	PB14			CH31
	PF13	PF13			PB13	PB13				CH30
PF12			PF12	PB12			PB12			CH29
	PF11	PF11			PB11	PB11				CH28
PF10			PF10	PB10			PB10			CH27
	PF9	PF9			PB9	PB9				CH26
PF8			PF8							CH25
	PF7	PF7								CH24
PF6			PF6	PB6			PB6			CH23
	PF5	PF5			PB5	PB5				CH22
PF4			PF4	PB4			PB4			CH21
	PF3	PF3			PB3	PB3				CH20
PF2			PF2	PB2			PB2			CH19
	PF1	PF1			PB1	PB1				CH18
PF0			PF0	PB0			PB0			CH17
	PE15	PE15			PA15	PA15				CH16
PE14			PE14	PA14			PA14			CH15
	PE13	PE13			PA13	PA13				CH14
PE12			PE12	PA12			PA12			CH13
	PE11	PE11			PA11	PA11				CH12
PE10			PE10	PA10			PA10			CH11
	PE9	PE9			PA9	PA9				CH10
PE8			PE8	PA8			PA8			CH9
	PE7	PE7			PA7	PA7		PG7	PG7	CH8
PE6			PE6	PA6			PA6	PG6	PG6	CH7
	PE5	PE5			PA5	PA5		PG5	PG5	CH6
PE4			PE4	PA4			PA4	PG4	PG4	CH5
					PA3	PA3		PG3	PG3	CH4
				PA2			PA2	PG2	PG2	CH3
	PE1	PE1			PA1	PA1		PG1	PG1	CH2
PE0			PE0	PA0			PA0	PG0	PG0	CH1
										CH0

Table 5.29. CSEN Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																												
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	APORT1X	APORT1Y	APORT3X	APORT3Y	BUSCX	BUSCY	PF15	PF14	PF13	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
	BUSCX	BUSCY	BUSCX	BUSCY	BUSCX	BUSCY	PF15	PF14	PF13	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
	BUSCX	BUSCY	BUSCX	BUSCY	BUSCX	BUSCY	PF15	PF14	PF13	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																							
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	APORT4Y	APORT4X	APORT2Y	APORT2X	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY	BUSDY

Table 5.30. IDAC0 Bus and Pin Mapping

APORT1Y	APORT1X	Port
BUSCY	BUSCX	Bus
PF15		CH31
	PF14	CH30
PF13		CH29
	PF12	CH28
PF11		CH27
	PF10	CH26
PF9		CH25
	PF8	CH24
PF7		CH23
	PF6	CH22
PF5		CH21
	PF4	CH20
PF3		CH19
	PF2	CH18
PF1		CH17
	PF0	CH16
PE15		CH15
	PE14	CH14
PE13		CH13
	PE12	CH12
PE11		CH11
	PE10	CH10
PE9		CH9
	PE8	CH8
PE7		CH7
	PE6	CH6
PE5		CH5
	PE4	CH4
		CH3
		CH2
PE1		CH1
	PE0	CH0

Table 8.2. BGA120 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.20	
C1		6.00	
C2		6.00	
E1		0.5	
E2		0.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8.3 BGA120 Package Marking



Figure 8.3. BGA120 Package Marking

The package marking consists of:

- P P P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code. The first letter is the device revision.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.

10. TQFP100 Package Specifications

10.1 TQFP100 Package Dimensions

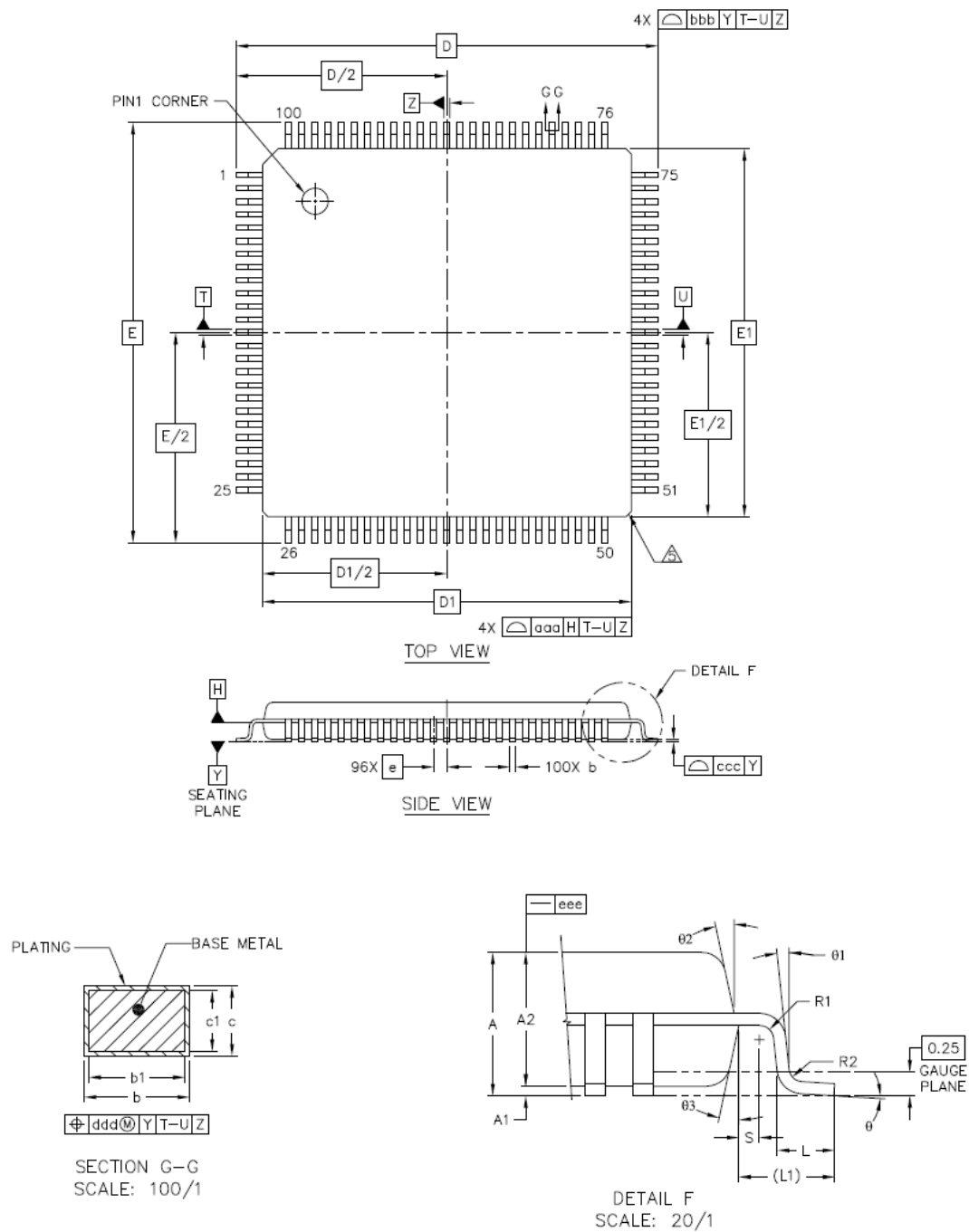


Figure 10.1. TQFP100 Package Drawing

11.2 TQFP64 PCB Land Pattern

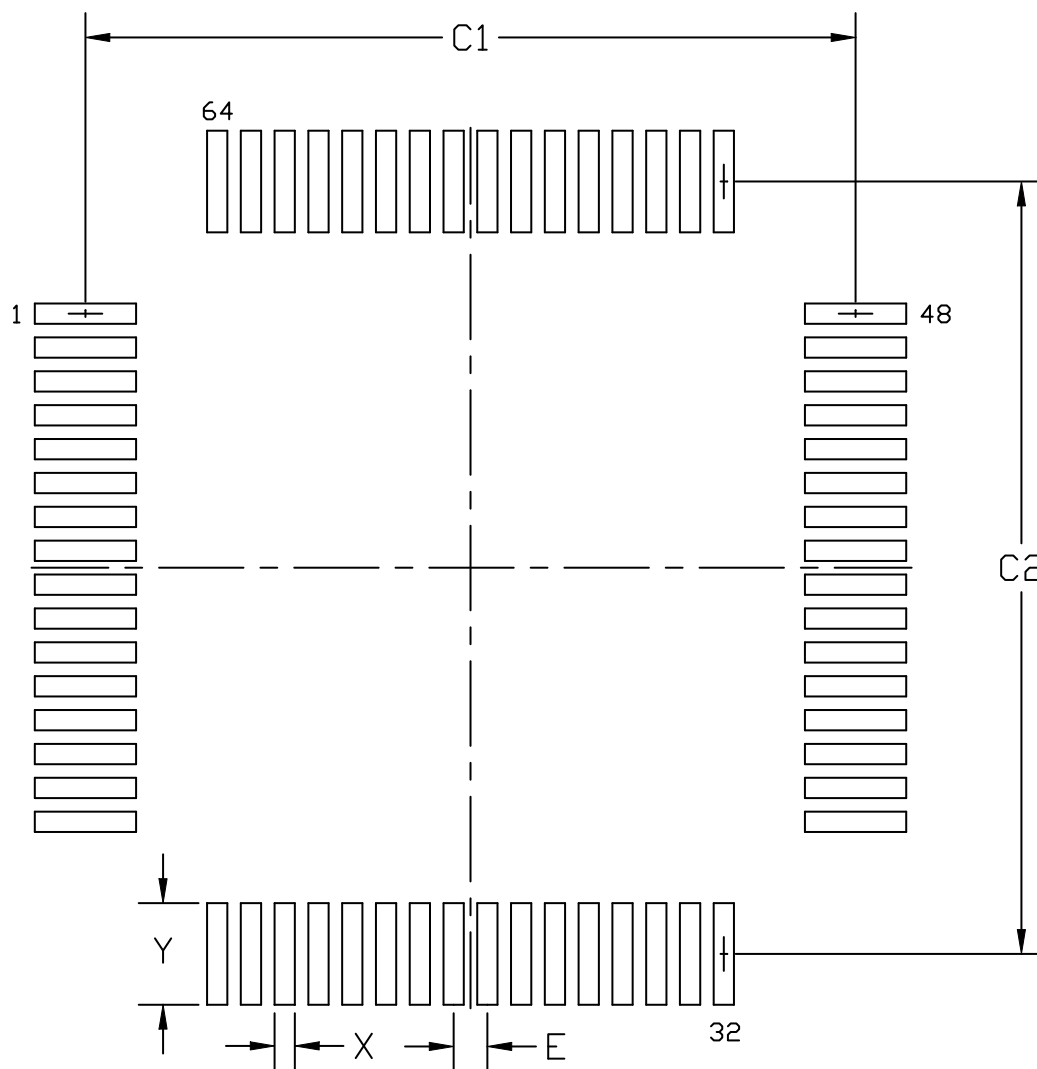


Figure 11.2. TQFP64 PCB Land Pattern Drawing

Table 11.2. TQFP64 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

- Note:**
- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
 - 2. This Land Pattern Design is based on the IPC-7351 guidelines.
 - 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
 - 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
 - 5. The stencil thickness should be 0.125 mm (5 mils).
 - 6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
 - 7. A No-Clean, Type-3 solder paste is recommended.
 - 8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11.3 TQFP64 Package Marking



Figure 11.3. TQFP64 Package Marking

- The package marking consists of:
- P – The part number designation.
 - T – A trace or manufacturing code. The first letter is the device revision.
 - Y – The last 2 digits of the assembly year.
 - W – The 2-digit workweek when the device was assembled.

Table 12.1. QFN64 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	—	0.05
b	0.20	0.25	0.30
A3	0.203 REF		
D	9.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
D2	7.10	7.20	7.30
E2	7.10	7.20	7.30
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.