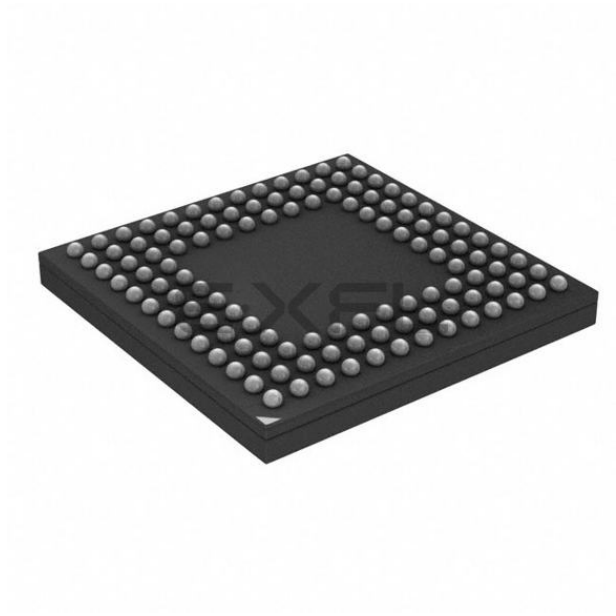

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 95 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.8V |
| Data Converters | A/D 16x12b SAR; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 120-VFBGA |
| Supplier Device Package | 120-BGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024il120-a |

| Ordering Code | Flash (kB) | RAM (kB) | DC-DC Converter | USB | Ethernet | QSPI | SDIO | LCD | GPIO | Package | Temp Range |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EFM32GG11B520F2048GQ64-A | 2048 | 512 | Yes | No | No | No | No | Yes | 50 | QFP64 | -40 to +85°C |
| EFM32GG11B510F2048GQ64-A | 2048 | 384 | Yes | No | No | No | No | Yes | 50 | QFP64 | -40 to +85°C |
| EFM32GG11B520F2048GM64-A | 2048 | 512 | Yes | No | No | No | No | Yes | 53 | QFN64 | -40 to +85°C |
| EFM32GG11B510F2048GM64-A | 2048 | 384 | Yes | No | No | No | No | Yes | 53 | QFN64 | -40 to +85°C |
| EFM32GG11B520F2048IQ64-A | 2048 | 512 | Yes | No | No | No | No | Yes | 50 | QFP64 | -40 to +125°C |
| EFM32GG11B510F2048IQ64-A | 2048 | 384 | Yes | No | No | No | No | Yes | 50 | QFP64 | -40 to +125°C |
| EFM32GG11B520F2048IM64-A | 2048 | 512 | Yes | No | No | No | No | Yes | 53 | QFN64 | -40 to +125°C |
| EFM32GG11B510F2048IM64-A | 2048 | 384 | Yes | No | No | No | No | Yes | 53 | QFN64 | -40 to +125°C |
| EFM32GG11B420F2048GL120-A | 2048 | 512 | No | Yes | Yes | Yes | Yes | Yes | 93 | BGA120 | -40 to +85°C |
| EFM32GG11B420F2048IL120-A | 2048 | 512 | No | Yes | Yes | Yes | Yes | Yes | 93 | BGA120 | -40 to +125°C |
| EFM32GG11B420F2048GL112-A | 2048 | 512 | No | Yes | Yes | Yes | Yes | Yes | 87 | BGA112 | -40 to +85°C |
| EFM32GG11B420F2048IL112-A | 2048 | 512 | No | Yes | Yes | Yes | Yes | Yes | 87 | BGA112 | -40 to +125°C |
| EFM32GG11B420F2048GQ100-A | 2048 | 512 | No | Yes | Yes | Yes | Yes | Yes | 83 | QFP100 | -40 to +85°C |
| EFM32GG11B420F2048IQ100-A | 2048 | 512 | No | Yes | Yes | Yes | Yes | Yes | 83 | QFP100 | -40 to +125°C |
| EFM32GG11B420F2048GQ64-A | 2048 | 512 | No | Yes | Yes | Yes | Yes | Yes | 50 | QFP64 | -40 to +85°C |
| EFM32GG11B420F2048GM64-A | 2048 | 512 | No | Yes | Yes | Yes | Yes | Yes | 53 | QFN64 | -40 to +85°C |
| EFM32GG11B420F2048IQ64-A | 2048 | 512 | No | Yes | Yes | Yes | Yes | Yes | 50 | QFP64 | -40 to +125°C |
| EFM32GG11B420F2048IM64-A | 2048 | 512 | No | Yes | Yes | Yes | Yes | Yes | 53 | QFN64 | -40 to +125°C |
| EFM32GG11B320F2048GL112-A | 2048 | 512 | No | No | No | No | No | Yes | 90 | BGA112 | -40 to +85°C |
| EFM32GG11B310F2048GL112-A | 2048 | 384 | No | No | No | No | No | Yes | 90 | BGA112 | -40 to +85°C |
| EFM32GG11B320F2048GQ100-A | 2048 | 512 | No | No | No | No | No | Yes | 86 | QFP100 | -40 to +85°C |
| EFM32GG11B310F2048GQ100-A | 2048 | 384 | No | No | No | No | No | Yes | 86 | QFP100 | -40 to +85°C |
| EFM32GG11B120F2048GQ64-A | 2048 | 512 | No | No | No | No | No | No | 53 | QFP64 | -40 to +85°C |
| EFM32GG11B110F2048GQ64-A | 2048 | 384 | No | No | No | No | No | No | 53 | QFP64 | -40 to +85°C |
| EFM32GG11B120F2048GM64-A | 2048 | 512 | No | No | No | No | No | No | 56 | QFN64 | -40 to +85°C |
| EFM32GG11B110F2048GM64-A | 2048 | 384 | No | No | No | No | No | No | 56 | QFN64 | -40 to +85°C |
| EFM32GG11B120F2048IQ64-A | 2048 | 512 | No | No | No | No | No | No | 53 | QFP64 | -40 to +125°C |
| EFM32GG11B110F2048IQ64-A | 2048 | 384 | No | No | No | No | No | No | 53 | QFP64 | -40 to +125°C |
| EFM32GG11B120F2048IM64-A | 2048 | 512 | No | No | No | No | No | No | 56 | QFN64 | -40 to +125°C |
| EFM32GG11B110F2048IM64-A | 2048 | 384 | No | No | No | No | No | No | 56 | QFN64 | -40 to +125°C |

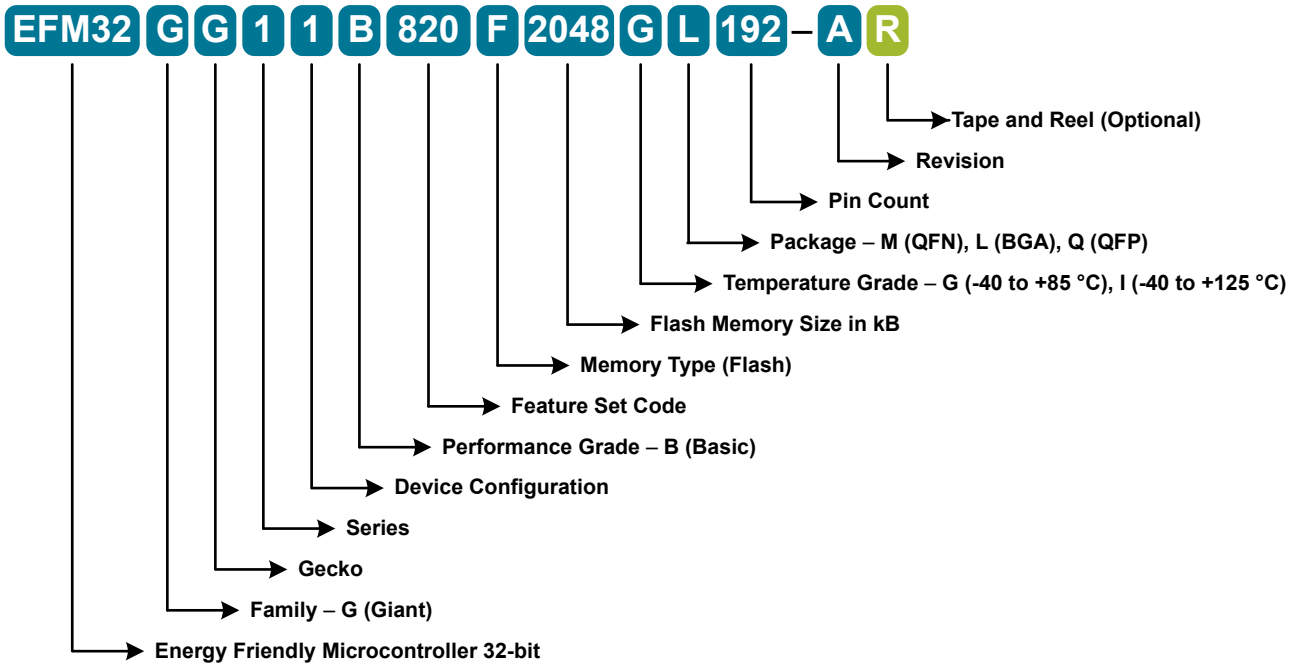


**Figure 2.1. Ordering Code Key**

### 3.11 Memory Map

The EFM32GG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

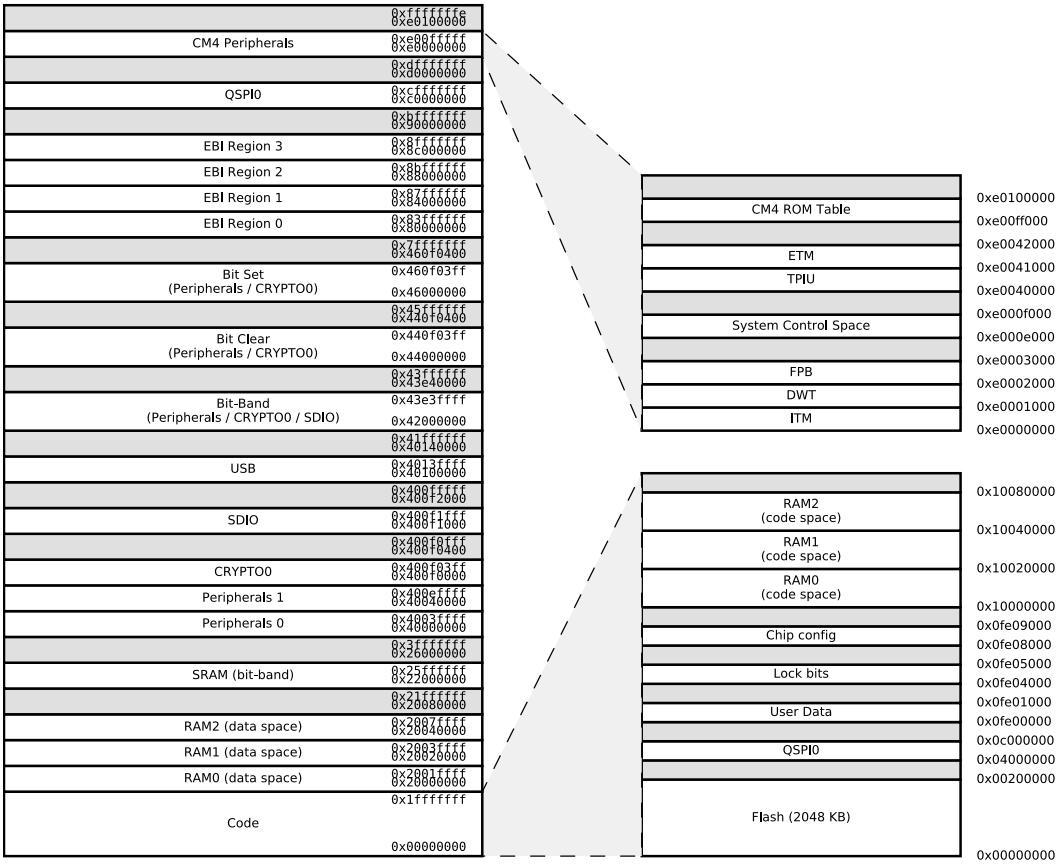


**Figure 3.2. EFM32GG11 Memory Map — Core Peripherals and Code Space**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|

**Note:**

1. The minimum voltage required in bypass mode is calculated using $R_{BYP}$ from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV / usec for approximately 20 usec. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
5. When the CSEN peripheral is used with chopping enabled (CSEN_CTRL_CHOPEN = ENABLE), IOVDD must be equal to AVDD.
6. The maximum limit on $T_A$ may be lower due to device self-heating, which depends on the power dissipation of the specific application. $T_A$ (max) = $T_J$ (max) - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for $T_J$ and $THETA_{JA}$.

### 4.1.3 Thermal Characteristics

**Table 4.3. Thermal Characteristics**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal resistance, QFN64 Package | $THETA_{JA\_QFN64}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 17.8 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 15.4 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 13.8 | — | °C/W |
| Thermal resistance, TQFP64 Package | $THETA_{JA\_TQFP64}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 33.9 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 32.1 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 30.1 | — | °C/W |
| Thermal resistance, TQFP100 Package | $THETA_{JA\_TQFP100}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 44.1 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 37.7 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 35.5 | — | °C/W |
| Thermal resistance, BGA112 Package | $THETA_{JA\_BGA112}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 42.0 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 37.0 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 35.3 | — | °C/W |
| Thermal resistance, BGA120 Package | $THETA_{JA\_BGA120}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 47.9 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 41.8 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 39.6 | — | °C/W |
| Thermal resistance, BGA152 Package | $THETA_{JA\_BGA152}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 35.7 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 31.0 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 29.5 | — | °C/W |
| Thermal resistance, BGA192 Package | $THETA_{JA\_BGA192}$ | 4-Layer PCB, Air velocity = 0 m/s | — | 47.9 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 1 m/s | — | 41.8 | — | °C/W |
| | | 4-Layer PCB, Air velocity = 2 m/s | — | 39.6 | — | °C/W |

### 4.1.6 Backup Supply Domain

**Table 4.6. Backup Supply Domain**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Backup supply voltage range | $V_{BU\_VIN}$ | | 1.8 | — | 3.8 | V |
| PWRRES resistor | $R_{PWRRES}$ | EMU_BUCTRL_PWRRES = RES0 | 3400 | 3900 | 4400 | Ω |
| | | EMU_BUCTRL_PWRRES = RES1 | 1450 | 1800 | 2150 | Ω |
| | | EMU_BUCTRL_PWRRES = RES2 | 1000 | 1350 | 1700 | Ω |
| | | EMU_BUCTRL_PWRRES = RES3 | 525 | 815 | 1100 | Ω |
| Output impedance between BU_VIN and BU_VOUT [2] | $R_{BU\_VOUT}$ | EMU_BUCTRL_VOUTRES = STRONG | 35 | 110 | 185 | Ω |
| | | EMU_BUCTRL_VOUTRES = MED | 475 | 775 | 1075 | Ω |
| | | EMU_BUCTRL_VOUTRES = WEAK | 5600 | 6500 | 7400 | Ω |
| Supply current | $I_{BU\_VIN}$ | BU_VIN not powering backup domain | — | 11 | TBD | nA |
| | | BU_VIN powering backup domain[1] | — | 550 | TBD | nA |

**Note:**

1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.
2. BU_VOUT and BU_STAT signals are not available in all package configurations. Check the device pinout for availability.

### 4.1.19 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAINOUTEN = 1, $C_{LOAD}$ = 75 pF with OUTSCALE = 0, or $C_{LOAD}$ = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes[8] [1].

**Table 4.27. Operational Amplifier (OPAMP)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (from AVDD) | $V_{OPA}$ | HCMDIS = 0, Rail-to-rail input range | 2 | — | 3.8 | V |
| | | HCMDIS = 1 | 1.62 | — | 3.8 | V |
| Input voltage | $V_{IN}$ | HCMDIS = 0, Rail-to-rail input range | $V_{VSS}$ | — | $V_{OPA}$ | V |
| | | HCMDIS = 1 | $V_{VSS}$ | — | $V_{OPA}$-1.2 | V |
| Input impedance | $R_{IN}$ | | 100 | — | — | MΩ |
| Output voltage | $V_{OUT}$ | | $V_{VSS}$ | — | $V_{OPA}$ | V |
| Load capacitance[2] | $C_{LOAD}$ | OUTSCALE = 0 | — | — | 75 | pF |
| | | OUTSCALE = 1 | — | — | 37.5 | pF |
| Output impedance | $R_{OUT}$ | DRIVESTRENGTH = 2 or 3, 0.4 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.4 V, -8 mA < $I_{OUT}$ < 8 mA, Buffer connection, Full supply range | — | 0.25 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.4 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.4 V, -400 µA < $I_{OUT}$ < 400 µA, Buffer connection, Full supply range | — | 0.6 | — | Ω |
| | | DRIVESTRENGTH = 2 or 3, 0.1 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.1 V, -2 mA < $I_{OUT}$ < 2 mA, Buffer connection, Full supply range | — | 0.4 | — | Ω |
| | | DRIVESTRENGTH = 0 or 1, 0.1 V ≤ $V_{OUT}$ ≤ $V_{OPA}$ - 0.1 V, -100 µA < $I_{OUT}$ < 100 µA, Buffer connection, Full supply range | — | 1 | — | Ω |
| Internal closed-loop gain | $G_{CL}$ | Buffer connection | TBD | 1 | TBD | - |
| | | 3x Gain connection | TBD | 2.99 | TBD | - |
| | | 16x Gain connection | TBD | 15.7 | TBD | - |
| Active current[4] | $I_{OPA}$ | DRIVESTRENGTH = 3, OUTSCALE = 0 | — | 580 | — | µA |
| | | DRIVESTRENGTH = 2, OUTSCALE = 0 | — | 176 | — | µA |
| | | DRIVESTRENGTH = 1, OUTSCALE = 0 | — | 13 | — | µA |
| | | DRIVESTRENGTH = 0, OUTSCALE = 0 | — | 4.7 | — | µA |

### 4.1.23 I2C

#### 4.1.23.1 I2C Standard-mode (Sm)[1]

**Table 4.31. I2C Standard-mode (Sm)[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[2] | $f_{SCL}$ | | 0 | — | 100 | kHz |
| SCL clock low time | $t_{LOW}$ | | 4.7 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 4 | — | — | µs |
| SDA set-up time | $t_{SU\_DAT}$ | | 250 | — | — | ns |
| SDA hold time[3] | $t_{HD\_DAT}$ | | 100 | — | 3450 | ns |
| Repeated START condition set-up time | $t_{SU\_STA}$ | | 4.7 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD\_STA}$ | | 4 | — | — | µs |
| STOP condition set-up time | $t_{SU\_STO}$ | | 4 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 4.7 | — | — | µs |

**Note:**
1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD\_DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).

#### 4.1.23.2 I2C Fast-mode (Fm)[1]

**Table 4.32. I2C Fast-mode (Fm)[1]**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SCL clock frequency[2] | $f_{SCL}$ | | 0 | — | 400 | kHz |
| SCL clock low time | $t_{LOW}$ | | 1.3 | — | — | µs |
| SCL clock high time | $t_{HIGH}$ | | 0.6 | — | — | µs |
| SDA set-up time | $t_{SU\_DAT}$ | | 100 | — | — | ns |
| SDA hold time[3] | $t_{HD\_DAT}$ | | 100 | — | 900 | ns |
| Repeated START condition set-up time | $t_{SU\_STA}$ | | 0.6 | — | — | µs |
| (Repeated) START condition hold time | $t_{HD\_STA}$ | | 0.6 | — | — | µs |
| STOP condition set-up time | $t_{SU\_STO}$ | | 0.6 | — | — | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | | 1.3 | — | — | µs |

**Note:**

1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).

### EBI Read Enable Timing Requirements

Timing applies to both EBI_REn and EBI_NANDREn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.40. EBI Read Enable Timing Requirements**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Setup time, from EBI_AD valid to trailing EBI_REn edge | $t_{SU\_REn}$ | IOVDD ≥ 1.62 V | 55 | — | — | ns |
| | | IOVDD ≥ 3.0 V | 36 | — | — | ns |
| Hold time, from trailing EBI_REn edge to EBI_AD invalid | $t_{H\_REn}$ | IOVDD ≥ 1.62 V | -9 | — | — | ns |

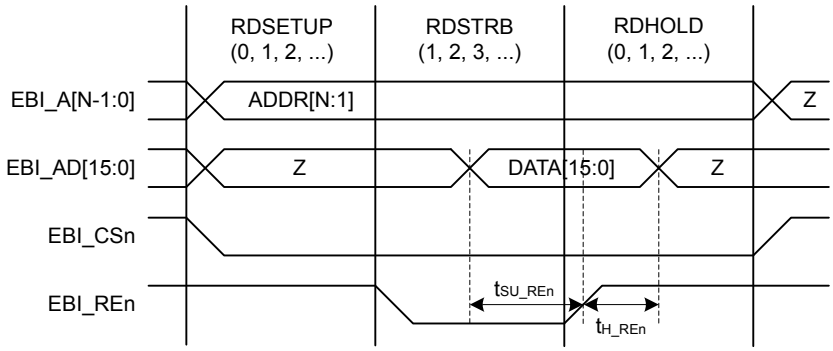


**Figure 4.7. EBI Read Enable Timing Requirements**

### EBI Ready/Wait Timing Requirements

Timing applies to both EBI_REn and EBI_WEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

**Table 4.41. EBI Ready/Wait Timing Requirements**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge | $t_{SU\_ARDY}$ | IOVDD ≥ 1.62 V | 55 + (3 * $t_{HFCOR-ECLK}$) | — | — | ns |
| | | IOVDD ≥ 3.0 V | 36 + (3 * $t_{HFCOR-ECLK}$) | — | — | ns |
| Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid | $t_{H\_ARDY}$ | IOVDD ≥ 1.62 V | -9 | — | — | ns |

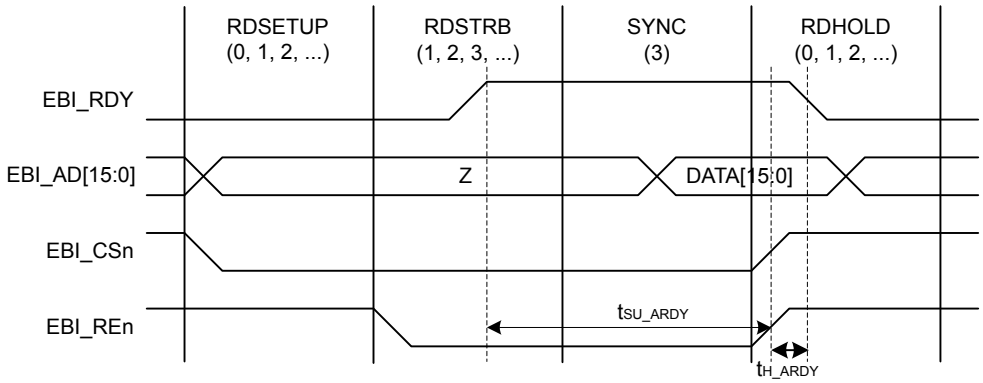


**Figure 4.8. EBI Ready/Wait Timing Requirements**

### SDIO HS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 0. Loading between 5 and 10 pF on all pins or between 10 and 20 pF on all pins.

**Table 4.47. SDIO HS Mode Timing (Location 0)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Clock frequency during data transfer | $F_{SD\_CLK}$ | Using HFRCO, AUXHFRCO, or USHFRCO | — | — | 45 | MHz |
| | | Using HFXO | — | — | TBD | MHz |
| Clock low time | $t_{WL}$ | Using HFRCO, AUXHFRCO, or USHFRCO | 10.0 | — | — | ns |
| | | Using HFXO | TBD | — | — | ns |
| Clock high time | $t_{WH}$ | Using HFRCO, AUXHFRCO, or USHFRCO | 10.0 | — | — | ns |
| | | Using HFXO | TBD | — | — | ns |
| Clock rise time | $t_R$ | | 1.69 | 3.23 | — | ns |
| Clock fall time | $t_F$ | | 1.42 | 2.79 | — | ns |
| Input setup time, CMD, DAT[0:3] valid to SD_CLK | $t_{ISU}$ | | 6 | — | — | ns |
| Input hold time, SD_CLK to CMD, DAT[0:3] change | $t_{IH}$ | | 2.5 | — | — | ns |
| Output delay time, SD_CLK to CMD, DAT[0:3] valid | $t_{ODLY}$ | | 0 | — | 13 | ns |
| Output hold time, SD_CLK to CMD, DAT[0:3] change | $t_{OH}$ | | 2 | — | — | ns |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PB2 | 11 | GPIO | PB3 | 12 | GPIO |
| PB4 | 13 | GPIO | PB5 | 14 | GPIO |
| PB6 | 15 | GPIO | VSS | 16<br>32<br>59<br>83 | Ground |
| PC0 | 18 | GPIO (5V) | PC1 | 19 | GPIO (5V) |
| PC2 | 20 | GPIO (5V) | PC3 | 21 | GPIO (5V) |
| PC4 | 22 | GPIO | PC5 | 23 | GPIO |
| PB7 | 24 | GPIO | PB8 | 25 | GPIO |
| PA7 | 26 | GPIO | PA8 | 27 | GPIO |
| PA9 | 28 | GPIO | PA10 | 29 | GPIO |
| PA11 | 30 | GPIO | PA12 | 33 | GPIO (5V) |
| PA13 | 34 | GPIO (5V) | PA14 | 35 | GPIO |
| RESETn | 36 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | PB9 | 37 | GPIO (5V) |
| PB10 | 38 | GPIO (5V) | PB11 | 39 | GPIO |
| PB12 | 40 | GPIO | AVDD | 41 | Analog power supply. |
| PB13 | 42 | GPIO | PB14 | 43 | GPIO |
| PD0 | 45 | GPIO (5V) | PD1 | 46 | GPIO |
| PD2 | 47 | GPIO (5V) | PD3 | 48 | GPIO |
| PD4 | 49 | GPIO | PD5 | 50 | GPIO |
| PD6 | 51 | GPIO | PD7 | 52 | GPIO |
| PD8 | 53 | GPIO | PC7 | 54 | GPIO |
| VREGVSS | 55 | Voltage regulator VSS | VREGSW | 56 | DCDC regulator switching node |
| VREGVDD | 57 | Voltage regulator VDD input | DVDD | 58 | Digital power supply. |
| DECOUPLE | 60 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. | PE1 | 61 | GPIO (5V) |
| PE2 | 62 | GPIO | PE3 | 63 | GPIO |
| PE4 | 64 | GPIO | PE5 | 65 | GPIO |
| PE6 | 66 | GPIO | PE7 | 67 | GPIO |
| PC8 | 68 | GPIO (5V) | PC9 | 69 | GPIO (5V) |
| PC10 | 70 | GPIO (5V) | PC11 | 71 | GPIO (5V) |
| VREGI | 72 | Input to 5 V regulator. | VREGO | 73 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |
| PF10 | 74 | GPIO (5V) | PF11 | 75 | GPIO (5V) |
| PF0 | 76 | GPIO (5V) | PF1 | 77 | GPIO (5V) |

### 5.12 EFM32GG11B8xx in QFP64 Device Pinout

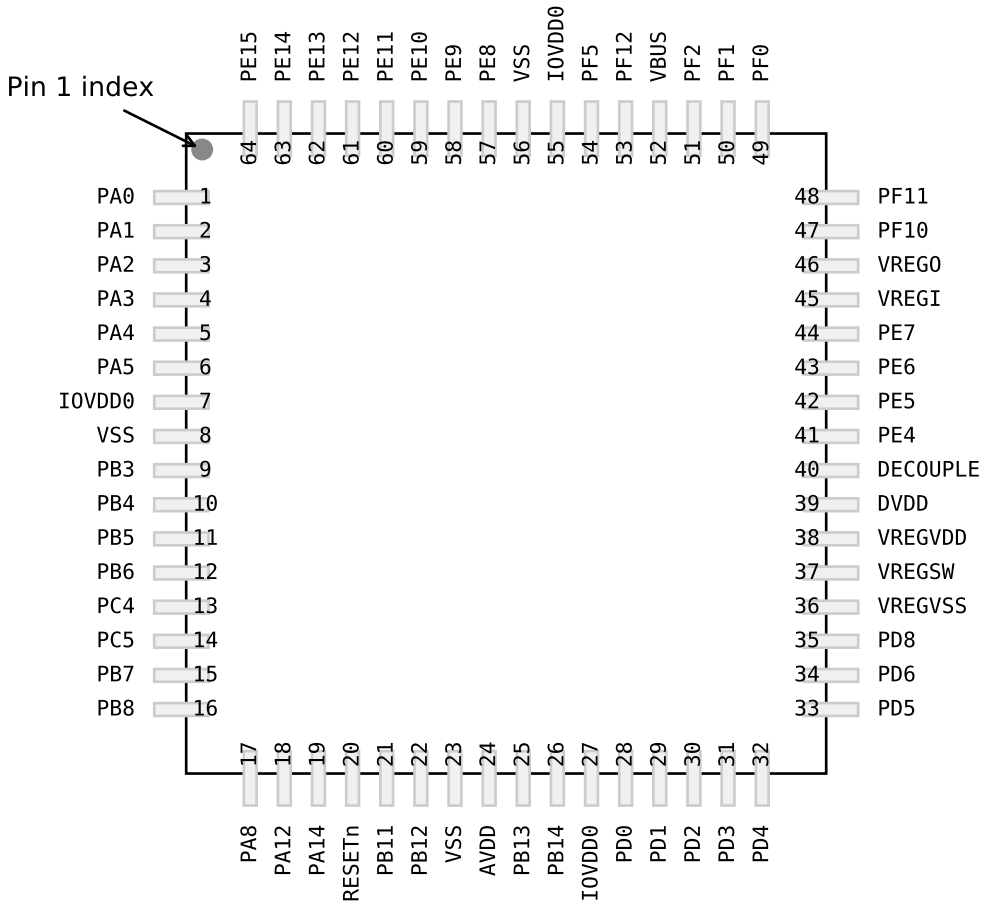


**Figure 5.12. EFM32GG11B8xx in QFP64 Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

**Table 5.12. EFM32GG11B8xx in QFP64 Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PA0 | 1 | GPIO | PA1 | 2 | GPIO |
| PA2 | 3 | GPIO | PA3 | 4 | GPIO |
| PA4 | 5 | GPIO | PA5 | 6 | GPIO |
| IOVDD0 | 7<br>27<br>55 | Digital IO power supply 0. | VSS | 8<br>23<br>56 | Ground |
| PB3 | 9 | GPIO | PB4 | 10 | GPIO |
| PB5 | 11 | GPIO | PB6 | 12 | GPIO |

### 5.17 EFM32GG11B5xx in QFN64 Device Pinout

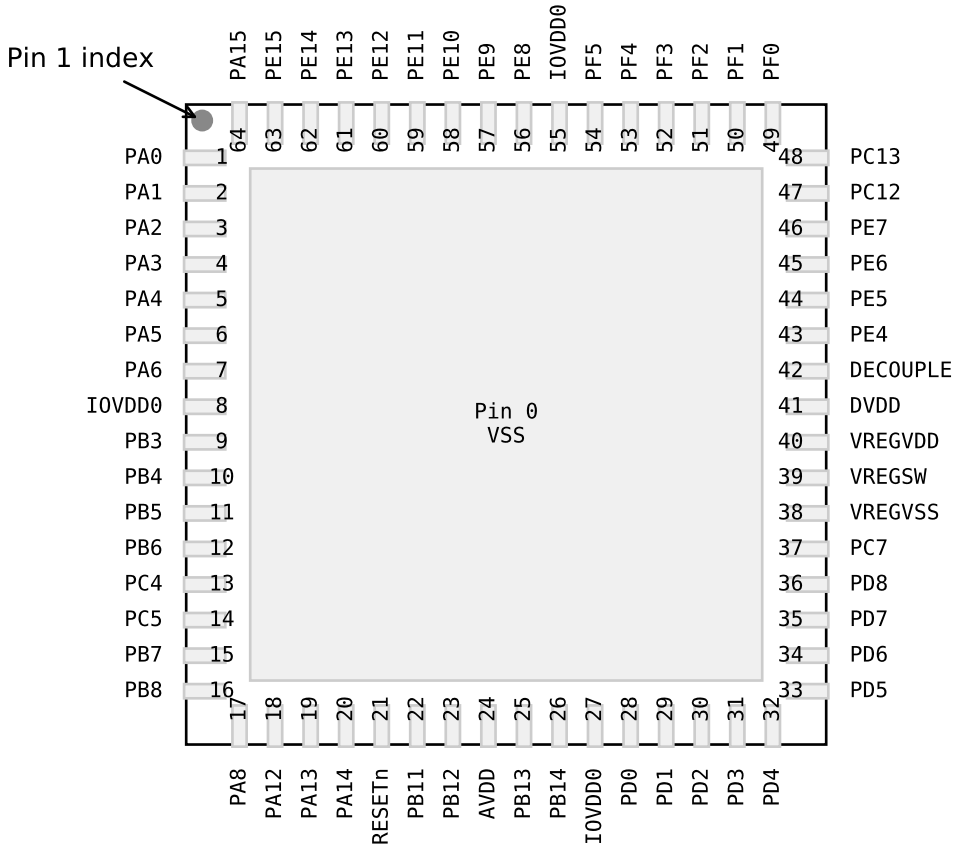


**Figure 5.17. EFM32GG11B5xx in QFN64 Device Pinout**

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

**Table 5.17. EFM32GG11B5xx in QFN64 Device Pinout**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| VSS | 0 | Ground | PA0 | 1 | GPIO |
| PA1 | 2 | GPIO | PA2 | 3 | GPIO |
| PA3 | 4 | GPIO | PA4 | 5 | GPIO |
| PA5 | 6 | GPIO | PA6 | 7 | GPIO |
| IOVDD0 | 8<br>27<br>55 | Digital IO power supply 0. | PB3 | 9 | GPIO |
| PB4 | 10 | GPIO | PB5 | 11 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PB6 | 12 | GPIO | PC4 | 13 | GPIO |
| PC5 | 14 | GPIO | PB7 | 15 | GPIO |
| PB8 | 16 | GPIO | PA8 | 17 | GPIO |
| PA12 | 18 | GPIO (5V) | PA13 | 19 | GPIO (5V) |
| PA14 | 20 | GPIO | RESETn | 21 | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. |
| PB11 | 22 | GPIO | PB12 | 23 | GPIO |
| AVDD | 24 | Analog power supply. | PB13 | 25 | GPIO |
| PB14 | 26 | GPIO | PD0 | 28 | GPIO (5V) |
| PD1 | 29 | GPIO | PD2 | 30 | GPIO (5V) |
| PD3 | 31 | GPIO | PD4 | 32 | GPIO |
| PD5 | 33 | GPIO | PD6 | 34 | GPIO |
| PD7 | 35 | GPIO | PD8 | 36 | GPIO |
| PC7 | 37 | GPIO | VREGVSS | 38 | Voltage regulator VSS |
| VREGSW | 39 | DCDC regulator switching node | VREGVDD | 40 | Voltage regulator VDD input |
| DVDD | 41 | Digital power supply. | DECOUPLE | 42 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. |
| PE4 | 43 | GPIO | PE5 | 44 | GPIO |
| PE6 | 45 | GPIO | PE7 | 46 | GPIO |
| PC12 | 47 | GPIO (5V) | PC13 | 48 | GPIO (5V) |
| PF0 | 49 | GPIO (5V) | PF1 | 50 | GPIO (5V) |
| PF2 | 51 | GPIO | PF3 | 52 | GPIO |
| PF4 | 53 | GPIO | PF5 | 54 | GPIO |
| PE8 | 56 | GPIO | PE9 | 57 | GPIO |
| PE10 | 58 | GPIO | PE11 | 59 | GPIO |
| PE12 | 60 | GPIO | PE13 | 61 | GPIO |
| PE14 | 62 | GPIO | PE15 | 63 | GPIO |
| PA15 | 64 | GPIO | | | |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).

| Alternate | LOCATION | | |
|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| ETH_TSUTMR-TOG | 0: PB6<br>1: PB15<br>2: PC3<br>3: PF9 | | Ethernet IEEE1588 Timer Toggle. |
| ETM_TCLK | 0: PD7<br>1: PF8<br>2: PC6<br>3: PA6 | 4: PE11<br>5: PG15 | Embedded Trace Module ETM clock . |
| ETM_TD0 | 0: PD6<br>1: PF9<br>2: PC7<br>3: PA2 | 4: PE12<br>5: PG14 | Embedded Trace Module ETM data 0. |
| ETM_TD1 | 0: PD3<br>1: PD13<br>2: PD3<br>3: PA3 | 4: PE13<br>5: PG13 | Embedded Trace Module ETM data 1. |
| ETM_TD2 | 0: PD4<br>1: PB15<br>2: PD4<br>3: PA4 | 4: PE14<br>5: PG12 | Embedded Trace Module ETM data 2. |
| ETM_TD3 | 0: PD5<br>1: PF3<br>2: PD5<br>3: PA5 | 4: PE15<br>5: PG11 | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | 0: PA0 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | 0: PA6 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU2 | 0: PC9 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | 0: PF1 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | 0: PF2 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | 0: PE13 | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU6 | 0: PC4 | | Pin can be used to wake the system up from EM4 |

**Table 5.24. ACMP1 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT0X | BUSACMP1X | | | | | | | | | | | | | | | | | | | | | | | | | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 |
| APORT0Y | BUSACMP1Y | | | | | | | | | | | | | | | | | | | | | | | | | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 |
| APORT1X | BUSAX | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT1Y | BUSAY | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | |
| APORT2X | BUSBX | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | |
| APORT2Y | BUSBY | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT3X | BUSCX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | | | PE0 |
| APORT3Y | BUSCY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | | | PE1 | |
| APORT4X | BUSDX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | | | PE1 | |
| APORT4Y | BUSDY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | | | PE0 |

**Table 5.25. ACMP2 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT0X | BUSACMP2X | | | | | | | | | | | | | | | | | | | | | | | | | PG7 | PG6 | PG5 | PG4 | PG3 | PG2 | PG1 | PG0 |
| APORT0Y | BUSACMP2Y | | | | | | | | | | | | | | | | | | | | | | | | | PG7 | PG6 | PG5 | PG4 | PG3 | PG2 | PG1 | PG0 |
| APORT1X | BUSAX | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT1Y | BUSAY | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | |
| APORT2X | BUSBX | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | |
| APORT2Y | BUSBY | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT3X | BUSCX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | | | PE0 |
| APORT3Y | BUSCY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | | | PE1 | |
| APORT4X | BUSDX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | | | PE1 | |
| APORT4Y | BUSDY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | | | PE0 |

# 12. QFN64 Package Specifications

## 12.1 QFN64 Package Dimensions

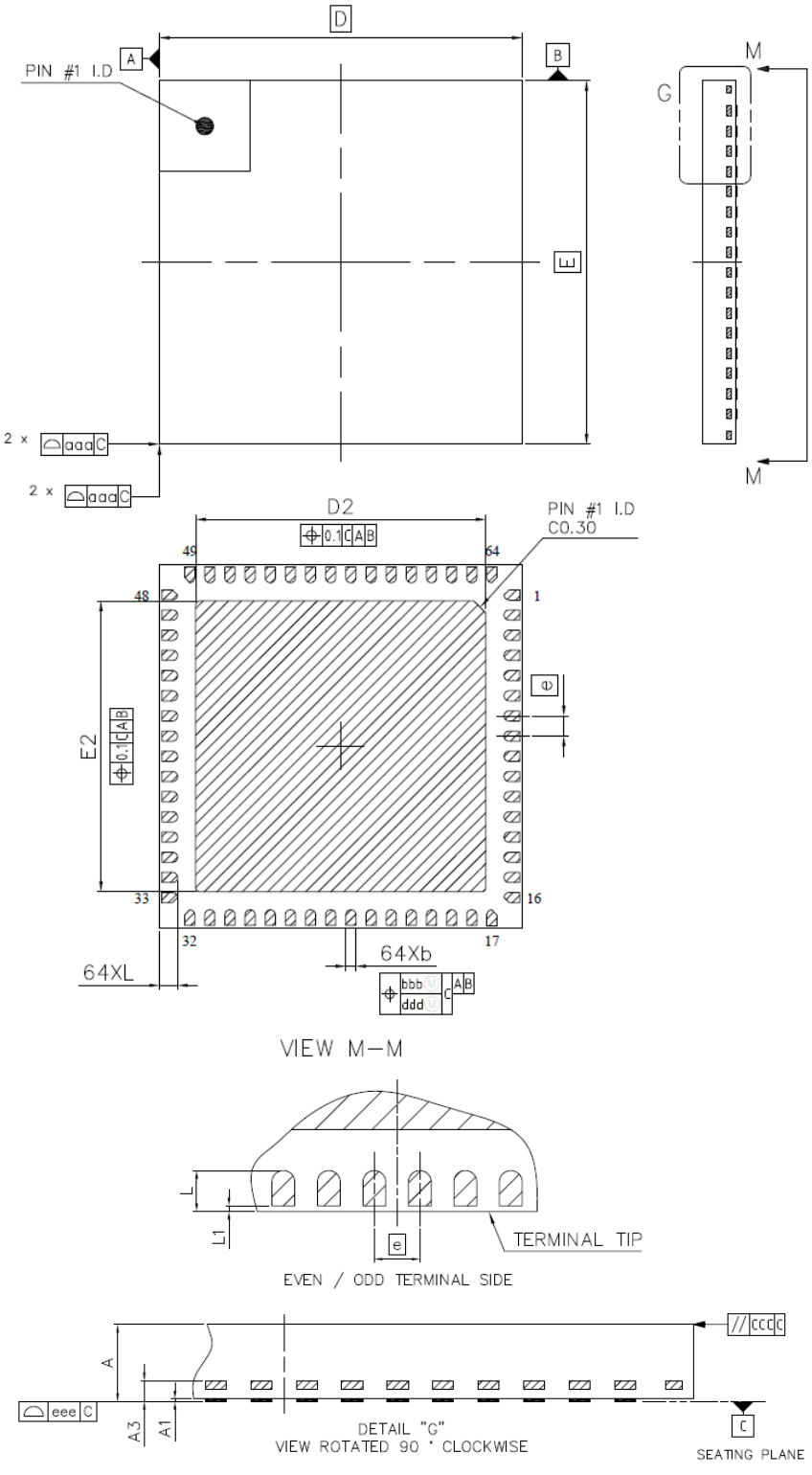


**Figure 12.1. QFN64 Package Drawing**