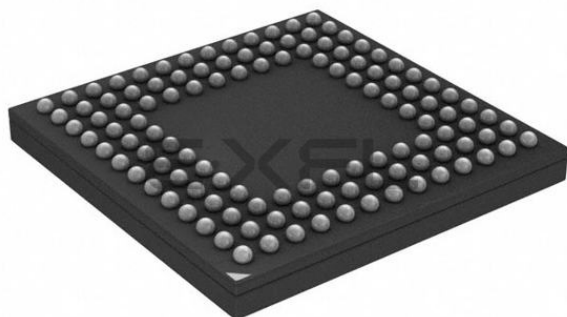




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	95
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024il120-ar

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 μ H (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 μ F (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V _{DCDC_I}	Bypass mode, I _{DCDC_LOAD} = 50 mA	1.8	—	V _{VREGVDD_MAX}	V
		Low noise (LN) mode, 1.8 V output, I _{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I _{DCDC_LOAD} = 10 mA	2.4	—	V _{VREGVDD_MAX}	V
		Low noise (LN) mode, 1.8 V output, I _{DCDC_LOAD} = 200 mA	2.6	—	V _{VREGVDD_MAX}	V
Output voltage programmable range ¹	V _{DCDC_O}		1.8	—	V _{VREGVDD}	V
Regulation DC accuracy	ACC _{DC}	Low Noise (LN) mode, 1.8 V target output	TBD	—	TBD	V
Regulation window ⁴	WIN _{REG}	Low Power (LP) mode, LPCMPBIASEMxx ³ = 0, 1.8 V target output, I _{DCDC_LOAD} ≤ 75 μ A	TBD	—	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx ³ = 3, 1.8 V target output, I _{DCDC_LOAD} ≤ 10 mA	TBD	—	TBD	V
Steady-state output ripple	V _R		—	3	—	mVpp
Output voltage under/overshoot	V _{OV}	CCM Mode (LNFORCECCM ³ = 1), Load changes between 0 mA and 100 mA	—	25	TBD	mV
		DCM Mode (LNFORCECCM ³ = 0), Load changes between 0 mA and 10 mA	—	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM ³ = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM ³ = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V _{REG}	Input changes between V _{VREGVDD_MAX} and 2.4 V	—	0.1	—	%
DC load regulation	I _{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

4.1.8 Wake Up Times

Table 4.10. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake up time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	11.8	—	μs
		Code execution from RAM	—	4.1	—	μs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	11.8	—	μs
		Code execution from RAM	—	4.1	—	μs
Wake up from EM4H ¹	t_{EM4H_WU}	Executing from flash	—	94	—	μs
Wake up from EM4S ¹	t_{EM4S_WU}	Executing from flash	—	294	—	μs
Time from release of reset source to first instruction execution	t_{RESET}	Soft Pin Reset released	—	55	—	μs
		Any other reset released	—	359	—	μs
Power mode scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz ^{4 2}	—	31.8	—	μs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz ³	—	4.3	—	μs

Note:

1. Time from wake up request until first instruction is executed. Wakeup results in device reset.
2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/ μs for approximately 20 μs . During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 μF capacitor) to 70 mA (with a 2.7 μF capacitor).
3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 μs + 29 HFCLKs.
4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 μs + 28 HFCLKs.

4.1.10.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.14. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f _{LFRCO}	ENVREF ² = 1	TBD	32.768	TBD	kHz
		ENVREF ² = 1, T > 85 °C	TBD	32.768	TBD	kHz
		ENVREF ² = 0	TBD	32.768	TBD	kHz
Startup time	t _{LFRCO}		—	500	—	μs
Current consumption ¹	I _{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	370	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	520	—	nA

Note:
1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. In CMU_LFRCOCTRL register.

4.1.15 Analog Comparator (ACMP)

Table 4.23. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL ¹	—	—	$V_{ACMPVDD}$	V
Supply voltage	$V_{ACMPVDD}$	BIASPROG ⁴ ≤ 0x10 or FULL- BIAS ⁴ = 0	1.8	—	$V_{VREGVDD_MAX}$	V
		0x10 < BIASPROG ⁴ ≤ 0x20 and FULLBIAS ⁴ = 1	2.1	—	$V_{VREGVDD_MAX}$	V
Active current not including voltage reference ²	I_{ACMP}	BIASPROG ⁴ = 1, FULLBIAS ⁴ = 0	—	50	—	nA
		BIASPROG ⁴ = 0x10, FULLBIAS ⁴ = 0	—	306	—	nA
		BIASPROG ⁴ = 0x02, FULLBIAS ⁴ = 1	—	6.5	—	μA
		BIASPROG ⁴ = 0x20, FULLBIAS ⁴ = 1	—	74	TBD	μA
Current consumption of inter- nal voltage reference ²	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	μA
		VADIV selected as input using VDD/1	—	2.4	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis ($V_{CM} = 1.25\text{ V}$, $BIASPROG^4 = 0x10$, $FULLBIAS^4 = 1$)	$V_{ACMPHYST}$	$HYSTSEL^5 = HYST0$	TBD	0	TBD	mV
		$HYSTSEL^5 = HYST1$	TBD	18	TBD	mV
		$HYSTSEL^5 = HYST2$	TBD	33	TBD	mV
		$HYSTSEL^5 = HYST3$	TBD	46	TBD	mV
		$HYSTSEL^5 = HYST4$	TBD	57	TBD	mV
		$HYSTSEL^5 = HYST5$	TBD	68	TBD	mV
		$HYSTSEL^5 = HYST6$	TBD	79	TBD	mV
		$HYSTSEL^5 = HYST7$	TBD	90	TBD	mV
		$HYSTSEL^5 = HYST8$	TBD	0	TBD	mV
		$HYSTSEL^5 = HYST9$	TBD	-18	TBD	mV
		$HYSTSEL^5 = HYST10$	TBD	-33	TBD	mV
		$HYSTSEL^5 = HYST11$	TBD	-45	TBD	mV
		$HYSTSEL^5 = HYST12$	TBD	-57	TBD	mV
		$HYSTSEL^5 = HYST13$	TBD	-67	TBD	mV
		$HYSTSEL^5 = HYST14$	TBD	-78	TBD	mV
		$HYSTSEL^5 = HYST15$	TBD	-88	TBD	mV
Comparator delay ³	$t_{ACMPDELAY}$	$BIASPROG^4 = 1$, $FULLBIAS^4 = 0$	—	30	—	μs
		$BIASPROG^4 = 0x10$, $FULLBIAS^4 = 0$	—	3.7	—	μs
		$BIASPROG^4 = 0x02$, $FULLBIAS^4 = 1$	—	360	—	ns
		$BIASPROG^4 = 0x20$, $FULLBIAS^4 = 1$	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	$BIASPROG^4 = 0x10$, $FULLBIAS^4 = 1$	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	$CSRESSEL^6 = 0$	—	infinite	—	k Ω
		$CSRESSEL^6 = 1$	—	15	—	k Ω
		$CSRESSEL^6 = 2$	—	27	—	k Ω
		$CSRESSEL^6 = 3$	—	39	—	k Ω
		$CSRESSEL^6 = 4$	—	51	—	k Ω
		$CSRESSEL^6 = 5$	—	100	—	k Ω
		$CSRESSEL^6 = 6$	—	162	—	k Ω
		$CSRESSEL^6 = 7$	—	235	—	k Ω

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load. 2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range. 3. Entire range is monotonic and has no missing codes. 4. Current from HUPERCLK is dependent on HUPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU. 5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain. 6. PSRR calculated as $20 * \log_{10}(\Delta V_{DD} / \Delta V_{OUT})$, VDAC output at 90% of full scale						

EBI Read Enable Timing Requirements

Timing applies to both EBI_REn and EBI_NANDREn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.40. EBI Read Enable Timing Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Setup time, from EBI_AD valid to trailing EBI_REn edge	t_{SU_REn}	IOVDD $\geq$ 1.62 V	55	—	—	ns
		IOVDD $\geq$ 3.0 V	36	—	—	ns
Hold time, from trailing EBI_REn edge to EBI_AD invalid	t_{H_REn}	IOVDD $\geq$ 1.62 V	-9	—	—	ns

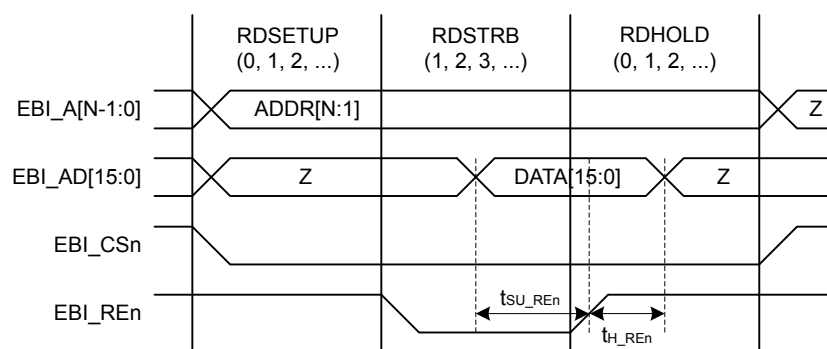


Figure 4.7. EBI Read Enable Timing Requirements

4.1.27 Serial Data I/O Host Controller (SDIO)

SDIO DS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.46. SDIO DS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F _{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	23	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t _{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t _{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t _R		1.69	3.23	—	ns
Clock fall time	t _F		1.42	2.79	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t _{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t _{IH}		0	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t _{ODLY}		0	—	14	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t _{OH}		5	—	—	ns

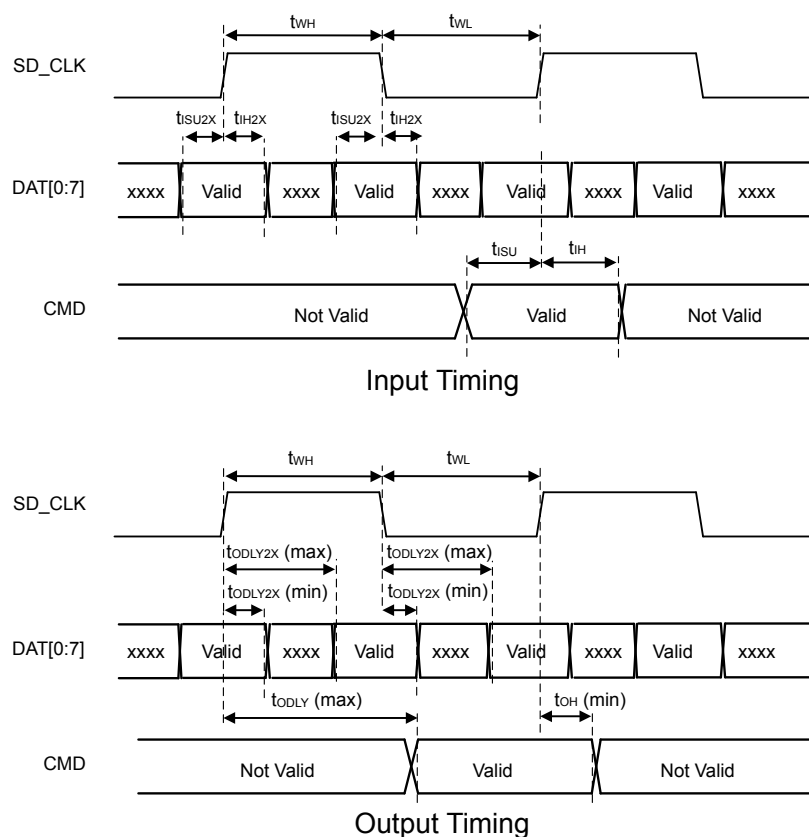


Figure 4.20. SDIO MMC DDR Mode Timing

4.1.28 Quad SPI (QSPI)

4.1.28.1 QSPI SDR Mode

QSPI SDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 23, RX DLL = 48, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.54. QSPI SDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Full SCLK period	T		$(1/F_{SCLK}) * 0.95$	—	—	ns
Output valid	t_{OV}		—	—	$T/2 - 2.4$	ns
Output hold	t_{OH}		$T/2 - 32.9$	—	—	ns
Input setup	t_{SU}		$36.2 - T/2$	—	—	ns
Input hold	t_{H}		$T/2 - 3.3$	—	—	ns

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF11	A13	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO
PE8	B4	GPIO	PD12	B5	GPIO
PD10	B6	GPIO	PF8	B7	GPIO
PF6	B8	GPIO	PF13	B9	GPIO (5V)
PF4	B10	GPIO	PF3	B11	GPIO
VBUS	B12	USB VBUS signal and auxiliary input to 5 V regulator.	PF10	B13	GPIO (5V)
PA1	C1	GPIO	PA0	C2	GPIO
PE10	C3	GPIO	PD13	C4	GPIO (5V)
VSS	C5 C8 H3 J3 K11 L12 L15	Ground	IOVDD1	C6	Digital IO power supply 1.
PF9	C7	GPIO	IOVDD0	C9 J11 K3 L11 L16	Digital IO power supply 0.
PF2	C10	GPIO	PF1	C11	GPIO (5V)
PC14	C12	GPIO (5V)	PC15	C13	GPIO (5V)
PA3	D1	GPIO	PA2	D2	GPIO
PB15	D3	GPIO (5V)	PF0	D11	GPIO (5V)
PC12	D12	GPIO (5V)	PC13	D13	GPIO (5V)
PA6	E1	GPIO	PA5	E2	GPIO
PA4	E3	GPIO	PC9	E11	GPIO (5V)
PC10	E12	GPIO (5V)	PC11	E13	GPIO (5V)
PB0	F1	GPIO	PB1	F2	GPIO
PB2	F3	GPIO	PE6	F11	GPIO
PE7	F12	GPIO	PC8	F13	GPIO (5V)
PB3	G1	GPIO	PB4	G2	GPIO
IOVDD2	G3	Digital IO power supply 2.	PE3	G11	GPIO
PE4	G12	GPIO	PE5	G13	GPIO
PB5	H1	GPIO	PB6	H2	GPIO
DVDD	H11	Digital power supply.	PE2	H12	GPIO
DECOUPLE	H13	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PD14	J1	GPIO (5V)
PD15	J2	GPIO (5V)	PE1	J12	GPIO (5V)

5.6 EFM32GG11B4xx in BGA112 Device Pinout

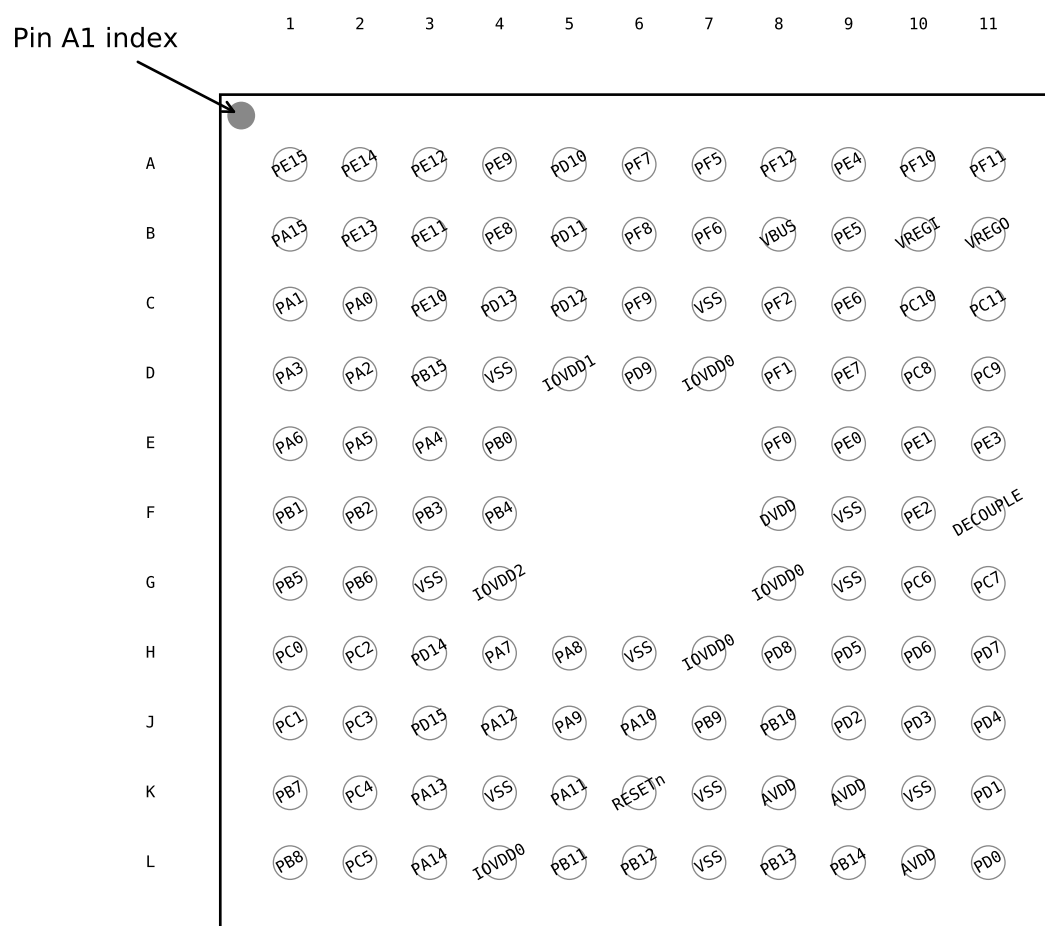


Figure 5.6. EFM32GG11B4xx in BGA112 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.6. EFM32GG11B4xx in BGA112 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD10	A5	GPIO	PF7	A6	GPIO
PF5	A7	GPIO	PF12	A8	GPIO
PE4	A9	GPIO	PF10	A10	GPIO (5V)
PF11	A11	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	B3	GPIO

5.12 EFM32GG11B8xx in QFP64 Device Pinout

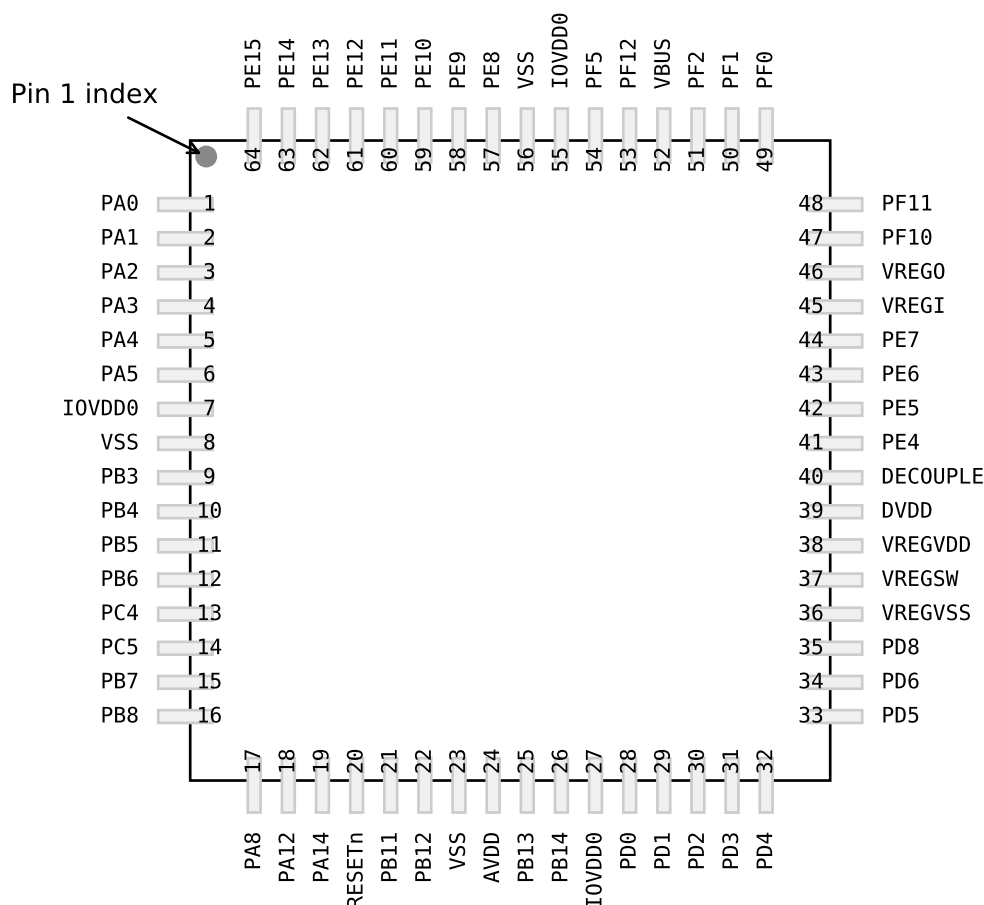


Figure 5.12. EFM32GG11B8xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see [5.20 GPIO Functionality Table](#) or [5.21 Alternate Functionality Overview](#).

Table 5.12. EFM32GG11B8xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 27 55	Digital IO power supply 0.	VSS	8 23 56	Ground
PB3	9	GPIO	PB4	10	GPIO
PB5	11	GPIO	PB6	12	GPIO

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF14	BUSDY BUSCX		TIM1_CC1 #6 TIM4_CC1 #1 TIM5_CC2 #7 WTIM3_CC1 #7	I2C2_SCL #4	
PF11	BUSCY BUSDX	EBI_NANDWE _n #5	TIM5_CC2 #6 WTIM3_CC2 #3 PCNT2_S1IN #3	US5_CTS #2 U1_RX #1 I2C2_SCL #2 USB_DP	
PF10	BUSDY BUSCX	EBI_ARDY #5	TIM5_CC1 #6 WTIM3_CC1 #3 PCNT2_S0IN #3	US5_RTS #2 U1_TX #1 I2C2_SDA #2 USB_DM	
PF0	BUSDY BUSCX	EBI_A24 #1	TIM0_CC0 #4 WTIM0_CC1 #4 LE- TIM0_OUT0 #2	US2_TX #5 CAN0_RX #1 US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	PRS_CH15 #2 ACMP3_O #0 DBG_SWCLKTCK BOOT_TX
PA0	BUSBY BUSAX LCD_SEG13	EBI_AD09 #0 EBI_CSTFT #3	TIM0_CC0 #0 TIM0_CC1 #7 TIM3_CC0 #4 PCNT0_S0IN #4	ETH_RMIITXEN #0 ETH_MII_TXCLK #0 SDIO_DAT0 #1 US1_RX #5 US3_TX #0 QSPI0_CS0 #1 LEU0_RX #4 I2C0_SDA #0	CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
PD11	LCD_SEG30	EBI_CS2 #0 EBI_HSNC #1	TIM4_CC0 #6 WTIM3_CC2 #0	ETH_RMIICRS _{SDV} #1 SDIO_DAT5 #0 QSPI0_DQ2 #0 ETH_MII_RXD3 #2 US4_CLK #1	
PD10	LCD_SEG29	EBI_CS1 #0 EBI_VSNC #1	TIM4_CC2 #5 WTIM3_CC1 #0	ETH_RMIIREFCLK #1 SDIO_DAT6 #0 QSPI0_DQ1 #0 ETH_MII_RXD2 #2 US4_RX #1	CMU_CLK2 #5 CMU_CLKI0 #5
PD9	LCD_SEG28	EBI_CS0 #0 EBI_DTEN #1	TIM4_CC1 #5 WTIM3_CC0 #0	ETH_RMIIRXD0 #1 SDIO_DAT7 #0 QSPI0_DQ0 #0 ETH_MII_RXD1 #2 US4_TX #1	
PF9	BUSCY BUSDX LCD_SEG27	EBI_RE _n #4 EBI_BL1 #1	TIM4_CC0 #5	ETH_RMIIRXD1 #1 US2_CS #4 QSPI0_DQS #0 ETH_MII_RXD0 #2 ETH_TSUTMRTOG #3 SDIO_WP #0 U0_RTS #0 U1_CTS #1	ETM_TD0 #1
PF8	BUSDY BUSCX LCD_SEG26	EBI_WE _n #4 EBI_BL0 #1	TIM0_CC2 #1 TIM4_CC2 #4	ETH_RMIITXEN #1 US2_CLK #4 QSPI0_CS1 #0 ETH_MII_RXDV #2 ETH_TSUEXTCLK #3 SDIO_CD #0 U0_CTS #0 U1_RTS #1	ETM_TCLK #1 GPIO_EM4WU8

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_TSUTMR-TOG	0: PB6 1: PB15 2: PC3 3: PF9		Ethernet IEEE1588 Timer Toggle.
ETM_TCLK	0: PD7 1: PF8 2: PC6 3: PA6	4: PE11 5: PG15	Embedded Trace Module ETM clock .
ETM_TD0	0: PD6 1: PF9 2: PC7 3: PA2	4: PE12 5: PG14	Embedded Trace Module ETM data 0.
ETM_TD1	0: PD3 1: PD13 2: PD3 3: PA3	4: PE13 5: PG13	Embedded Trace Module ETM data 1.
ETM_TD2	0: PD4 1: PB15 2: PD4 3: PA4	4: PE14 5: PG12	Embedded Trace Module ETM data 2.
ETM_TD3	0: PD5 1: PF3 2: PD5 3: PA5	4: PE15 5: PG11	Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US1_CTS	0: PB9 1: PD4 2: PF3 3: PC6	4: PC12 5: PB13 6: PH2	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PB10 1: PD5 2: PF4 3: PC7	4: PC13 5: PB14 6: PH3	USART1 Request To Send hardware flow control output.
US1_RX	0: PC1 1: PD1 2: PD6 3: PF7	4: PC2 5: PA0 6: PA2	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PC0 1: PD0 2: PD7 3: PF6	4: PC1 5: PF2 6: PA14	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	0: PC4 1: PB5 2: PA9 3: PA15	4: PF8 5: PF2	USART2 clock input / output.
US2_CS	0: PC5 1: PB6 2: PA10 3: PB11	4: PF9 5: PF5	USART2 chip select input / output.
US2_CTS	0: PC1 1: PB12 2: PA11 3: PB10	4: PC12 5: PD6	USART2 Clear To Send hardware flow control input.
US2_RTS	0: PC0 1: PB15 2: PA12 3: PC14	4: PC13 5: PD8	USART2 Request To Send hardware flow control output.
US2_RX	0: PC3 1: PB4 2: PA8 3: PA14	4: PF7 5: PF1	USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	0: PC2 1: PB3 2: PA7 3: PA13	4: PF6 5: PF0	USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
US3_CLK	0: PA2 1: PD7 2: PD4 3: PG8	4: PG2 5: PI14	USART3 clock input / output.
US3_CS	0: PA3 1: PE4 2: PC14 3: PC0	4: PG3 5: PI15	USART3 chip select input / output.
US3_CTS	0: PA4 1: PE5 2: PD6 3: PG10	4: PG4 5: PG9	USART3 Clear To Send hardware flow control input.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US3_RTS	0: PA5 1: PC1 2: PA14 3: PC15	4: PG5 5: PG11	USART3 Request To Send hardware flow control output.
US3_RX	0: PA1 1: PE7 2: PB7 3: PG7	4: PG1 5: PI13	USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PA0 1: PE6 2: PB3 3: PG6	4: PG0 5: PI12	USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI).
US4_CLK	0: PC4 1: PD11 2: PI2 3: PI8	4: PH6	USART4 clock input / output.
US4_CS	0: PC5 1: PD12 2: PI3 3: PI9	4: PH7	USART4 chip select input / output.
US4_CTS	0: PA7 1: PD13 2: PI4 3: PI10	4: PH8	USART4 Clear To Send hardware flow control input.
US4_RTS	0: PA8 1: PD14 2: PI5 3: PI11	4: PH9	USART4 Request To Send hardware flow control output.
US4_RX	0: PB8 1: PD10 2: PI1 3: PI7	4: PH5	USART4 Asynchronous Receive. USART4 Synchronous mode Master Input / Slave Output (MISO).
US4_TX	0: PB7 1: PD9 2: PI0 3: PI6	4: PH4	USART4 Asynchronous Transmit. Also used as receive input in half duplex communication. USART4 Synchronous mode Master Output / Slave Input (MOSI).
US5_CLK	0: PB11 1: PD13 2: PF13 3: PH12		USART5 clock input / output.
US5_CS	0: PB13 1: PD14 2: PF12 3: PH13		USART5 chip select input / output.
US5_CTS	0: PB14 1: PD15 2: PF11 3: PH14		USART5 Clear To Send hardware flow control input.
US5_RTS	0: PB12 1: PB15 2: PF10 3: PH15		USART5 Request To Send hardware flow control output.

[illegible]

9. BGA112 Package Specifications

9.1 BGA112 Package Dimensions

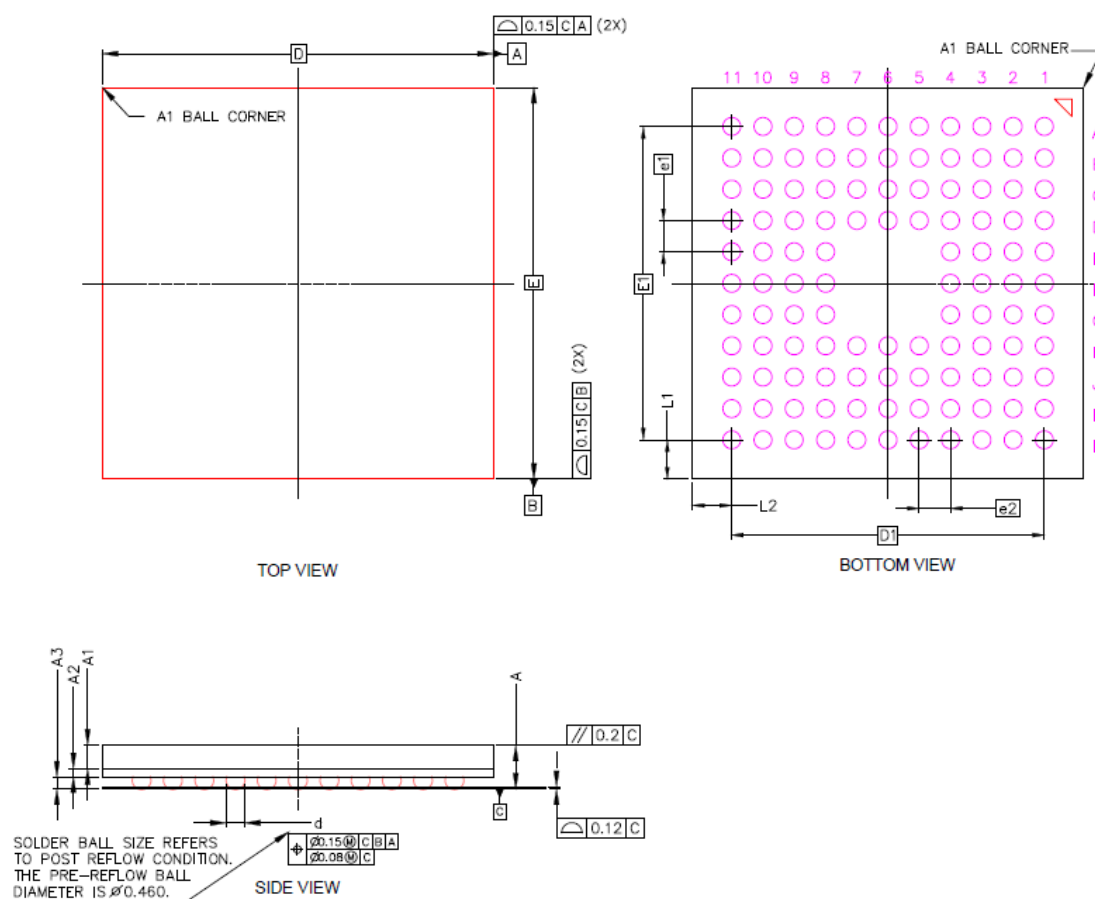


Figure 9.1. BGA112 Package Drawing

9.2 BGA112 PCB Land Pattern

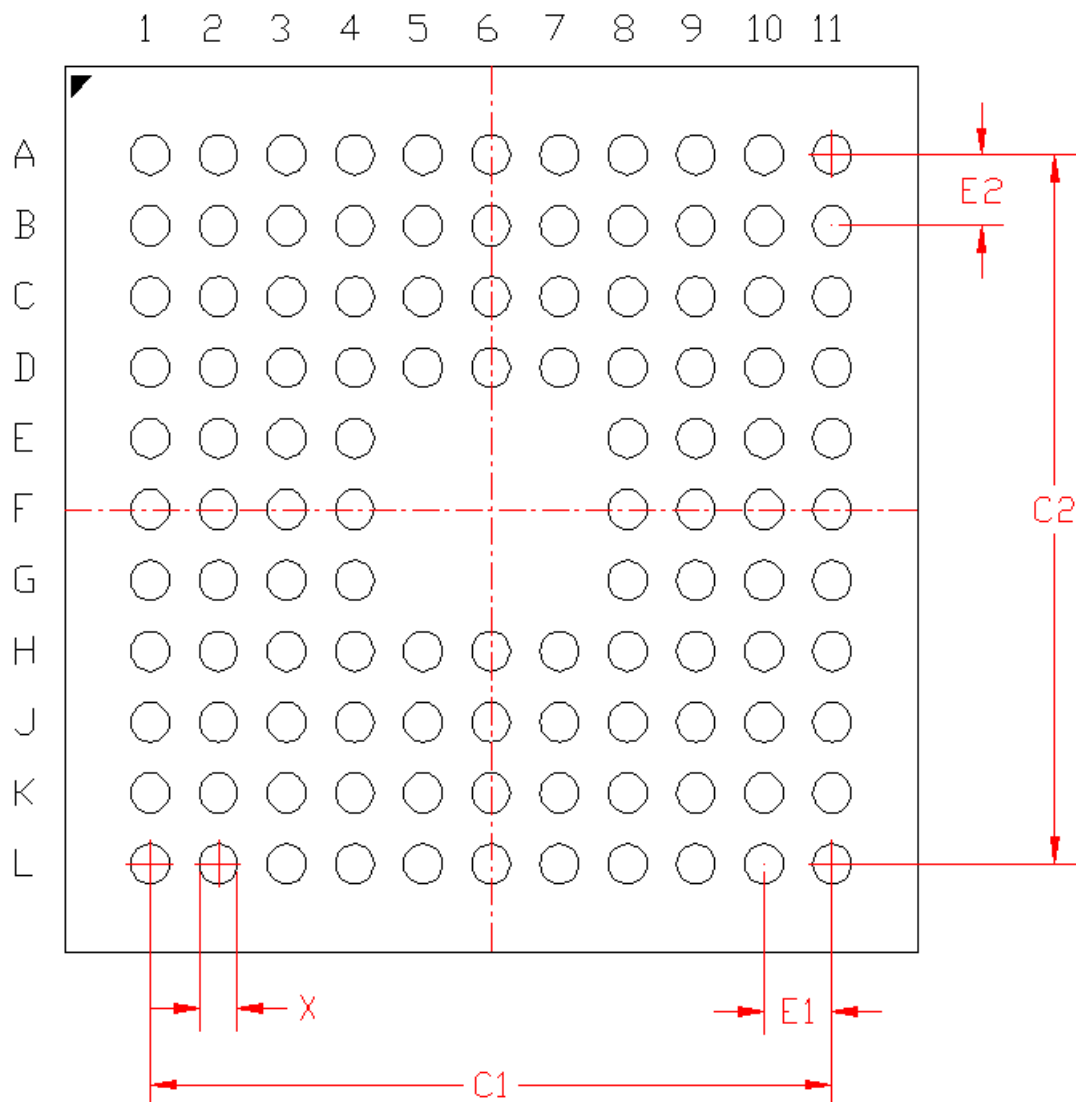


Figure 9.2. BGA112 PCB Land Pattern Drawing

Table 12.2. QFN64 PCB Land Pattern Dimensions

Dimension	Typ
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	7.30
Y2	7.30

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μ m minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
8. A 3x3 array of 1.45 mm square openings on a 2.00 mm pitch can be used for the center ground pad.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.