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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	121
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	152-VFBGA
Supplier Device Package	152-BGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024il152-b

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1. Feature List

The EFM32GG11 highlighted features are listed below.

- ARM Cortex-M4 CPU platform
 - High performance 32-bit processor @ up to 72 MHz
 - DSP instruction support and Floating Point Unit
 - Memory Protection Unit
 - Wake-up Interrupt Controller
- Flexible Energy Management System
 - + 80 $\mu\text{A}/\text{MHz}$ in Active Mode (EM0)
 - 2.1 µA EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
- Integrated DC-DC buck converter
- Up to 2048 kB flash program memory
 - Dual-bank with read-while-write support
- Up to 512 kB RAM data memory
 - 256 kB with ECC (SEC-DED)
- Octal/Quad-SPI Flash Memory Interface
 - Supports 3 V and 1.8 V memories
 - 1/2/4/8-bit data bus
 - Quad-SPI Execute In Place (XIP)
- Communication Interfaces
 - Low-energy Universal Serial Bus (USB) with Device and Host support
 - Fully USB 2.0 compliant
 - On-chip PHY and embedded 5V to 3.3V regulator
 - Crystal-free Device mode operation
 - Patent-pending Low-Energy Mode (LEM)
 - SD/MMC/SDIO Host Controller
 - SD v3.01, SDIO v3.0 and MMC v4.51
 - 1/4/8-bit bus width
 - 10/100 Ethernet MAC with MII/RMII interface
 - IEEE1588-2008 precision time stamping
 - Energy Efficient Ethernet (802.3az)
 - Up to 2× CAN Bus Controller
 - Version 2.0A and 2.0B up to 1 Mbps
 - 6× Universal Synchronous/Asynchronous Receiver/ Transmitter
 - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
 - · Triple buffered full/half-duplex operation with flow control
 - Ultra high speed (36 MHz) operation on one instance
 - 2× Universal Asynchronous Receiver/ Transmitter
 - 2× Low Energy UART
 - · Autonomous operation with DMA in Deep Sleep Mode
 - 3× I²C Interface with SMBus support
 - Address recognition in EM3 Stop Mode

- Up to 144 General Purpose I/O Pins
 - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
 - Configurable peripheral I/O locations
 - 5 V tolerance on select pins
 - Asynchronous external interrupts
 - · Output state retention and wake-up from Shutoff Mode
- Up to 24 Channel DMA Controller
- Up to 24 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling
- External Bus Interface for up to 4x256 MB of external memory mapped space
 - TFT Controller with Direct Drive
 - Per-pixel alpha-blending engine
- Hardware Cryptography
 - AES 128/256-bit keys
 - ECC B/K163, B/K233, P192, P224, P256
 - SHA-1 and SHA-2 (SHA-224 and SHA-256)
 - True Random Number Generator (TRNG)
- Hardware CRC engine
 - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- Security Management Unit (SMU)
 - · Fine-grained access control for on-chip peripherals
- Integrated Low-energy LCD Controller with up to 8×36 segments
 - · Voltage boost, contrast and autonomous animation
 - Patented low-energy LCD driver
- Backup Power Domain
 - RTCC and retention registers in a separate power domain, available down to energy mode EM4H
 - Operation from backup battery when main power absent/ insufficient
- Ultra Low-Power Precision Analog Peripherals
 - 2× 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
 - · On-chip temperature sensor
 - 2× 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
 - Digital to Analog Current Converter (IDAC)
 - Up to 4× Analog Comparator (ACMP)
 - Up to 4× Operational Amplifier (OPAMP)
 - Robust current-based capacitive sensing with up to 64 inputs and wake-on-touch (CSEN)
 - Up to 108 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
 - Supply Voltage Monitor

3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Giant Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 μ A and 64 μ A with several ranges consisting of various step sizes.

3.8.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per singleended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.8 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x36 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32GG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor with FPU achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 2048 kB flash program memory
 - · Dual-bank memory with read-while-write support
- Up to 512 kB RAM data memory
- · Configuration and event handling of all modules
- · 2-pin Serial-Wire or 4-pin JTAG debug interface

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Storage temperature range	T _{STG}		-50	—	150	°C
Voltage on supply pins other than VREGI and VBUS	V _{DDMAX}		-0.3	_	3.8	V
Voltage ramp rate on any supply pin	V _{DDRAMPMAX}		_	—	1	V / µs
DC voltage on any GPIO pin	V _{DIGPIN}	5V tolerant GPIO pins ^{1 2 3}	-0.3	_	Min of 5.25 and IOVDD +2	V
		LCD pins ³	-0.3	_	Min of 3.8 and IOVDD +2	V
		Standard GPIO pins	-0.3	_	IOVDD+0.3	V
Total current into VDD power lines	I _{VDDMAX}	Source			200	mA
Total current into VSS ground lines	IVSSMAX	Sink			200	mA
Current per I/O pin	I _{IOMAX}	Sink	_	_	50	mA
		Source	_	_	50	mA
Current for all I/O pins	I _{IOALLMAX}	Sink	_	_	200	mA
		Source	_	_	200	mA
Junction temperature	TJ	-G grade devices	-40	_	105	°C
		-I grade devices	-40	_	125	°C
Voltage on regulator supply pins VREGI and VBUS	V _{VREGI}		-0.3		5.5	V

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

 Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.

3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
SCLK period ^{1 3 2}	t _{SCLK}		6 * t _{HFPERCLK}	—	—	ns
SCLK high time ^{1 3 2}	t _{SCLK_HI}		2.5 * t _{HFPERCLK}	—	—	ns
SCLK low time ^{1 3 2}	t _{SCLK_LO}		2.5 * t _{HFPERCLK}	—	—	ns
CS active to MISO ^{1 3}	t _{CS_ACT_MI}		24	_	69	ns
CS disable to MISO ^{1 3}	t _{CS_DIS_MI}		19	_	175	ns
MOSI setup time ^{1 3}	t _{SU_MO}		7	_	—	ns
MOSI hold time ^{1 3 2}	t _{H_MO}		6	_	—	ns
SCLK to MISO ^{1 3 2}	t _{SCLK_MI}		16 + 1.5 * t _{HFPERCLK}	—	43 + 2.5 * ^t HFPERCLK	ns

Table 4.35. SPI Slave Timing

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).

2. t_{HFPERCLK} is one period of the selected HFPERCLK.

3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).



Figure 4.2. SPI Slave Timing Diagram

SDIO DDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 30 pF on all pins.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Clock frequency during data transfer	F _{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	-	_	20	MHz
		Using HFXO			TBD	MHz
Clock low time	t _{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	_	_	ns
		Using HFXO	TBD	_	_	ns
Clock high time	t _{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6		_	ns
		Using HFXO	TBD	_	_	ns
Clock rise time	t _R		1.69	6.52		ns
Clock fall time	t _F		1.42	4.96	_	ns
Input setup time, CMD valid to SD_CLK	t _{ISU}		6			ns
Input hold time, SD_CLK to CMD change	t _{IH}		1.8			ns
Output delay time, SD_CLK to CMD valid	t _{ODLY}		0		16	ns
Output hold time, SD_CLK to CMD change	t _{он}		0.8	_	_	ns
Input setup time, DAT[0:3] valid to SD_CLK	t _{ISU2X}		6			ns
Input hold time, SD_CLK to DAT[0:3] change	t _{IH2X}		1.5			ns
Output delay time, SD_CLK to DAT[0:3] valid	t _{ODLY2X}		0	_	16	ns
Output hold time, SD_CLK to DAT[0:3] change	t _{OH2X}		0.8	_	_	ns

Table 4.49. SDIO DS Mode Timing (Location 0)



Figure 4.17. SDIO MMC SDR Mode Timing

4.1.28.2 QSPI DDR Mode

QSPI DDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 35, RX DLL = 70, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.56. QSPI DDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Half SCLK period	T/2	HFXO	(1/F _{SCLK}) * 0.4 - 0.4	—	_	ns
		HFRCO, AUXHFRCO, USHFRCO	(1/F _{SCLK}) * 0.44	—	_	ns
Output valid	t _{OV}		—	_	T/2 - 5.0	ns
Output hold	t _{OH}		T/2 - 39.4	_	_	ns
Input setup	t _{SU}		33.1	_	_	ns
Input hold	t _H		-0.9			ns

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 µH, CDCDC = 4.7 µF, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz



Figure 4.29. DC-DC Converter Typical Performance Characteristics

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	K2	GPIO (5V)	PE0	K12	GPIO (5V)
VREGSW	K13	DCDC regulator switching node	PC2	L1	GPIO (5V)
PC3	L2	GPIO (5V)	PA7	L3	GPIO
PB9	L13	GPIO (5V)	PB10	L14	GPIO (5V)
PD1	L17	GPIO	PC6	L18	GPIO
PC7	L19	GPIO	VREGVSS	L20	Voltage regulator VSS
PB7	M1	GPIO	PC4	M2	GPIO
PA8	M3	GPIO	PA10	M4	GPIO
PA13	M5	GPIO (5V)	PA14	M6	GPIO
RESETn	M7	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB12	M8	GPIO
PD0	M9	GPIO (5V)	PD2	M10	GPIO (5V)
PD3	M11	GPIO	PD4	M12	GPIO
PD8	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	BODEN	N7	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.
PB13	N8	GPIO	PB14	N9	GPIO
AVDD	N10	Analog power supply.	PD5	N11	GPIO
PD6	N12	GPIO	PD7	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.6 EFM32GG11B4xx in BGA112 Device Pinout

1	2	3	4	5	6	7	8	9	10	11
• (1)	(TA	(T)	759	29	(FT)	255	(eV4	SEA)	(2)	(T)
PE-	per FE13	pt-	PE8	60-)	pr8	pr pr6	PT-	PL DE5	pr-	pr.
(Aq)	(PAO)	PEIO	2013	6013	(PF9)	() (155)	pF2	PE6	PC19	PC1
(PA3)	PA2	PB15	(15 ⁵)	LOVODI	(P09)	LOVDDO	PF1	(PET)	PC8	(⁰)9
PAG	PAS	PAA	P80				(PFO)	PEO	PEL	PE3
PBI	PB2	PB3	(PBA)				pupp	455	PE2	DECOUPLE
(PB5)	PB6	155	101002				101000	155	<i>6</i> 09	(PC1)
(PC)	PC2	6014	(TAG)	849	N55	LOVDDO	(PD8)	PD5	<i>b0e</i>	109
PCJ	PC3	013	PAIZ	(PA9)	PA10	(PB9)	PB10	605	(PD3)	(P04)
PBT	PCA	ELA9	VSS	(A)	RESETIN	VSS	AVIDO	AVOD	VSS	(p01)
PB8	PCS	PALA	TONDO	PB1	PB1 3	V55)	6813	6B 1 4	AVDD	600
	1 (1) (1) (1) (1) (1) (1) (1) (1	1 2 (1) (1) (1) (1) (1) (1) (1) (1)	1 2 3 623 623 623 623 623 623 623 623 623 624 623 623 625 626 623 626 626 623 626 626 623 626 626 626 626 626 626 626 626 626 626 626 626 626 626 626 626 626 626 626 626 626 626 626 626	1 2 3 4 	1 2 3 4 5	1 2 3 4 5 6	1 2 3 4 5 6 7	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$\begin{array}{cccccccccccccccccccccccccccccccccccc$

Figure 5.6. EFM32GG11B4xx in BGA112 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.6. EFM32GG11B4xx in BGA112 Device Pino
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD10	A5	GPIO	PF7	A6	GPIO
PF5	A7	GPIO	PF12	A8	GPIO
PE4	A9	GPIO	PF10	A10	GPIO (5V)
PF11	A11	GPIO (5V)	PA15	B1	GPIO
PE13	B2	GPIO	PE11	В3	GPIO



Figure 5.11. EFM32GG11B3xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.11. EFM32GG11B3xx in QFP100 Device Pinor	ut
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO



Figure 5.16. EFM32GG11B8xx in QFN64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VSS	0	Ground	PA0	1	GPIO
PA1	2	GPIO	PA2	3	GPIO
PA3	4	GPIO	PA4	5	GPIO
PA5	6	GPIO	PA6	7	GPIO
IOVDD0	8 27 55	Digital IO power supply 0.	PB3	9	GPIO
PB4	10	GPIO	PB5	11	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB6	12	GPIO	PC4	13	GPIO
PC5	14	GPIO	PB7	15	GPIO
PB8	16	GPIO	PA12	17	GPIO (5V)
PA13	18	GPIO (5V)	PA14	19	GPIO
RESETn	20	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB11	21	GPIO
PB12	22	GPIO	AVDD	23 27	Analog power supply.
PB13	24	GPIO	PB14	25	GPIO
PD0	28	GPIO (5V)	PD1	29	GPIO
PD2	30	GPIO (5V)	PD3	31	GPIO
PD4	32	GPIO	PD5	33	GPIO
PD6	34	GPIO	PD7	35	GPIO
PD8	36	GPIO	PC6	37	GPIO
PC7	38	GPIO	DVDD	39	Digital power supply.
DECOUPLE	40	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE4	41	GPIO
PE5	42	GPIO	PE6	43	GPIO
PE7	44	GPIO	VREGI	45	Input to 5 V regulator.
VREGO	46	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs	PF10	47	GPIO (5V)
PF11	48	GPIO (5V)	PF0	49	GPIO (5V)
PF1	50	GPIO (5V)	PF2	51	GPIO
VBUS	52	USB VBUS signal and auxiliary input to 5 V regulator.	PF12	53	GPIO
PF5	54	GPIO	PE8	56	GPIO
PE9	57	GPIO	PE10	58	GPIO
PE11	59	GPIO	PE12	60	GPIO
PE13	61	GPIO	PE14	62	GPIO
PE15	63	GPIO	PA15	64	GPIO
Note:		·			

1. GPIO with 5V tolerance are indicated by (5V).

GPIO Name	Pin Alternate Functionality / Description					
	Analog	EBI	Timers	Communication	Other	
PD15		EBI_NANDREn #1	TIM2_CDTI2 #1 TIM3_CC0 #7 WTIM0_CDTI0 #1 PCNT1_S0IN #2	ETH_TSUEXTCLK #1 CAN0_TX #5 US5_CTS #1 I2C0_SCL #3		
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSACMP1Y BU- SACMP1X	EBI_ARDY #4	TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 TIM5_CC2 #5 WTIM3_CC2 #2 PCNT0_S0IN #0 PCNT2_S1IN #4	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3 U1_RX #0 I2C2_SCL #6	LES_CH13 PRS_CH21 #1 ACMP3_O #3	
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSACMP1Y BU- SACMP1X		TIM1_CC3 #0 TIM5_CC1 #5 WTIM3_CC1 #2 PCNT2_S0IN #4	CAN1_RX #4 US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3 U1_TX #0 I2C2_SDA #6	CMU_CLK0 #1 LES_CH12 PRS_CH20 #1	
PC11	BUSACMP1Y BU- SACMP1X	EBI_ALE #4 EBI_ALE #5 EBI_A23 #1	TIM5_CC0 #5 WTIM3_CC0 #2	CAN1_TX #4 US0_TX #2 I2C1_SDA #4	LES_CH11 PRS_CH19#1	
PA3	BUSAY BUSBX LCD_SEG16	EBI_AD12 #0 EBI_VSNC #3	TIM0_CDTI0 #0 TIM3_CC0 #5	ETH_RMIIREFCLK #0 ETH_MIITXD1 #0 SDIO_DAT3 #1 US3_CS #0 U0_TX #2 QSPI0_DQ1 #1	CMU_CLK2 #1 CMU_CLK10 #1 CMU_CLK2 #4 LES_ALTEX2 PRS_CH9 #1 ETM_TD1 #3	
PG2	BUSACMP2Y BU- SACMP2X	EBI_AD02 #2	TIM6_CC2 #0 TIM2_CDTI2 #3 WTIM0_CC0 #2 LE- TIM1_OUT0 #7	ETH_MIITXD2 #1 US3_CLK #4 QSPI0_DQ1 #2	CMU_CLK0 #3	
PG1	BUSACMP2Y BU- SACMP2X	EBI_AD01 #2	TIM6_CC1 #0 TIM2_CDTI1 #3 WTIM0_CDTI2 #1 LETIM1_OUT1 #6	ETH_MIITXD3 #1 US3_RX #4 QSPI0_DQ0 #2	CMU_CLK1 #3	
PC10	BUSACMP1Y BU- SACMP1X	EBI_A10 #2 EBI_A22 #1	TIM2_CC2 #2 TIM5_CC2 #4 WTIM3_CC2 #1	CAN1_TX #3 US0_RX #2	LES_CH10 PRS_CH18 #1	
PC9	BUSACMP1Y BU- SACMP1X	EBI_A09 #2 EBI_A21 #1 EBI_A27 #3	TIM2_CC1 #2 TIM5_CC1 #4 WTIM3_CC1 #1	CAN1_RX #3 US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2	
PC8	BUSACMP1Y BU- SACMP1X	EBI_A08 #2 EBI_A15 #0 EBI_A20 #1 EBI_A26 #3	TIM2_CC0 #2 TIM5_CC0 #4 WTIM3_CC0 #1	US0_CS #2	LES_CH8 PRS_CH4 #0	
PA4	BUSBY BUSAX LCD_SEG17	EBI_AD13 #0 EBI_HSNC #3	TIM0_CDTI1 #0 TIM3_CC1 #5	ETH_RMIICRSDV #0 ETH_MIITXD0 #0 SDIO_DAT4 #1 US3_CTS #0 U0_RX #2 QSPI0_DQ2 #1	LES_ALTEX3 PRS_CH16 #0 ETM_TD2 #3	
PG4	BUSACMP2Y BU- SACMP2X	EBI_AD04 #2	TIM6_CDTI1 #0 WTIM0_CC2 #2	ETH_MIITXD0 #1 US3_CTS #4 QSPI0_DQ3 #2		

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US5 RX	0: PE9 1: PA7		USART5 Asynchronous Receive.
	2: PB1 3: PH11		USART5 Synchronous mode Master Input / Slave Output (MISO).
US5_TX	0: PE8 1: PA6		USART5 Asynchronous Transmit. Also used as receive input in half duplex communica- tion.
	2. PF 15 3: PH10		USART5 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	0: PF10		USB D- pin.
USB_DP	0: PF11		USB D+ pin.
USB_ID	0: PF12		USB ID pin.
USB_VBUSEN	0: PF5		USB 5 V VBUS enable.
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6 2: PG2 3: PG8	4: PC15 5: PB0 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5 1: PD13 2: PG3 3: PG9	4: PF0 5: PB1 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.

Table 6.2. BGA192 PCB Land Pattern Dimensions

Dimension	Min	Nom	Мах	
Х	0.20			
C1	6.00			
C2	6.00			
E1		0.4		
E2		0.4		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.

3. This Land Pattern Design is based on the IPC-7351 guidelines.

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

6. The stencil thickness should be 0.125 mm (5 mils).

7. The ratio of stencil aperture to land pad size should be 1:1.

8. A No-Clean, Type-3 solder paste is recommended.

9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9.2 BGA112 PCB Land Pattern



Figure 9.2. BGA112 PCB Land Pattern Drawing

Table 11.2. TQFP64 PCB Land Pattern Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50	BSC
x	0.20	0.30
Y	1.40	1.50

Note:

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. This Land Pattern Design is based on the IPC-7351 guidelines.
- 3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
- 4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.5. The stencil thickness should be 0.125 mm (5 mils).
- 6. The ratio of stencil aperture to land pad size can be 1:1 for all pads.
- 7. A No-Clean, Type-3 solder paste is recommended.
- 8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11.3 TQFP64 Package Marking



Figure 11.3. TQFP64 Package Marking

The package marking consists of:

- PPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.

Dimension	Min	Тур	Мах		
A	0.70	0.75	0.80		
A1	0.00	_	0.05		
b	0.20	0.25	0.30		
A3	0.203 REF				
D		9.00 BSC			
е		0.50 BSC			
E	9.00 BSC				
D2	7.10	7.20	7.30		
E2	7.10	7.20	7.30		
L	0.40	0.45	0.50		
L1	0.00	_	0.10		
ааа	0.10				
bbb	0.10				
ссс	0.10				
ddd	0.05				
eee	0.08				

Table 12.1. QFN64 Package Dimensions

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.