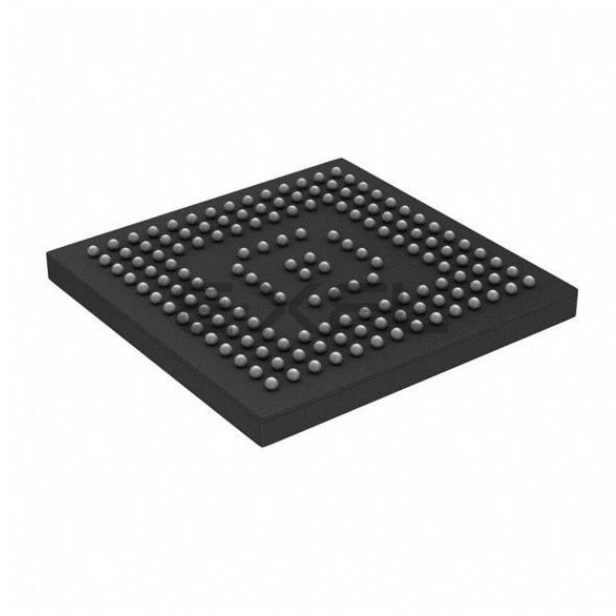

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 121 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.8V |
| Data Converters | A/D 16x12b SAR; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 152-VFBGA |
| Supplier Device Package | 152-BGA (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024il152-br |

# 1. Feature List

The EFM32GG11 highlighted features are listed below.

- **ARM Cortex-M4 CPU platform**
  - High performance 32-bit processor @ up to 72 MHz
  - DSP instruction support and Floating Point Unit
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 80 µA/MHz in Active Mode (EM0)
  - 2.1 µA EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
- **Integrated DC-DC buck converter**
- **Up to 2048 kB flash program memory**
  - Dual-bank with read-while-write support
- **Up to 512 kB RAM data memory**
  - 256 kB with ECC (SEC-DED)
- **Octal/Quad-SPI Flash Memory Interface**
  - Supports 3 V and 1.8 V memories
  - 1/2/4/8-bit data bus
  - Quad-SPI Execute In Place (XIP)
- **Communication Interfaces**
  - Low-energy Universal Serial Bus (USB) with Device and Host support
    - Fully USB 2.0 compliant
    - On-chip PHY and embedded 5V to 3.3V regulator
    - Crystal-free Device mode operation
    - Patent-pending Low-Energy Mode (LEM)
  - SD/MMC/SDIO Host Controller
    - SD v3.01, SDIO v3.0 and MMC v4.51
    - 1/4/8-bit bus width
  - 10/100 Ethernet MAC with MII/RMII interface
    - IEEE1588-2008 precision time stamping
    - Energy Efficient Ethernet (802.3az)
  - Up to 2× CAN Bus Controller
    - Version 2.0A and 2.0B up to 1 Mbps
  - 6× Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
    - Triple buffered full/half-duplex operation with flow control
    - Ultra high speed (36 MHz) operation on one instance
  - 2× Universal Asynchronous Receiver/ Transmitter
  - 2× Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 3× $I^2C$ Interface with SMBus support
    - Address recognition in EM3 Stop Mode
- **Up to 144 General Purpose I/O Pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 5 V tolerance on select pins
  - Asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **Up to 24 Channel DMA Controller**
- **Up to 24 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **External Bus Interface for up to 4x256 MB of external memory mapped space**
  - TFT Controller with Direct Drive
  - Per-pixel alpha-blending engine
- **Hardware Cryptography**
  - AES 128/256-bit keys
  - ECC B/K163, B/K233, P192, P224, P256
  - SHA-1 and SHA-2 (SHA-224 and SHA-256)
  - True Random Number Generator (TRNG)
- **Hardware CRC engine**
  - Single-cycle computation with 8/16/32-bit data and 16-bit (programmable)/32-bit (fixed) polynomial
- **Security Management Unit (SMU)**
  - Fine-grained access control for on-chip peripherals
- **Integrated Low-energy LCD Controller with up to 8×36 segments**
  - Voltage boost, contrast and autonomous animation
  - Patented low-energy LCD driver
- **Backup Power Domain**
  - RTCC and retention registers in a separate power domain, available down to energy mode EM4H
  - Operation from backup battery when main power absent/ insufficient
- **Ultra Low-Power Precision Analog Peripherals**
  - 2× 12-bit 1 Msamples/s Analog to Digital Converter (ADC)
    - On-chip temperature sensor
  - 2× 12-bit 500 ksamples/s Digital to Analog Converter (VDAC)
  - Digital to Analog Current Converter (IDAC)
  - Up to 4× Analog Comparator (ACMP)
  - Up to 4× Operational Amplifier (OPAMP)
  - Robust current-based capacitive sensing with up to 64 inputs and wake-on-touch (CSEN)
  - Up to 108 GPIO pins are analog-capable. Flexible analog peripheral-to-pin routing via Analog Port (APORT)
  - Supply Voltage Monitor

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode[3] | $I_{ACTIVE\_LPM}$ | 32 MHz HFRCO, CPU running while loop from flash | — | 82 | — | µA/MHz |
| | | 26 MHz HFRCO, CPU running while loop from flash | — | 83 | — | µA/MHz |
| | | 16 MHz HFRCO, CPU running while loop from flash | — | 88 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 257 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1] | $I_{ACTIVE\_CCM\_VS}$ | 19 MHz HFRCO, CPU running while loop from flash | — | 117 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 1231 | — | µA/MHz |
| Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode[3] | $I_{ACTIVE\_LPM\_VS}$ | 19 MHz HFRCO, CPU running while loop from flash | — | 72 | — | µA/MHz |
| | | 1 MHz HFRCO, CPU running while loop from flash | — | 219 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2] | $I_{EM1\_DCM}$ | 72 MHz HFRCO | — | 42 | — | µA/MHz |
| | | 50 MHz crystal | — | 46 | — | µA/MHz |
| | | 48 MHz HFRCO | — | 46 | — | µA/MHz |
| | | 32 MHz HFRCO | — | 53 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 57 | — | µA/MHz |
| | | 16 MHz HFRCO | — | 72 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 663 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode[3] | $I_{EM1\_LPM}$ | 32 MHz HFRCO | — | 42 | — | µA/MHz |
| | | 26 MHz HFRCO | — | 43 | — | µA/MHz |
| | | 16 MHz HFRCO | — | 48 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 219 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2] | $I_{EM1\_DCM\_VS}$ | 19 MHz HFRCO | — | 60 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 637 | — | µA/MHz |
| Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode[3] | $I_{EM1\_LPM\_VS}$ | 19 MHz HFRCO | — | 39 | — | µA/MHz |
| | | 1 MHz HFRCO | — | 190 | — | µA/MHz |
| Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode[3] | $I_{EM2\_VS}$ | Full 512 kB RAM retention and RTCC running from LFXO | — | 2.8 | — | µA |
| | | Full 512 kB RAM retention and RTCC running from LFRCO | — | 3.1 | — | µA |
| | | 16 kB (1 bank) RAM retention and RTCC running from LFRCO[5] | — | 2.1 | — | µA |
| Current consumption in EM3 mode, with voltage scaling enabled | $I_{EM3\_VS}$ | Full 512 kB RAM retention and CRYOTIMER running from ULFRCO | — | 2.4 | — | µA |

### 4.1.12 General-Purpose I/O (GPIO)

**Table 4.20. General-Purpose I/O (GPIO)**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input low voltage | $V_{IL}$ | GPIO pins | — | — | IOVDD*0.3 | V |
| Input high voltage | $V_{IH}$ | GPIO pins | IOVDD*0.7 | — | — | V |
| Output high voltage relative to IOVDD | $V_{OH}$ | Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK | IOVDD*0.8 | — | — | V |
| | | Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK | IOVDD*0.6 | — | — | V |
| | | Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG | IOVDD*0.8 | — | — | V |
| | | Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG | IOVDD*0.6 | — | — | V |
| Output low voltage relative to IOVDD | $V_{OL}$ | Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK | — | — | IOVDD*0.2 | V |
| | | Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK | — | — | IOVDD*0.4 | V |
| | | Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG | — | — | IOVDD*0.2 | V |
| | | Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG | — | — | IOVDD*0.4 | V |
| Input leakage current | $I_{IOLEAK}$ | All GPIO except LFXO pins, GPIO ≤ IOVDD, T ≤ 85 °C | — | 0.1 | TBD | nA |
| | | LFXO Pins, GPIO ≤ IOVDD, T ≤ 85 °C | — | 0.1 | TBD | nA |
| | | All GPIO except LFXO pins, GPIO ≤ IOVDD, T > 85 °C | — | — | TBD | nA |
| | | LFXO Pins, GPIO ≤ IOVDD, T > 85 °C | — | — | TBD | nA |
| Input leakage current on 5VTOL pads above IOVDD | $I_{5VTOLLEAK}$ | IOVDD < GPIO ≤ IOVDD + 2 V | — | 3.3 | TBD | µA |
| I/O pin pull-up/pull-down resistor | $R_{PUD}$ | | TBD | 40 | TBD | kΩ |
| Pulse width of pulses removed by the glitch suppression filter | $t_{IOGLITCH}$ | | 15 | 25 | 35 | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Start up time | $t_{IDAC\_SU}$ | Output within 1% of steady state value | — | 5 | — | µs |
| Settling time, (output settled within 1% of steady state value), | $t_{IDAC\_SETTLE}$ | Range setting is changed | — | 5 | — | µs |
| | | Step value is changed | — | 1 | — | µs |
| Current consumption[2] | $I_{IDAC}$ | EM0 or EM1 Source mode, excluding output current, Across operating temperature range | — | 11 | TBD | µA |
| | | EM0 or EM1 Sink mode, excluding output current, Across operating temperature range | — | 13 | TBD | µA |
| | | EM2 or EM3 Source mode, excluding output current, T = 25 °C | — | 0.05 | — | µA |
| | | EM2 or EM3 Sink mode, excluding output current, T = 25 °C | — | 0.07 | — | µA |
| | | EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C | — | 11 | — | µA |
| | | EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C | — | 13 | — | µA |
| Output voltage compliance in source mode, source current change relative to current sourced at 0 V | $I_{COMP\_SRC}$ | RANGESEL1=0, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-100 mv) | — | 0.11 | — | % |
| | | RANGESEL1=1, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-100 mV) | — | 0.06 | — | % |
| | | RANGESEL1=2, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-150 mV) | — | 0.04 | — | % |
| | | RANGESEL1=3, output voltage = min($V_{IOVDD}$, $V_{AVDD}$[2]-250 mV) | — | 0.03 | — | % |
| Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD | $I_{COMP\_SINK}$ | RANGESEL1=0, output voltage = 100 mV | — | 0.29 | — | % |
| | | RANGESEL1=1, output voltage = 100 mV | — | 0.27 | — | % |
| | | RANGESEL1=2, output voltage = 150 mV | — | 0.12 | — | % |
| | | RANGESEL1=3, output voltage = 250 mV | — | 0.03 | — | % |

**Note:**

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

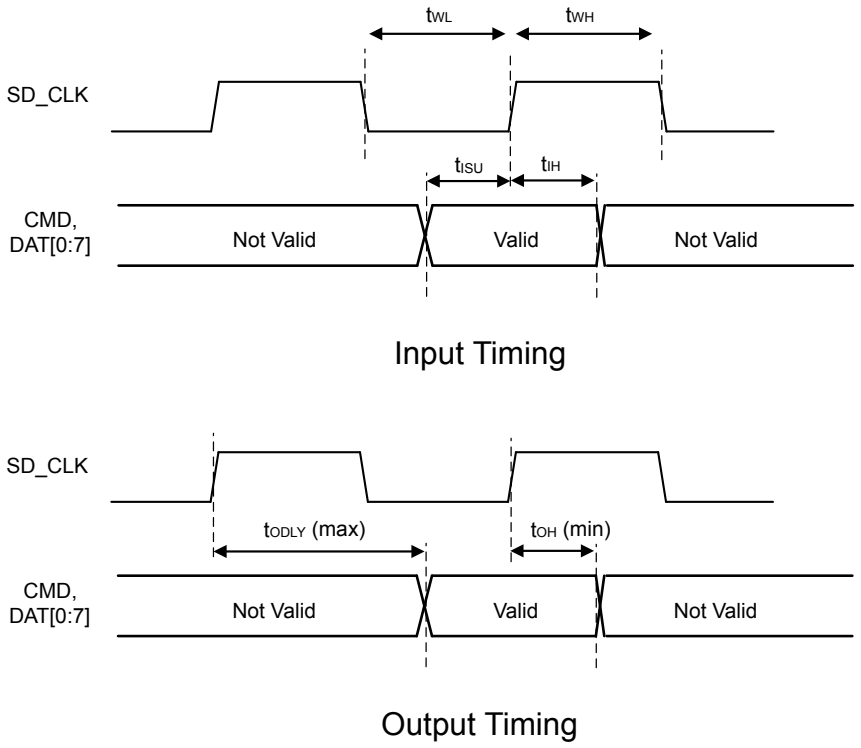


**Figure 4.14. SDIO HS Mode Timing**

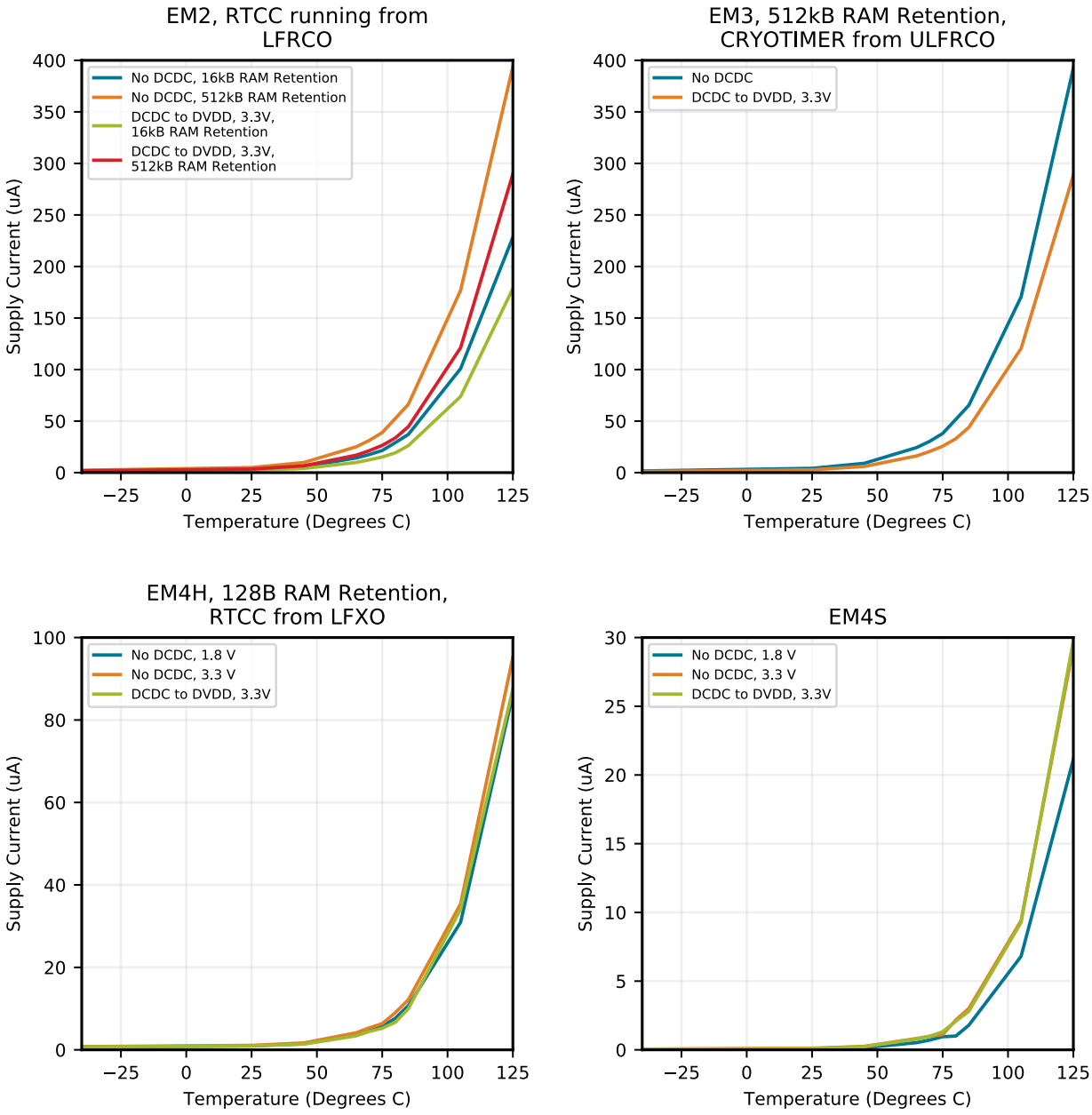


**Figure 4.26. EM2, EM3, EM4H and EM4S Typical Supply Current vs. Temperature**

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PE8 | B4 | GPIO | PD11 | B5 | GPIO |
| PF8 | B6 | GPIO | PF6 | B7 | GPIO |
| VBUS | B8 | USB VBUS signal and auxiliary input to 5 V regulator. | PE5 | B9 | GPIO |
| VREGI | B10 | Input to 5 V regulator. | VREGO | B11 | Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs |
| PA1 | C1 | GPIO | PA0 | C2 | GPIO |
| PE10 | C3 | GPIO | PD13 | C4 | GPIO (5V) |
| PD12 | C5 | GPIO | PF9 | C6 | GPIO |
| VSS | C7<br>D4<br>F9<br>G3<br>G9<br>H6<br>K4<br>K7<br>K10<br>L7 | Ground | PF2 | C8 | GPIO |
| PE6 | C9 | GPIO | PC10 | C10 | GPIO (5V) |
| PC11 | C11 | GPIO (5V) | PA3 | D1 | GPIO |
| PA2 | D2 | GPIO | PB15 | D3 | GPIO (5V) |
| IOVDD1 | D5 | Digital IO power supply 1. | PD9 | D6 | GPIO |
| IOVDD0 | D7<br>G8<br>H7<br>L4 | Digital IO power supply 0. | PF1 | D8 | GPIO (5V) |
| PE7 | D9 | GPIO | PC8 | D10 | GPIO (5V) |
| PC9 | D11 | GPIO (5V) | PA6 | E1 | GPIO |
| PA5 | E2 | GPIO | PA4 | E3 | GPIO |
| PB0 | E4 | GPIO | PF0 | E8 | GPIO (5V) |
| PE0 | E9 | GPIO (5V) | PE1 | E10 | GPIO (5V) |
| PE3 | E11 | GPIO | PB1 | F1 | GPIO |
| PB2 | F2 | GPIO | PB3 | F3 | GPIO |
| PB4 | F4 | GPIO | DVDD | F8 | Digital power supply. |
| PE2 | F10 | GPIO | DECOUPLE | F11 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. |
| PB5 | G1 | GPIO | PB6 | G2 | GPIO |
| IOVDD2 | G4 | Digital IO power supply 2. | PC6 | G10 | GPIO |
| PC7 | G11 | GPIO | PC0 | H1 | GPIO (5V) |
| PC2 | H2 | GPIO (5V) | PD14 | H3 | GPIO (5V) |
| PA7 | H4 | GPIO | PA8 | H5 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PE8 | B4 | GPIO | PD11 | B5 | GPIO |
| PF8 | B6 | GPIO | PF6 | B7 | GPIO |
| PF3 | B8 | GPIO | PE5 | B9 | GPIO |
| PC12 | B10 | GPIO (5V) | PC13 | B11 | GPIO (5V) |
| PA1 | C1 | GPIO | PA0 | C2 | GPIO |
| PE10 | C3 | GPIO | PD13 | C4 | GPIO (5V) |
| PD12 | C5 | GPIO | PF9 | C6 | GPIO |
| VSS | C7<br>D4<br>F9<br>G3<br>G9<br>H6<br>K4<br>K7<br>K10<br>L7 | Ground | PF2 | C8 | GPIO |
| PE6 | C9 | GPIO | PC10 | C10 | GPIO (5V) |
| PC11 | C11 | GPIO (5V) | PA3 | D1 | GPIO |
| PA2 | D2 | GPIO | PB15 | D3 | GPIO (5V) |
| IOVDD1 | D5 | Digital IO power supply 1. | PD9 | D6 | GPIO |
| IOVDD0 | D7<br>G8<br>H7<br>L4 | Digital IO power supply 0. | PF1 | D8 | GPIO (5V) |
| PE7 | D9 | GPIO | PC8 | D10 | GPIO (5V) |
| PC9 | D11 | GPIO (5V) | PA6 | E1 | GPIO |
| PA5 | E2 | GPIO | PA4 | E3 | GPIO |
| PB0 | E4 | GPIO | PF0 | E8 | GPIO (5V) |
| PE0 | E9 | GPIO (5V) | PE1 | E10 | GPIO (5V) |
| PE3 | E11 | GPIO | PB1 | F1 | GPIO |
| PB2 | F2 | GPIO | PB3 | F3 | GPIO |
| PB4 | F4 | GPIO | DVDD | F8 | Digital power supply. |
| PE2 | F10 | GPIO | DECOUPLE | F11 | Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin. |
| PB5 | G1 | GPIO | PB6 | G2 | GPIO |
| IOVDD2 | G4 | Digital IO power supply 2. | PC6 | G10 | GPIO |
| PC7 | G11 | GPIO | PC0 | H1 | GPIO (5V) |
| PC2 | H2 | GPIO (5V) | PD14 | H3 | GPIO (5V) |
| PA7 | H4 | GPIO | PA8 | H5 | GPIO |
| PD8 | H8 | GPIO | PD5 | H9 | GPIO |
| PD6 | H10 | GPIO | PD7 | H11 | GPIO |

| Pin Name | Pin(s) | Description | Pin Name | Pin(s) | Description |
|---|---|---|---|---|---|
| PF1 | 77 | GPIO (5V) | PF2 | 78 | GPIO |
| VBUS | 79 | USB VBUS signal and auxiliary input to 5 V regulator. | PF12 | 80 | GPIO |
| PF5 | 81 | GPIO | PF6 | 84 | GPIO |
| PF7 | 85 | GPIO | PF8 | 86 | GPIO |
| PF9 | 87 | GPIO | PD9 | 88 | GPIO |
| PD10 | 89 | GPIO | PD11 | 90 | GPIO |
| PD12 | 91 | GPIO | PE8 | 92 | GPIO |
| PE9 | 93 | GPIO | PE10 | 94 | GPIO |
| PE11 | 95 | GPIO | PE12 | 96 | GPIO |
| PE13 | 97 | GPIO | PE14 | 98 | GPIO |
| PE15 | 99 | GPIO | PA15 | 100 | GPIO |

**Note:**

1. GPIO with 5V tolerance are indicated by (5V).

| GPIO Name | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|
| | Analog | EBI | Timers | Communication | Other |
| PB0 | BUSBY BUSAX LCD_SEG32 | EBI_AD00 #1 EBI_CS0 #3 EBI_A16 #0 | TIM2_CDTI0 #0 TIM1_CC0 #2 TIM3_CC2 #7 WTIM0_CC0 #5 PCNT0_S0IN #5 PCNT1_S1IN #2 | LEU1_TX #3 | PRS_CH4 #1 ACMP0_O #5 |
| PE0 | BUSDY BUSCX | EBI_A00 #2 EBI_A07 #0 | TIM3_CC0 #1 WTIM1_CC1 #3 PCNT0_S0IN #1 | CAN0_RX #6 U0_TX #1 I2C1_SDA #2 | PRS_CH22 #1 ACMP2_O #1 |
| PC7 | BUSACMP0Y BUSACMP0X OPA3_N | EBI_A06 #0 EBI_A13 #1 EBI_A21 #3 | WTIM1_CC0 #3 | US0_CTS #2 US1_RTS #3 LEU1_RX #0 I2C0_SCL #2 | LES_CH7 PRS_CH15 #1 ETM_TD0 #2 |
| PB1 | BUSAY BUSBX LCD_SEG33 | EBI_AD01 #1 EBI_CS1 #3 EBI_A17 #0 | TIM2_CDTI1 #0 TIM1_CC1 #2 WTIM0_CC1 #5 LE-TIM1_OUT1 #5 PCNT0_S1IN #5 | ETH_MIICRS #0 US5_RX #2 LEU1_RX #3 | PRS_CH5 #1 |
| PB2 | BUSBY BUSAX LCD_SEG34 | EBI_AD02 #1 EBI_CS2 #3 EBI_A18 #0 | TIM2_CDTI2 #0 TIM1_CC2 #2 WTIM0_CC2 #5 LE-TIM1_OUT0 #5 | ETH_MIICOL #0 US1_CS #6 | PRS_CH18 #0 ACMP0_O #6 |
| PB3 | BUSAY BUSBX LCD_SEG20 / LCD_COM4 | EBI_AD03 #1 EBI_CS3 #3 EBI_A19 #0 | TIM1_CC3 #2 WTIM0_CC0 #6 PCNT1_S0IN #1 | ETH_MIICRS #2 ETH_MDIO #0 SDIO_DAT6 #1 US2_TX #1 US3_TX #2 QSPI0_DQ4 #1 | PRS_CH19 #0 ACMP0_O #7 |
| PC6 | BUSACMP0Y BUSACMP0X OPA3_P | EBI_A05 #0 | WTIM1_CC3 #2 | US0_RTS #2 US1_CTS #3 LEU1_TX #0 I2C0_SDA #2 | LES_CH6 PRS_CH14 #1 ETM_TCLK #2 |
| PB4 | BUSBY BUSAX LCD_SEG21 / LCD_COM5 | EBI_AD04 #1 EBI_ARDY #3 EBI_A20 #0 | WTIM0_CC1 #6 PCNT1_S1IN #1 | ETH_MIICOL #2 ETH_MDC #0 SDIO_DAT7 #1 US2_RX #1 QSPI0_DQ5 #1 LEU1_TX #4 | PRS_CH20 #0 |
| PB5 | BUSAY BUSBX LCD_SEG22 / LCD_COM6 | EBI_AD05 #1 EBI_ALE #3 EBI_A21 #0 | WTIM0_CC2 #6 LE-TIM1_OUT0 #4 PCNT0_S0IN #6 | ETH_TSUEXTCLK #0 US0_RTS #4 US2_CLK #1 QSPI0_DQ6 #1 LEU1_RX #4 | PRS_CH21 #0 |
| PB6 | BUSBY BUSAX LCD_SEG23 / LCD_COM7 | EBI_AD06 #1 EBI_WEn #3 EBI_A22 #0 | TIM0_CC0 #3 TIM2_CC0 #4 WTIM3_CC0 #6 LE-TIM1_OUT1 #4 PCNT0_S1IN #6 | ETH_TSUTMRTOG #0 US0_CTS #4 US2_CS #1 QSPI0_DQ7 #1 | PRS_CH12 #1 |
| PD5 | BUSADC0Y BUSADC0X OPA2_OUT | EBI_A09 #1 EBI_A18 #3 | TIM6_CC1 #7 WTIM0_CDTI1 #4 WTIM1_CC3 #1 WTIM2_CC2 #5 | US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3 | PRS_CH11 #2 ETM_TD3 #0 ETM_TD3 #2 |

| Alternate | LOCATION | | |
|---|---|---|---|
| Functionality | 0 - 3 | 4 - 7 | Description |
| EBI_A10 | 0: PE3<br>1: PD6<br>2: PC10<br>3: PB10 | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | 0: PE4<br>1: PD7<br>2: PI6<br>3: PB11 | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | 0: PE5<br>1: PD8<br>2: PI7<br>3: PB12 | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | 0: PE6<br>1: PC7<br>2: PI8<br>3: PD0 | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | 0: PE7<br>1: PE2<br>2: PI9<br>3: PD1 | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | 0: PC8<br>1: PE3<br>2: PI10<br>3: PD2 | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | 0: PB0<br>1: PE4<br>2: PH4<br>3: PD3 | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | 0: PB1<br>1: PE5<br>2: PH5<br>3: PD4 | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | 0: PB2<br>1: PE6<br>2: PH6<br>3: PD5 | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | 0: PB3<br>1: PE7<br>2: PH7<br>3: PD6 | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | 0: PB4<br>1: PC8<br>2: PH8<br>3: PD7 | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | 0: PB5<br>1: PC9<br>2: PH9<br>3: PC7 | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | 0: PB6<br>1: PC10<br>2: PH10<br>3: PE4 | | External Bus Interface (EBI) address output pin 22. |

| Alternate Functionality | Location | Priority |
|---|---|---|
| US2_CLK | 4: PF8<br>5: PF2 | High Speed<br>High Speed |
| US2_CS | 4: PF9<br>5: PF5 | High Speed<br>High Speed |
| US2_RX | 4: PF7<br>5: PF1 | High Speed<br>High Speed |
| US2_TX | 4: PF6<br>5: PF0 | High Speed<br>High Speed |

## 5.22 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 5.20 APORT Connection Diagram on page 211 shows the APORT routing for this device family (note that available features may vary by part number). A complete description of APORT functionality can be found in the Reference Manual.

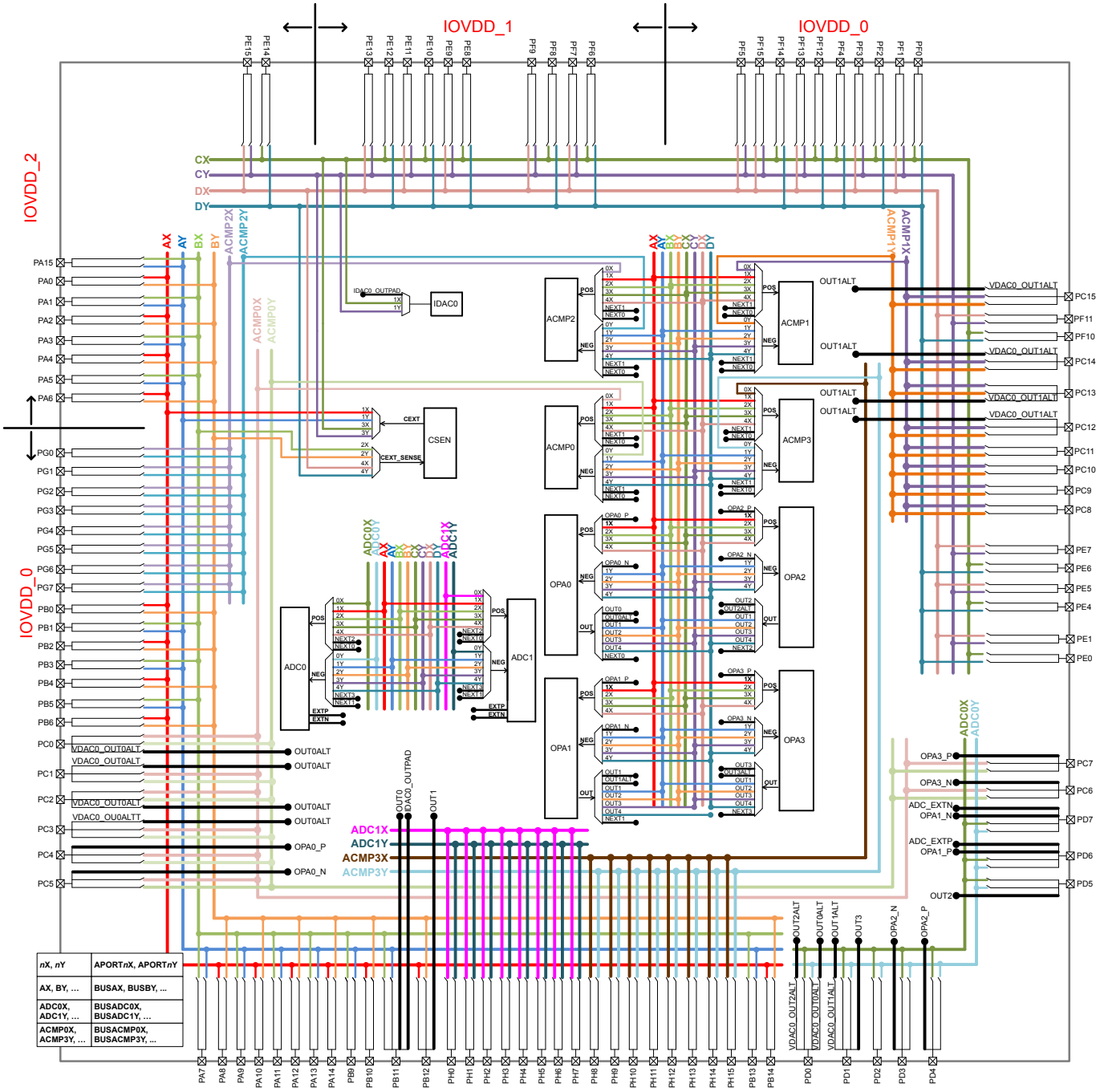


**Figure 5.20. APORT Connection Diagram**

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

**Table 5.25. ACMP2 Bus and Pin Mapping**

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| APORT0X | BUSACMP2X | | | | | | | | | | | | | | | | | | | | | | | | | PG7 | PG6 | PG5 | PG4 | PG3 | PG2 | PG1 | PG0 |
| APORT0Y | BUSACMP2Y | | | | | | | | | | | | | | | | | | | | | | | | | PG7 | PG6 | PG5 | PG4 | PG3 | PG2 | PG1 | PG0 |
| APORT1X | BUSAX | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT1Y | BUSAY | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | |
| APORT2X | BUSBX | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | |
| APORT2Y | BUSBY | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT3X | BUSCX | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | | | PE0 |
| APORT3Y | BUSCY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | | | PE1 | |
| APORT4X | BUSDX | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | | | PE1 | |
| APORT4Y | BUSDY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | | | PE0 |

| Port | Bus | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 | CH0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **VDAC0_OUT1 / OPA1_OUT** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| APORT1Y | BUSAY | PB15 | | PB13 | | PB11 | | PB9 | | | | PB5 | | PB3 | | PB1 | | PA15 | | PA13 | | PA11 | | PA9 | | PA7 | | PA5 | | PA3 | | PA1 | |
| APORT2Y | BUSBY | | PB14 | | PB12 | | PB10 | | | | PB6 | | PB4 | | PB2 | | PB0 | | PA14 | | PA12 | | PA10 | | PA8 | | PA6 | | PA4 | | PA2 | | PA0 |
| APORT3Y | BUSCY | PF15 | | PF13 | | PF11 | | PF9 | | PF7 | | PF5 | | PF3 | | PF1 | | PE15 | | PE13 | | PE11 | | PE9 | | PE7 | | PE5 | | | | PE1 | |
| APORT4Y | BUSDY | | PF14 | | PF12 | | PF10 | | PF8 | | PF6 | | PF4 | | PF2 | | PF0 | | PE14 | | PE12 | | PE10 | | PE8 | | PE6 | | PE4 | | | | PE0 |

# 6. BGA192 Package Specifications

## 6.1 BGA192 Package Dimensions

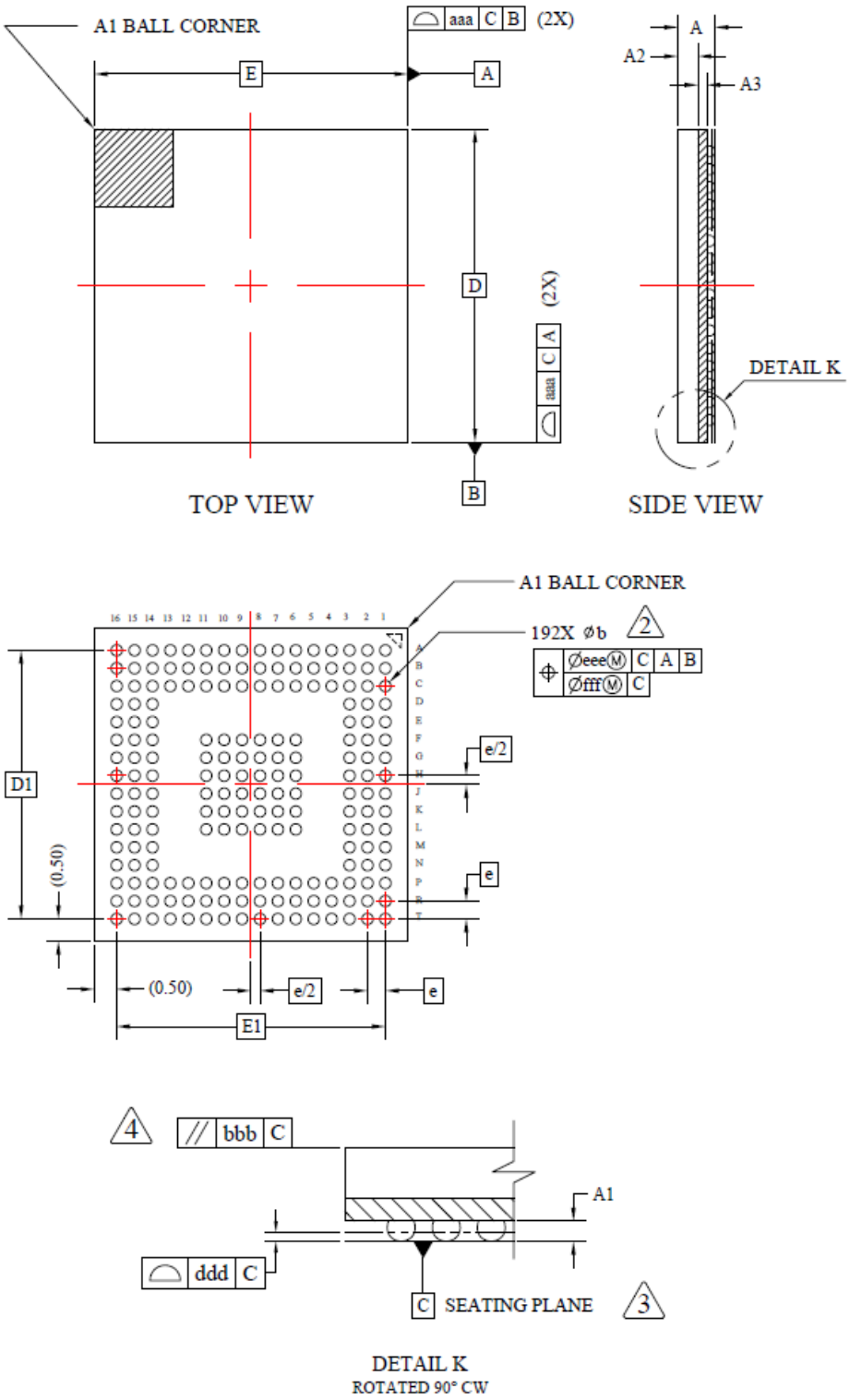


**Figure 6.1. BGA192 Package Drawing**

**Table 6.1. BGA192 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | 0.77 | 0.83 | 0.89 |
| A1 | 0.13 | 0.18 | 0.23 |
| A3 | 0.16 | 0.20 | 0.24 |
| A2 | | 0.45 REF | |
| D | | 7.00 BSC | |
| e | | 0.40 BSC | |
| E | | 7.00 BSC | |
| D1 | | 6.00 BSC | |
| E1 | | 6.00 BSC | |
| b | 0.20 | 0.25 | 0.30 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ddd | | 0.08 | |
| eee | | 0.15 | |
| fff | | 0.05 | |

**Note:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

**Table 7.1. BGA152 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | 0.78 | 0.84 | 0.90 |
| A1 | 0.13 | 0.18 | 0.23 |
| A3 | 0.16 | 0.20 | 0.24 |
| A2 | | 0.45 REF | |
| D | | 8.00 BSC | |
| e | | 0.50 BSC | |
| E | | 8.00 BSC | |
| D1 | | 6.50 BSC | |
| E1 | | 6.50 BSC | |
| b | 0.20 | 0.25 | 0.30 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ddd | | 0.08 | |
| eee | | 0.15 | |
| fff | | 0.05 | |

**Note:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

**Table 10.2. TQFP100 PCB Land Pattern Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| C1 | | 15.4 | |
| C2 | | 15.4 | |
| E | | 0.50 BSC | |
| X | | 0.30 | |
| Y | | 1.50 | |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

### 10.3 TQFP100 Package Marking


**Figure 10.3. TQFP100 Package Marking**

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

**Table 12.1. QFN64 Package Dimensions**

| Dimension | Min | Typ | Max |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | — | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| A3 | 0.203 REF | | |
| D | 9.00 BSC | | |
| e | 0.50 BSC | | |
| E | 9.00 BSC | | |
| D2 | 7.10 | 7.20 | 7.30 |
| E2 | 7.10 | 7.20 | 7.30 |
| L | 0.40 | 0.45 | 0.50 |
| L1 | 0.00 | — | 0.10 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |

**Note:**
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.