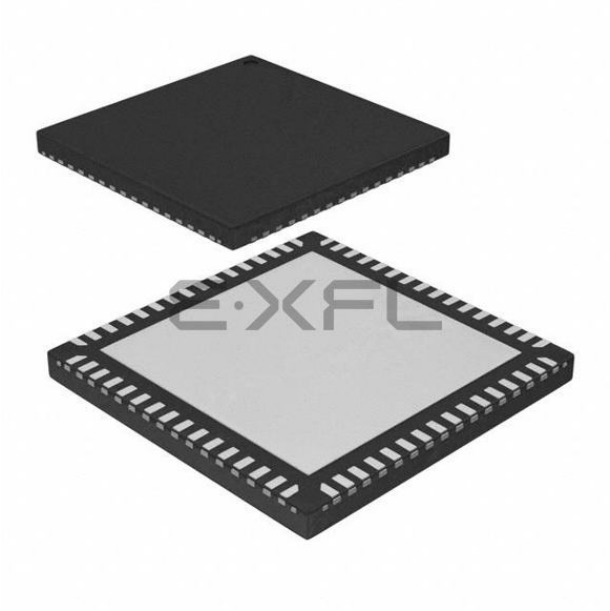

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024im64-b

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	USB	Ethernet	QSPI	SDIO	LCD	GPIO	Package	Temp Range
EFM32GG11B820F2048GL192-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85°C
EFM32GG11B840F1024GL192-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85°C
EFM32GG11B820F2048GL152-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +85°C
EFM32GG11B820F2048IL152-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +125°C
EFM32GG11B840F1024GL152-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +85°C
EFM32GG11B840F1024IL152-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	121	BGA152	-40 to +125°C
EFM32GG11B820F2048GL120-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +85°C
EFM32GG11B820F2048IL120-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +125°C
EFM32GG11B840F1024GL120-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +85°C
EFM32GG11B840F1024IL120-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	95	BGA120	-40 to +125°C
EFM32GG11B820F2048GQ100-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85°C
EFM32GG11B820F2048IQ100-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +125°C
EFM32GG11B840F1024GQ100-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85°C
EFM32GG11B840F1024IQ100-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +125°C
EFM32GG11B820F2048GQ64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +85°C
EFM32GG11B820F2048GM64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +85°C
EFM32GG11B820F2048IQ64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +125°C
EFM32GG11B820F2048IM64-A	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +125°C
EFM32GG11B840F1024GQ64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +85°C
EFM32GG11B840F1024GM64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +85°C
EFM32GG11B840F1024IQ64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	47	QFP64	-40 to +125°C
EFM32GG11B840F1024IM64-A	1024	512	Yes	Yes	Yes	Yes	Yes	Yes	50	QFN64	-40 to +125°C
EFM32GG11B520F2048GL120-A	2048	512	Yes	No	No	No	No	Yes	95	BGA120	-40 to +85°C
EFM32GG11B510F2048GL120-A	2048	384	Yes	No	No	No	No	Yes	95	BGA120	-40 to +85°C
EFM32GG11B520F2048IL120-A	2048	512	Yes	No	No	No	No	Yes	95	BGA120	-40 to +125°C
EFM32GG11B510F2048IL120-A	2048	384	Yes	No	No	No	No	Yes	95	BGA120	-40 to +125°C
EFM32GG11B520F2048GQ100-A	2048	512	Yes	No	No	No	No	Yes	83	QFP100	-40 to +85°C
EFM32GG11B510F2048GQ100-A	2048	384	Yes	No	No	No	No	Yes	83	QFP100	-40 to +85°C
EFM32GG11B520F2048IQ100-A	2048	512	Yes	No	No	No	No	Yes	83	QFP100	-40 to +125°C
EFM32GG11B510F2048IQ100-A	2048	384	Yes	No	No	No	No	Yes	83	QFP100	-40 to +125°C

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4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 µF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.8	—	$V_{VREGVDD_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC accuracy	ACC_{DC}	Low Noise (LN) mode, 1.8 V target output	TBD	—	TBD	V
Regulation window[4]	WIN_{REG}	Low Power (LP) mode, LPCMPBIASEMxx[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 µA	TBD	—	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	TBD	—	TBD	V
Steady-state output ripple	V_R		—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	25	TBD	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

4.1.7.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.9. Current Consumption 1.8 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	72 MHz HFRCO, CPU running Prime from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	140	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	122	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	122	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	126	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	131	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	315	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	107	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	259	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	72 MHz HFRCO	—	57	—	µA/MHz
		50 MHz crystal	—	59	—	µA/MHz
		48 MHz HFRCO	—	59	—	µA/MHz
		32 MHz HFRCO	—	61	—	µA/MHz
		26 MHz HFRCO	—	63	—	µA/MHz
		16 MHz HFRCO	—	68	—	µA/MHz
		1 MHz HFRCO	—	252	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	55	—	µA/MHz
		1 MHz HFRCO	—	207	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.7	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	4.0	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.5	—	µA

4.1.18 Capacitive Sense (CSEN)

Table 4.26. Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single conversion time (1x accumulation)	t_{CNV}	12-bit SAR Conversions	—	20.2	—	µs
		16-bit SAR Conversions	—	26.4	—	µs
		Delta Modulation Conversion (single comparison)	—	1.55	—	µs
Maximum external capacitive load	C_{EXTMAX}	CS0CG=7 (Gain = 1x), including routing parasitics	—	68	—	pF
		CS0CG=0 (Gain = 10x), including routing parasitics	—	680	—	pF
Maximum external series impedance	R_{EXTMAX}		—	1	—	kΩ
Supply current, EM2 bonded conversions, WARMUPMODE=NORMAL, WARMUPCNT=0	I_{CSEN_BOND}	12-bit SAR conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	326	—	nA
		Delta Modulation conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	226	—	nA
		12-bit SAR conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	33	—	nA
		Delta Modulation conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	25	—	nA
Supply current, EM2 scan conversions, WARMUPMODE=NORMAL, WARMUPCNT=0	I_{CSEN_EM2}	12-bit SAR conversions, 20 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	690	—	nA
		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	515	—	nA
		12-bit SAR conversions, 200 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	79	—	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	57	—	nA

4.1.24 USART SPI

SPI Master Timing

Table 4.34. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}	All USARTs except USART2	2 * $t_{HFPERCLK}$	—	—	ns
		USART2	2 * $t_{HFPERBCLK}$	—	—	ns
CS to MOSI [1] [3]	t_{CS_MO}	USART2, location 4, IOVDD = 1.8 V	-3.2	—	6.8	ns
		USART2, location 4, IOVDD = 3.0 V	-2.3	—	6.0	ns
		USART2, location 5, IOVDD = 1.8 V	-8.1	—	6.3	ns
		USART2, location 5, IOVDD = 3.0 V	-7.3	—	4.4	ns
		All other USARTs and locations, IOVDD = 1.8 V	-15	—	13	ns
		All other USARTs and locations, IOVDD = 3.0 V	-13	—	11	ns
SCLK to MOSI [1] [3]	t_{SCLK_MO}	USART2, location 4, IOVDD = 1.8 V	-0.3	—	9.2	ns
		USART2, location 4, IOVDD = 3.0 V	-0.3	—	8.6	ns
		USART2, location 5, IOVDD = 1.8 V	-3.6	—	5.0	ns
		USART2, location 5, IOVDD = 3.0 V	-3.4	—	3.2	ns
		All other USARTs and locations, IOVDD = 1.8 V	-10	—	11	ns
		All other USARTs and locations, IOVDD = 3.0 V	-9	—	11	ns
MISO setup time [1] [3]	t_{SU_MI}	USART2, location 4, IOVDD = 1.8 V	39.7	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	22.4	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	49.2	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	30.0	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	55	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	36	—	—	ns

SPI Slave Timing

Table 4.35. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1 3 2]	t_{SCLK}		6 * $t_{HFPERCLK}$	—	—	ns
SCLK high time[1 3 2]	t_{SCLK_HI}		2.5 * $t_{HFPERCLK}$	—	—	ns
SCLK low time[1 3 2]	t_{SCLK_LO}		2.5 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1 3]	$t_{CS_ACT_MI}$		24	—	69	ns
CS disable to MISO [1 3]	$t_{CS_DIS_MI}$		19	—	175	ns
MOSI setup time [1 3]	t_{SU_MO}		7	—	—	ns
MOSI hold time [1 3 2]	t_{H_MO}		6	—	—	ns
SCLK to MISO [1 3 2]	t_{SCLK_MI}		16 + 1.5 * $t_{HFPERCLK}$	—	43 + 2.5 * $t_{HFPERCLK}$	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

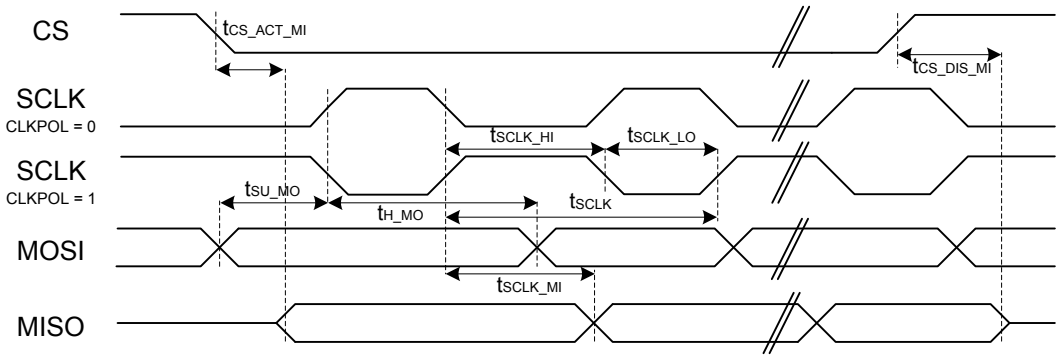

Figure 4.2. SPI Slave Timing Diagram

4.1.27 Serial Data I/O Host Controller (SDIO)

SDIO DS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 40 pF on all pins.

Table 4.46. SDIO DS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	23	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	19.7	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.69	3.23	—	ns
Clock fall time	t_F		1.42	2.79	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}		0	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}		0	—	14	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}		5	—	—	ns

SDIO MMC DDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 7, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 25 pF on all pins.

Table 4.53. SDIO MMC DDR Mode Timing (Location 0, 3V I/O)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.13	2.37	—	ns
Clock fall time	t_F		1.01	2.02	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		5.3	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		2.5	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		3	—	—	ns
Input setup time, DAT[0:7] valid to SD_CLK	t_{ISU2X}		5.3	—	—	ns
Input hold time, SD_CLK to DAT[0:7] change	t_{IH2X}		2.5	—	—	ns
Output delay time, SD_CLK to DAT[0:7] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:7] change	t_{OH2X}		3	—	—	ns

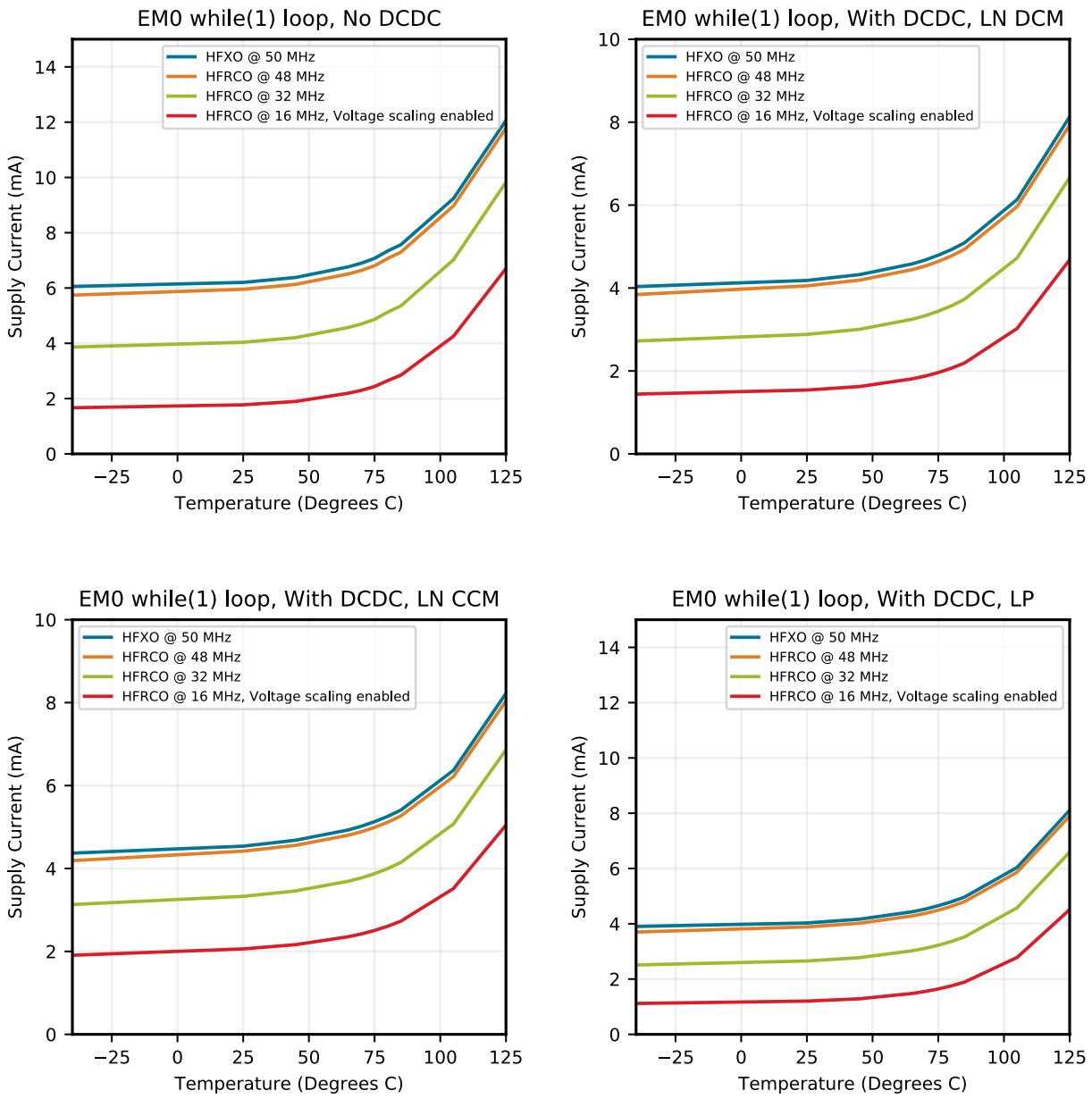

Figure 4.24. EM0 Active Mode Typical Supply Current vs. Temperature

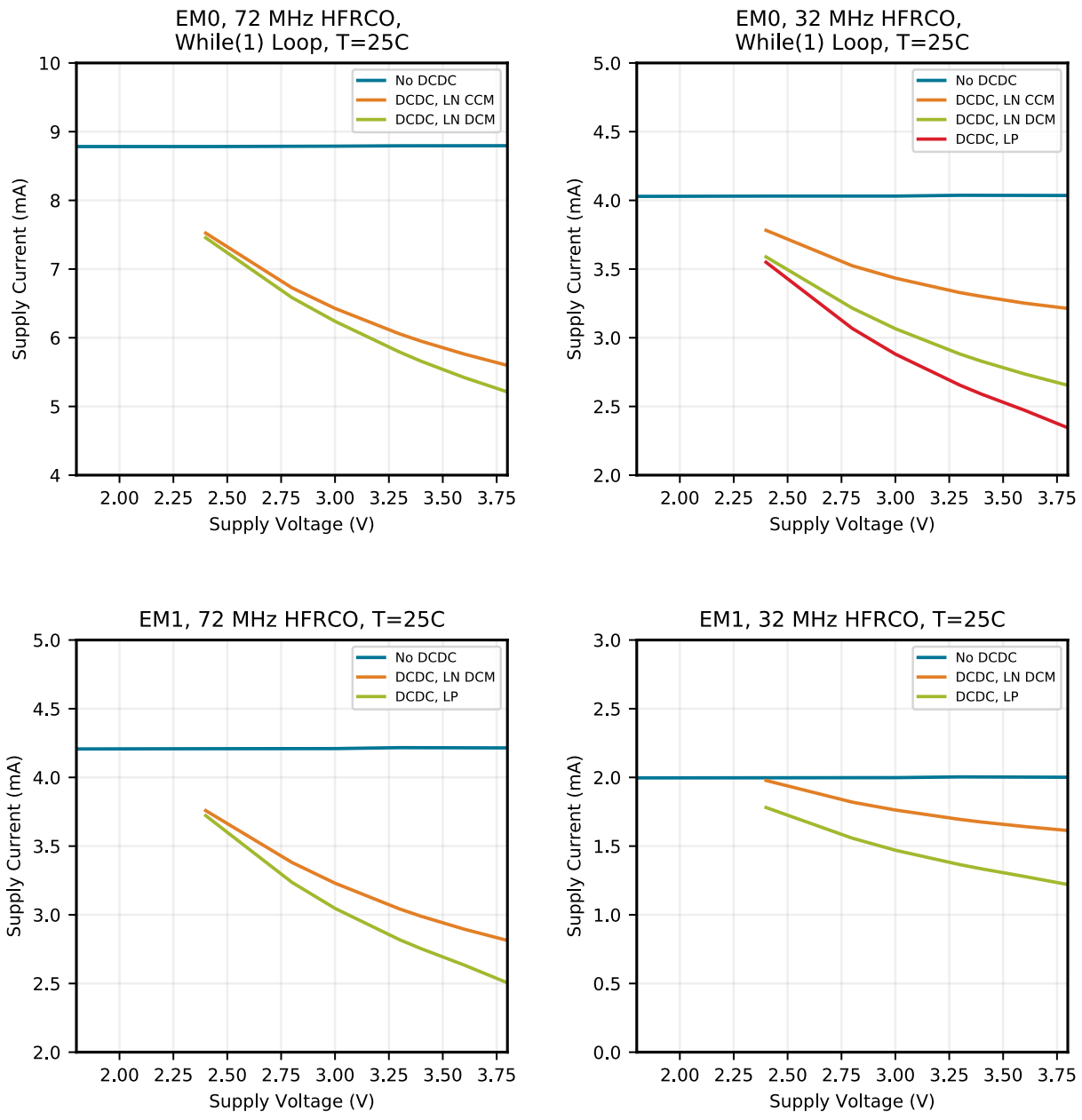

Figure 4.27. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF2	78	GPIO	NC	79	No Connect.
PF12	80	GPIO	PF5	81	GPIO
PF6	84	GPIO	PF7	85	GPIO
PF8	86	GPIO	PF9	87	GPIO
PD9	88	GPIO	PD10	89	GPIO
PD11	90	GPIO	PD12	91	GPIO
PE8	92	GPIO	PE9	93	GPIO
PE10	94	GPIO	PE11	95	GPIO
PE12	96	GPIO	PE13	97	GPIO
PE14	98	GPIO	PE15	99	GPIO
PA15	100	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.15 EFM32GG11B1xx in QFP64 Device Pinout

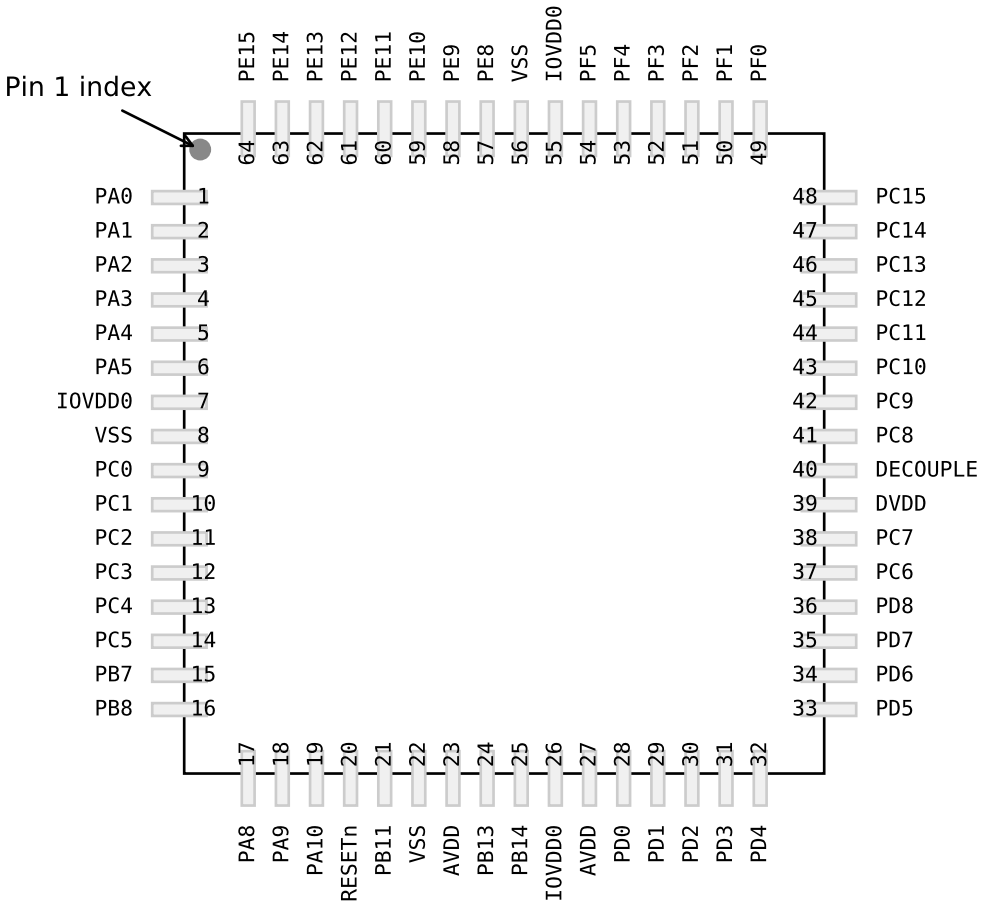

Figure 5.15. EFM32GG11B1xx in QFP64 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.15. EFM32GG11B1xx in QFP64 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
IOVDD0	7 26 55	Digital IO power supply 0.	VSS	8 22 56	Ground
PC0	9	GPIO (5V)	PC1	10	GPIO (5V)
PC2	11	GPIO (5V)	PC3	12	GPIO (5V)

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_CS1	0: PD10 1: PA11 2: PC1 3: PB1	4: PE9	External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	0: PD11 1: PA12 2: PC2 3: PB2	4: PE10	External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	0: PD12 1: PB15 2: PC3 3: PB3	4: PE11	External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	0: PA7 1: PF6 2: PB12 3: PA0		External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	0: PA8 1: PF7 2: PH0 3: PA1		External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	0: PA9 1: PD9 2: PH1 3: PA2		External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	0: PA11 1: PD11 2: PH3 3: PA4		External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	0: PC3 1: PD15 2: PB9 3: PC4	4: PC15 5: PF12	External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	0: PC5 1: PD14 2: PA13 3: PC2	4: PC14 5: PF11	External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	0: PF5 1: PA14 2: PA12 3: PC0	4: PF9 5: PF5	External Bus Interface (EBI) Read Enable output.
EBI_VSNC	0: PA10 1: PD10 2: PH2 3: PA3		External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	0: PF4 1: PA13 2: PC5 3: PB6	4: PF8 5: PF4	External Bus Interface (EBI) Write Enable output.
ETH_MDC	0: PB4 1: PD14 2: PC1 3: PA6		Ethernet Management Data Clock.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_MIITXD2	0: PA2 1: PG2		Ethernet MII Transmit Data Bit 2.
ETH_MIITXD3	0: PA1 1: PG1		Ethernet MII Transmit Data Bit 3.
ETH_MIITXEN	0: PA5 1: PG5		Ethernet MII Transmit Enable.
ETH_MIITXER	0: PA6 1: PG6		Ethernet MII Transmit Error.
ETH_RMIICRSDV	0: PA4 1: PD11		Ethernet RMII Carrier Sense / Data Valid.
ETH_RMIIREFCLK	0: PA3 1: PD10		Ethernet RMII Reference Clock.
ETH_RMIIRXD0	0: PA2 1: PD9		Ethernet RMII Receive Data Bit 0.
ETH_RMIIRXD1	0: PA1 1: PF9		Ethernet RMII Receive Data Bit 1.
ETH_RMIIRXER	0: PA5 1: PD12		Ethernet RMII Receive Error.
ETH_RMIITXD0	0: PE15 1: PF7		Ethernet RMII Transmit Data Bit 0.
ETH_RMIITXD1	0: PE14 1: PF6		Ethernet RMII Transmit Data Bit 1.
ETH_RMIITXEN	0: PA0 1: PF8		Ethernet RMII Transmit Enable.
ETH_TSUEXTCLK	0: PB5 1: PD15 2: PC2 3: PF8		Ethernet IEEE1588 External Reference Clock.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PF6		LCD segment line 24.
LCD_SEG25	0: PF7		LCD segment line 25.
LCD_SEG26	0: PF8		LCD segment line 26.
LCD_SEG27	0: PF9		LCD segment line 27.
LCD_SEG28	0: PD9		LCD segment line 28.
LCD_SEG29	0: PD10		LCD segment line 29.
LCD_SEG30	0: PD11		LCD segment line 30.
LCD_SEG31	0: PD12		LCD segment line 31.
LCD_SEG32	0: PB0		LCD segment line 32.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PCNT0_S0IN	0: PC13 1: PE0 2: PC0 3: PD6	4: PA0 5: PB0 6: PB5 7: PB12	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PC14 1: PE1 2: PC1 3: PD7	4: PA1 5: PB1 6: PB6 7: PB11	Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	0: PA5 1: PB3 2: PD15 3: PC4	4: PA7 5: PA12 6: PB11 7: PG14	Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	0: PA6 1: PB4 2: PB0 3: PC5	4: PA8 5: PA13 6: PB12 7: PG15	Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	0: PD0 1: PE8 2: PB13 3: PF10	4: PC12 5: PI2 6: PI0 7: PH14	Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	0: PD1 1: PE9 2: PB14 3: PF11	4: PC13 5: PI1 6: PH15 7: PH13	Pulse Counter PCNT2 input number 1.
PRS_CH0	0: PA0 1: PF3 2: PC14 3: PF2		Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PA1 1: PF4 2: PC15 3: PE12		Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PC0 1: PF5 2: PE10 3: PE13		Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PC1 1: PE8 2: PE11 3: PA0		Peripheral Reflex System PRS, channel 3.
PRS_CH4	0: PC8 1: PB0 2: PF1		Peripheral Reflex System PRS, channel 4.
PRS_CH5	0: PC9 1: PB1 2: PD6		Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA6 1: PB14 2: PE6		Peripheral Reflex System PRS, channel 6.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US1_CTS	0: PB9 1: PD4 2: PF3 3: PC6	4: PC12 5: PB13 6: PH2	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PB10 1: PD5 2: PF4 3: PC7	4: PC13 5: PB14 6: PH3	USART1 Request To Send hardware flow control output.
US1_RX	0: PC1 1: PD1 2: PD6 3: PF7	4: PC2 5: PA0 6: PA2	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PC0 1: PD0 2: PD7 3: PF6	4: PC1 5: PF2 6: PA14	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	0: PC4 1: PB5 2: PA9 3: PA15	4: PF8 5: PF2	USART2 clock input / output.
US2_CS	0: PC5 1: PB6 2: PA10 3: PB11	4: PF9 5: PF5	USART2 chip select input / output.
US2_CTS	0: PC1 1: PB12 2: PA11 3: PB10	4: PC12 5: PD6	USART2 Clear To Send hardware flow control input.
US2_RTS	0: PC0 1: PB15 2: PA12 3: PC14	4: PC13 5: PD8	USART2 Request To Send hardware flow control output.
US2_RX	0: PC3 1: PB4 2: PA8 3: PA14	4: PF7 5: PF1	USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	0: PC2 1: PB3 2: PA7 3: PA13	4: PF6 5: PF0	USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
US3_CLK	0: PA2 1: PD7 2: PD4 3: PG8	4: PG2 5: PI14	USART3 clock input / output.
US3_CS	0: PA3 1: PE4 2: PC14 3: PC0	4: PG3 5: PI15	USART3 chip select input / output.
US3_CTS	0: PA4 1: PE5 2: PD6 3: PG10	4: PG4 5: PG9	USART3 Clear To Send hardware flow control input.

Table 7.1. BGA152 Package Dimensions

Dimension	Min	Typ	Max
A	0.78	0.84	0.90
A1	0.13	0.18	0.23
A3	0.16	0.20	0.24
A2		0.45 REF	
D		8.00 BSC	
e		0.50 BSC	
E		8.00 BSC	
D1		6.50 BSC	
E1		6.50 BSC	
b	0.20	0.25	0.30
aaa		0.10	
bbb		0.10	
ddd		0.08	
eee		0.15	
fff		0.05	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. TQFP100 Package Specifications

10.1 TQFP100 Package Dimensions

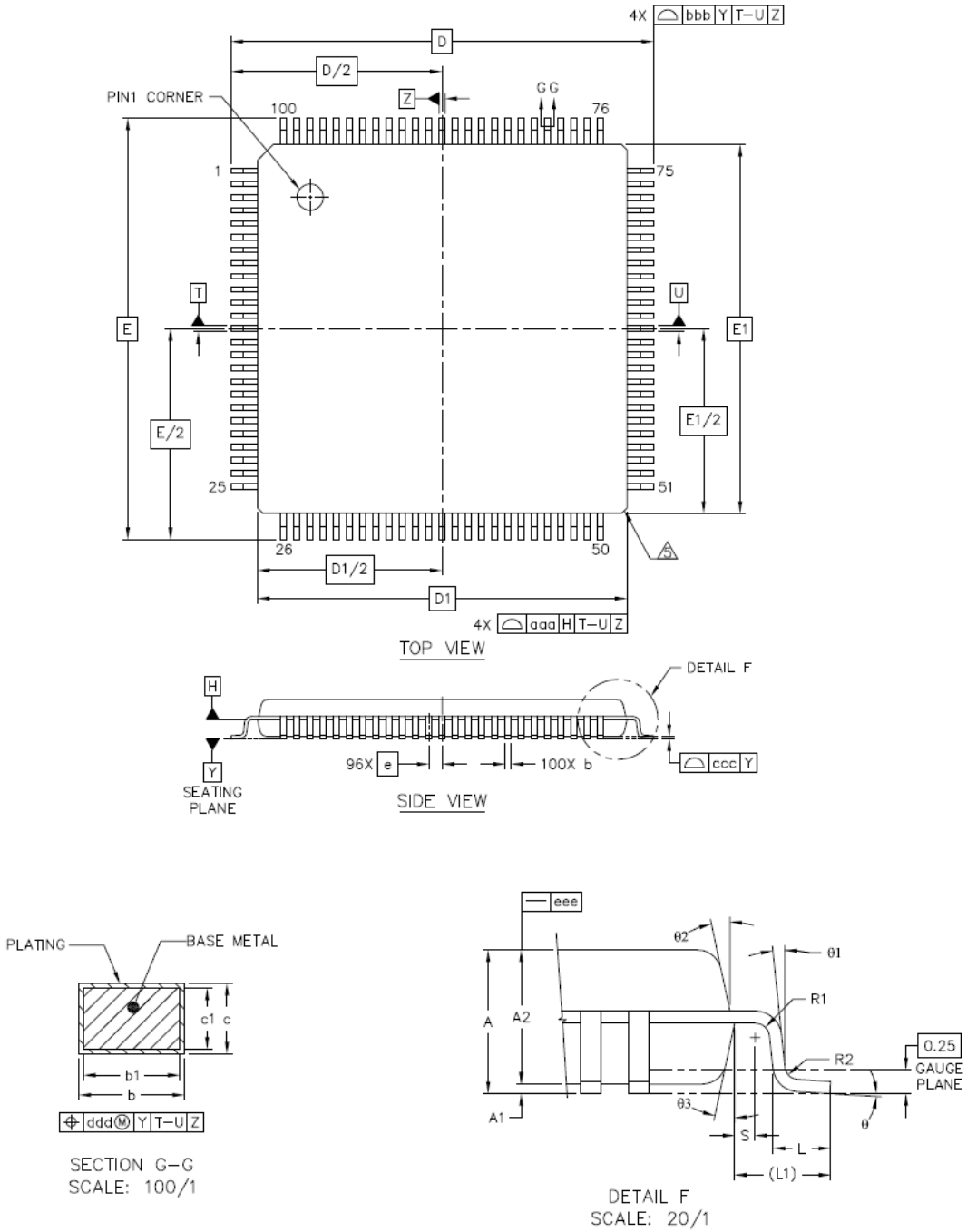

Figure 10.1. TQFP100 Package Drawing