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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	1MB (1M × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32gg11b840f1024im64-br

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Giant Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.11 Memory Map

The EFM32GG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

	8xfq1qqqe]		
CM4 Peripherals	8xe88fffff			
	8×85555555			
QSPIO	0xcfffffff			
	8886666666			
EBI Region 3	8×855555555			
EBI Region 2	8×8844444	i \		
EBI Region 1	8×87555555			0xe0100000
EBI Region 0	8×83555555		CM4 ROM Table	0xe00ff000
5	8×7fffffff			0xe0042000
Bit Set	0x460f03ff		EIM	0xe0041000
(Peripherals / CRYPTO0)	0×46000000		TPIO	0xe0040000
	8×455f5455) `, F	System Control Space	0xe000f000
Bit Clear (Paripherals / CRXPTOD)	0x440f03ff		b)stern control opace	0xe000e000
(Feripherals / CKTF100)	0x44000000 0x43ffffff		FPB	0xe0003000
Pit Pand	0x43e40000 0x43e3ffff		DWT	0xe0002000
(Peripherals / CRYPTO0 / SDIO)	0×42000000		ITM	0xe0001000
	8×41146666	1 -		0xe0000000
USB	8×48136666	1 _		
	8×488‡£555	1 /-	DAMO	0x10080000
SDIO	8×488f1666	1 /	(code space)	0100.40000
	8×488f8455		RAM1	0X10040000
CRYPT00	8×488‡8355	1 / -	(code space)	0x10020000
Peripherals 1	8×48825555		(code space)	0
Peripherals 0	8×48834444			0x10000000 0x0fe09000
	8×36666666	1 / F	Chip config	0x0fe08000
SRAM (bit-band)	8×355555555		Lock bits	0x0fe05000
	8×21ffffff			0x0fe04000
RAM2 (data space)	8×28871111		User Data	0x0fe00000
RAM1 (data space)	8×2883ffff		QSPI0	0x0c000000
BAMO (data space)	0x20020000 0x2001ffff	1/		0x04000000 0x00200000
(data space)	0x1ffffff	ł –		0.00200000
Code			F l ash (2048 KB)	
	0×000000000			0×00000000
				- 0.000000000

Figure 3.2. EFM32GG11 Memory Map — Core Peripherals and Code Space

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Storage temperature range	T _{STG}		-50	—	150	°C
Voltage on supply pins other than VREGI and VBUS	V _{DDMAX}		-0.3	_	3.8	V
Voltage ramp rate on any supply pin	V _{DDRAMPMAX}		_	—	1	V / µs
DC voltage on any GPIO pin	V _{DIGPIN}	5V tolerant GPIO pins ^{1 2 3}	-0.3	_	Min of 5.25 and IOVDD +2	V
		LCD pins ³	-0.3	_	Min of 3.8 and IOVDD +2	V
		Standard GPIO pins	-0.3	_	IOVDD+0.3	V
Total current into VDD power lines	I _{VDDMAX}	Source			200	mA
Total current into VSS ground lines	IVSSMAX	Sink			200	mA
Current per I/O pin	I _{IOMAX}	Sink	_	_	50	mA
		Source	_	_	50	mA
Current for all I/O pins	I _{IOALLMAX}	Sink	_	_	200	mA
		Source	_	_	200	mA
Junction temperature	TJ	-G grade devices	-40	_	105	°C
		-I grade devices	-40	_	125	°C
Voltage on regulator supply pins VREGI and VBUS	V _{VREGI}		-0.3		5.5	V

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

 Valid for IOVDD in valid operating range or when IOVDD is undriven (high-Z). If IOVDD is connected to a low-impedance source below the valid operating range (e.g. IOVDD shorted to VSS), the pin voltage maximum is IOVDD + 0.3 V, to avoid exceeding the maximum IO current specifications.

3. To operate above the IOVDD supply rail, over-voltage tolerance must be enabled according to the GPIO_Px_OVTDIS register. Pins with over-voltage tolerance disabled have the same limits as Standard GPIO.

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Output fall time, From 70%	t _{IOOF}	C _L = 50 pF,	_	1.8	_	ns
10 30% 01 V _{IO}		DRIVESTRENGTH ¹ = STRONG,				
		SLEWRATE ¹ = 0x6				
		C _L = 50 pF,	—	4.5	_	ns
		DRIVESTRENGTH ¹ = WEAK,				
		SLEWRATE ¹ = 0x6				
Output rise time, From 30%	t _{IOOR}	C _L = 50 pF,	_	2.2		ns
to 70% of V _{IO}		DRIVESTRENGTH ¹ = STRONG,				
		SLEWRATE = 0x6 ¹				
		C _L = 50 pF,	_	7.4		ns
		DRIVESTRENGTH ¹ = WEAK,				
		SLEWRATE ¹ = 0x6				
Note:	1		1	1		
1. In GPIO_Pn_CTRL regis	ter.					

4.1.14 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.22. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Resolution	VRESOLUTION		6	—	12	Bits
Input voltage range ⁵	V _{ADCIN}	Single ended	—	—	V _{FS}	V
		Differential	-V _{FS} /2	_	V _{FS} /2	V
Input range of external refer- ence voltage, single ended and differential	VADCREFIN_P		1	_	V _{AVDD}	V
Power supply rejection ²	PSRR _{ADC}	At DC	—	80	_	dB
Analog input common mode rejection ratio	CMRR _{ADC}	At DC	_	80	_	dB
Current from all supplies, us- ing internal reference buffer.	I _{ADC_CONTI-} NOUS_LP	1 Msps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³	_	270	TBD	μA
MUPMODE ⁴ = KEEPADC- WARM		250 ksps / 4 MHz ADCCLK, BIA- SPROG = 6, GPBIASACC = 1 ³	—	125	_	μA
		62.5 ksps / 1 MHz ADCCLK, BIA- SPROG = 15, GPBIASACC = 1 ³	_	80	_	μA
Current from all supplies, us- ing internal reference buffer.	IADC_NORMAL_LP	35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³	_	45	_	μA
MUPMODE ⁴ = NORMAL		5 ksps / 16 MHz ADCCLK BIA- SPROG = 0, GPBIASACC = 1 ³	—	8	_	μA
Current from all supplies, us- ing internal reference buffer.	IADC_STAND- BY_LP	125 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³	_	105	_	μA
AWARMUPMODE ⁴ = KEEP- INSTANDBY or KEEPIN- SLOWACC		35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 1 ³	_	70	_	μA
Current from all supplies, us- ing internal reference buffer.	I _{ADC_CONTI-} NOUS_HP	1 Msps / 16 MHz ADCCLK, BIA-SPROG = 0, GPBIASACC = 0 3	_	325	_	μA
MUPMODE ⁴ = KEEPADC- WARM		250 ksps / 4 MHz ADCCLK, BIA-SPROG = 6, GPBIASACC = 0 3	_	175	_	μA
		62.5 ksps / 1 MHz ADCCLK, BIA- SPROG = 15, GPBIASACC = 0 ³	_	125	_	μA
Current from all supplies, us- ing internal reference buffer.	IADC_NORMAL_HP	35 ksps / 16 MHz ADCCLK, BIA-SPROG = 0, GPBIASACC = 0 3	—	85	_	μA
MUPMODE ⁴ = NORMAL		5 ksps / 16 MHz ADCCLK BIA- SPROG = 0, GPBIASACC = 0 3	—	16	_	μA
Current from all supplies, us- ing internal reference buffer.	I _{ADC_STAND-} BY_HP	125 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 3	—	160	_	μA
AWARMUPMODE ⁴ = KEEP- INSTANDBY or KEEPIN- SLOWACC		35 ksps / 16 MHz ADCCLK, BIA- SPROG = 0, GPBIASACC = 0 ³	—	125	_	μA
Current from HFPERCLK	IADC_CLK	HFPERCLK = 16 MHz	—	180	_	μA

4.1.21 Pulse Counter (PCNT)

Table 4.29. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Input frequency	F _{IN}	Asynchronous Single and Quad- rature Modes	—	_	20	MHz
		Sampled Modes with Debounce filter set to 0.	_	_	8	kHz

4.1.22 Analog Port (APORT)

Table 4.30. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Supply current ^{2 1}	I _{APORT}	Operation in EM0/EM1	—	7	—	μA
		Operation in EM2/EM3		915		nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.

2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

RMII Receive Timing

Timing is specified with 3.0 V \leq IOVDD \leq 3.8 V, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.45.	Ethernet	RMII	Receive	Timing
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Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
REF_CLK frequency	F _{REF_CLK}	Output slew rate set to 7	—	50	_	MHz
REF_CLK duty cycle	DC _{REF_CLK}		35	_	65	%
Setup time, RXD[1:0], CRS_DV, RX_ER valid to REF_CLK	t _{SU}		4	_	_	ns
Hold time, REF_CLK to RXD[1:0], CRS_DV, RX_ER change	t _{HD}		2	_	_	ns



Figure 4.12. Ethernet RMII Receive Timing



Figure 4.25. EM1 Sleep Mode Typical Supply Current vs. Temperature

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.



Figure 4.30. DC-DC Converter Transition Waveforms

PB2M3GPIOPB3M3GPIOPC6M1GPIOVRECVSM1value regulator VSSVREGWM4DCO regulator switching nodePB4N1GPIOPB5M2GPIOPD4M3GPIOPD5M1GPIOPD4M2GPIOPC0P1GPIO(SV)PA6P2GPIO(SV)PH1P5GPIO(SV)PH2P4GPIOPH2P1GPIO(SV)PH1P12GPIOPH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P12GPIO(SV)PH3P1GPIO(SV)PH1P14GPIO(SV)PH3P1GPIO(SV)PH1P14GPIO(SV)PH3P3GPIO(SV)PH1P14GPIO(SV)PH3P3GPIO(SV)PH1P14GPIO(SV)PH4P3GPIO(SV)PH2R2GPIO(SV)PH3P3GPIO(SV)PH3R4GPIO(SV)PH4S1GPIO(SV)GPICR2GPIO(SV)PS0R3GPIO(SV)GPISR4GPIO(SV)PS0R4GPIO(SV)GPISR4 <td< th=""><th>Pin Name</th><th>Pin(s)</th><th>Description</th><th>Pin Name</th><th>Pin(s)</th><th>Description</th></td<>	Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC6M14GPI0VREGVSM15Voltage regulator VSSVREGSWM16DCDC regulator switching nodePP84N1GPI0PB65N2GPI0PP80N3GPI0PD55N14GPI0PP10PP2GPI0PC0P1GPI0PP10PP2GPI0PC1P3GPI0PP10PP2GPI0PC2P3GPI0GPI0PP3GPI0PC1P4GPI0GPI0PP3GPI0PC2P3GPI0GPI0PP41GPI0PC3P3GPI0GPI0PP3GPI0PH3P16GPI0PP30PP3GPI0PH3P17GPI0GPI0PP40GPI0PH3P13GPI0PP10P11GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30P18GPI0PH3P13GPI0PP30R2GPI0PH5R13GPI0PP30R4GPI0PH5R13GPI0PP40R16GPI0PH4P13GPI0PP40P14GPI0PH4R19GPI0GPI0P14GPI0PH4R19GPI0GPI0P14GPI0PH4R19GPI0GPI0P14GPI0PH4R19GPI0GPI0P14	PB2	M2	GPIO	PB3	M3	GPIO
VREGSWM14DCD regulator switching nodePB4N1CPI0PB5N2GPI0PPB6N3GPI0PD5N14GPI0PD4N15GPI0PC0P3GPI0 (5V)PA1PA2GPI0PA1P5GPI0PA3P6GPI0PA1P5GPI0PA3P6GPI0P14P7GPI0 (5V)PH12P8GPI0P14P1GPI0 (5V)PH13P10GPI0 (5V)P14P1GPI0 (5V)PH14P12GPI0 (5V)P14P13GPI0 (5V)PH10P12GPI0 (5V)P143P13GPI0 (5V)PH10P14GPI0 (5V)P143P14GPI0 (5V)PH10P14GPI0 (5V)P143P15GPI0 (5V)PD0P14GPI0 (5V)P15GPI0 (5V)PD0P14GPI0 (5V)P16R1GPI0 (5V)GPI0 (5V)Restingut active low. To apply an extractive low. To apply an extractina	PC6	M14	GPIO	VREGVSS	M15 N16	Voltage regulator VSS
PB5N2GPIOPB6N3GPIOPD5N14GPIOPD4N15GPIOPC0P1GPIO (5V)PC1P2GPIO (5V)PC1P3GPIO (5V)PA8P4GPIO (5V)PB9P7GPIO (5V)PB12P8GPIO (5V)PH8P1GPIO (5V)PH10P12GPIO (5V)PH3P13GPIO (5V)PD0PH10P12GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PH3SP15GPIO (5V)PD0P14GPIO (5V)PD3P15GPIO (5V)PD0P14GPIO (5V)PD4N14GPIO (5V)PD1PA9R4PD5R3GPIO (5V)FPA9R4GPIO (5V)PD5R3GPIO (5V)PH4R4GPIO (5V)PH4R4GPIO (5V)PH4R14GPIO (5V)PH4R14GPIO (5V)PH10R14GPIO (5V)PH4R14GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH12R14GPIO (5V)PH4R14GPIO (5V)PH4R14GPIO (5V)PH4<	VREGSW	M16	DCDC regulator switching node	PB4	N1	GPIO
PD5N14GP0PD4N15GP10PC0P1GP10 (5V)PC1P2GP10 (5V)PC2P3GP10 (5V)PA8P4GP10 (5V)PB9P7GP10 (5V)PB12P8GP10 (5V)PH2P9GP10 (5V)PH11P12GP10 (5V)PH3P11GP10 (5V)PH11P12GP10 (5V)PH3P13GP10 (5V)PD0P14GP10 (5V)PH3P13GP10 (5V)PD0P14GP10 (5V)PH3P15GP10 (5V)PD0P14GP10 (5V)PB7R1GP10 (5V)PD0P14GP10 (5V)PB7R3GP10 - Controlled to failed to main extension may be of the single active tow. To apply an extend extension exten	PB5	N2	GPIO	PB6	N3	GPIO
PC0P1GPI0 (5V)PC1P2GPI0 (5V)PC2P3GPI0 (5V)PA8P4GPI0PA11P5GPI0 (5V)PA13P6GPI0 (5V)PB9P7GPI0 (5V)PB12P8GPI0 (5V)PH2P9GPI0 (5V)PH15P10GPI0 (5V)PH3P11GPI0 (5V)PH11P12GPI0 (5V)PH3P13GPI0 (5V)PH10P14GPI0 (5V)PH3P13GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0 (5V)PD0P14GPI0 (5V)PD3R1GPI0 (5V)PD3R2GPI0 (5V)PC5R3GPI0 (5V)PA9R4GPI0 (5V)PC5R3GPI0 (5V)PA9R4GPI0 (5V)BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to M20D.R68GPI0 (5V)PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH10R14GPI0 (5V)PH4R13GPI0 (5V)PH10R14GPI0 (5V)PH4R13GPI0 (5V)PH10R14GPI0 (5V)PH4R15GPI0 (5V)PA14T6GPI0PH4R13GPI0 (5V)PA14T6GPI0PH4R13GPI0 (5V)PA14T6GPI0 (5V)PH4T3GPI0 (5V) <td>PD5</td> <td>N14</td> <td>GPIO</td> <td>PD4</td> <td>N15</td> <td>GPIO</td>	PD5	N14	GPIO	PD4	N15	GPIO
PC2 P3 GPIO (5V) PA8 P4 GPIO PA11 P5 GPIO PA13 P6 GPIO (5V) PB9 P7 GPIO (5V) PB12 P8 GPIO PH2 P9 GPIO (5V) PH5 P10 GPIO PH3 P11 GPIO (5V) PH11 P12 GPIO (5V) PH3 P13 GPIO (5V) PD0 P14 GPIO (5V) PH3 P13 GPIO (5V) PD0 P14 GPIO (5V) PD3 P15 GPIO PD3 P15 GPIO (5V) PD3 P15 GPIO PC3 R2 GPIO (5V) PD5 R3 GPIO PA9 R4 GPIO BODEN R5 Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. RESETn R6 GPIO (5V) PB10 R7 GPIO (5V) PH0 R8 GPIO (5V) PH3 R9 GPIO (5V) PH1 R1 GPIO (PC0	P1	GPIO (5V)	PC1	P2	GPIO (5V)
PA11 P5 GPIO PA13 P6 GPIO (5V) PB9 P7 GPIO (5V) PB12 P8 GPIO PH2 P9 GPIO (5V) PH5 P10 GPIO PH8 P11 GPIO (5V) PH11 P12 GPIO (5V) PH3 P13 GPIO (5V) PD0 P14 GPIO (5V) PD3 P15 GPIO (5V) PD0 P14 GPIO (5V) PD3 P15 GPIO PD3 P15 GPIO PD4 PB7 R1 GPIO PC3 R2 GPIO (5V) PC5 R3 GPIO PA9 R4 GPIO BODEN R5 Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD. RESETn R6 Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and left the internal pul-upensure that reset is released. PB10 R7 GPIO (5V) PH0 R8 GPIO (5V) PH3 R9 GPIO (5V) P	PC2	P3	GPIO (5V)	PA8	P4	GPIO
PB9P7GPIO (5V)PB12P8GPIOPH2P9GPIO (5V)PH5P10GPIOPH8P11GPIO (5V)PD11P12GPIO (5V)PH3P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD2P23R2GPIO (5V)PB7R1GPIOPA9R4GPIOPC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin wyb be left disconnected or tied to AVDD.RESETNR6Reset input, active low. To apply an ex- terral reset source to this pin, it is re- arrest only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIOPH4R13GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PD7R16GPIOPH3T1GPIOPA10T4GPIOPH4T3GPIO (5V)PA14T6GPIOPH4T3GPIO (5V)PH11T8GPIO (5V)PH4T9GPIO (5V)PH1T10GPIOPH4T9GPIO (5V)PH7T10GPIOPH4T9GPIO (5V)PH3T12GPIOPH4T13GPIO (5V)PH3T12GPIOPH4T14GPIO (5V)PH3T14Anal	PA11	P5	GPIO	PA13	P6	GPIO (5V)
PH2P9GPI0 (5V)PH5P10GPI0PH8P11GPI0 (5V)PH11P12GPI0 (5V)PH3P13GPI0 (5V)PD0P14GPI0 (5V)PD3P15GPI0PD0P14GPI0 (5V)PB7R1GPI0PC3R2GPI0 (5V)PC5R3GPI0PA9R4GPI0BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin out during reset, and let the internal pull-up ensure that reset is released.PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH6R10GPI0PH4R13GPI0 (5V)PH12R12GPI0 (5V)PH4R13GPI0 (5V)PH15R14GPI0 (5V)PH4R13GPI0 (5V)PD7R16GPI0PH3T1GPI0 (5V)PD7R16GPI0PH4T3GPI0 (5V)PA14T6GPI0PH4T3GPI0 (5V)PA14T6GPI0PH4T7GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T9GPI0 (5V)PA14T6GPI0 (5V)PH4T1GPI0 (5V)PB13T12GPI0PH4<	PB9	P7	GPIO (5V)	PB12	P8	GPIO
PH8P11GPIO (5V)PH11P12GPIO (5V)PH13P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD8P16GPIOPB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENRsBrown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETNR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and left the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIOPH4R13GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPA3T3GPIO (5V)PD7R16GPIOPH4T3GPIO (5V)PD7R16GPIOPH4T3GPIO (5V)PA14T6GPIOPH4T9GPIO (5V)PH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIOPH7 <t< td=""><td>PH2</td><td>P9</td><td>GPIO (5V)</td><td>PH5</td><td>P10</td><td>GPIO</td></t<>	PH2	P9	GPIO (5V)	PH5	P10	GPIO
PH13P13GPIO (5V)PD0P14GPIO (5V)PD3P15GPIOPD8P16GPIOPB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH3R9GPIO (5V)PH15R14GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPA7T3GPIO (5V)PA14T6GPIOPA12T5GPIO (5V)PA14T6GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH3T12GPIOPH4T9GPIO (5V)PH3T12GPIOPH4T13GPIOAVDDT14Analog power supply.PH4T15GPIO <td>PH8</td> <td>P11</td> <td>GPIO (5V)</td> <td>PH11</td> <td>P12</td> <td>GPIO (5V)</td>	PH8	P11	GPIO (5V)	PH11	P12	GPIO (5V)
PD3P15GPI0PD8P16GPI0PB7R1GPI0PC3R2GPI0 (5V)PC5R3GPI0PA9R4GPI0BC5R3GPI0PA9R4GPI0BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnReset input, active low. To apply an ex- ternal reset source to this pin, it is re- quied to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPI0 (5V)PH0R8GPI0 (5V)PH3R9GPI0 (5V)PH6R10GPI0PH3R9GPI0 (5V)PH6R10GPI0 (5V)PH3R1GPI0 (5V)PH12R12GPI0 (5V)PH4R13GPI0 (5V)PH15R14GPI0 (5V)PD2R15GPI0 (5V)PD7R16GPI0PB8T1GPI0PA10T4GPI0PA12T5GPI0 (5V)PA14T6GPI0PA14T9GPI0 (5V)PH1T8GPI0 (5V)PH4T9GPI0 (5V)PB13T12GPI0PH4T13GPI0 (5V)PB13T12GPI0PB14T13GPI0AVDDT14Analog power supply.PB14T15GPI0PD6T16GPI0	PH13	P13	GPIO (5V)	PD0	P14	GPIO (5V)
PB7R1GPIOPC3R2GPIO (5V)PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnReset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R13GPIO (5V)PH15R14GPIO (5V)PH14R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPA12T5GPIO (5V)PA14T6GPIOPH14T9GPIO (5V)PH1T10GPIO (5V)PH14T1GPIO (5V)PA14T6GPIOPH15T11GPIO (5V)PA14T6GPIOPH10T11GPIO (5V)PH1T10GPIO (5V)PH14T9GPIO (5V)PH3T12GPIOPH4T9GPIO (5V)PH3T12GPIOPH10T11GPIO (5V)PH3T12GPIOPH10T11GPIO (5V)PH3T14 </td <td>PD3</td> <td>P15</td> <td>GPIO</td> <td>PD8</td> <td>P16</td> <td>GPIO</td>	PD3	P15	GPIO	PD8	P16	GPIO
PC5R3GPIOPA9R4GPIOBODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.PB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH6R10GPIO (5V)PH4R11GPIO (5V)PH6R10GPIO (5V)PH4R13GPIO (5V)PH12R12GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PD7R16GPIOPA7T3GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PH3T12GPIOPH4T13GPIO (5V)PH6T14Analog power supply.PH10T15GPIOPD6T16GPIO	PB7	R1	GPIO	PC3	R2	GPIO (5V)
BODENR5Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.RESETnR6Reset input, active low. To apply an ex- termal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensurePB10R7GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH0R8GPIO (5V)PH3R9GPIO (5V)PH12R12GPIO (5V)PH3R1GPIO (5V)PH12R12GPIO (5V)PH4R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIO (5V)PD7R16GPIOPA12T5GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH4T9GPIO (5V)PB13T12GPIOPH10T11GPIO (5V)PB13T12GPIOPB14T13GPIO (5V)PD6T16GPIOPD1T15GPIOPD6T16GPIO	PC5	R3	GPIO	PA9	R4	GPIO
PB10 R7 GPIO (5V) PH0 R8 GPIO (5V) PH3 R9 GPIO (5V) PH6 R10 GPIO PH9 R11 GPIO (5V) PH12 R12 GPIO (5V) PH14 R13 GPIO (5V) PH12 R14 GPIO (5V) PD14 R13 GPIO (5V) PH12 R14 GPIO (5V) PD2 R15 GPIO (5V) PD7 R16 GPIO PD2 R15 GPIO (5V) PD7 R16 GPIO PB8 T1 GPIO (5V) PD7 R16 GPIO PB4 T3 GPIO (5V) PC4 T2 GPIO PA12 T5 GPIO (5V) PA14 T6 GPIO PB11 T7 GPIO (5V) PH1 T8 GPIO (5V) PH4 T9 GPIO (5V) PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14	BODEN	R5	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	RESETn	R6	Reset input, active low. To apply an ex- ternal reset source to this pin, it is re- quired to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PH3R9GPIO (5V)PH6R10GPIOPH9R11GPIO (5V)PH12R12GPIO (5V)PH14R13GPIO (5V)PH15R14GPIO (5V)PD2R15GPIO (5V)PD7R16GPIO (5V)PB8T1GPIO (5V)PC4T2GPIOPA7T3GPIO (5V)PA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PB10	R7	GPIO (5V)	PH0	R8	GPIO (5V)
PH9 R11 GPIO (5V) PH12 R12 GPIO (5V) PH14 R13 GPIO (5V) PH15 R14 GPIO (5V) PD2 R15 GPIO (5V) PD7 R16 GPIO PB8 T1 GPIO (5V) PC4 T2 GPIO PA7 T3 GPIO PA10 T4 GPIO PA12 T5 GPIO (5V) PA10 T4 GPIO PA12 T5 GPIO (5V) PA14 T6 GPIO PB11 T7 GPIO PH1 T8 GPIO (5V) PH10 T1 GPIO PH1 T8 GPIO (5V) PH4 T9 GPIO PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH3	R9	GPIO (5V)	PH6	R10	GPIO
PH14 R13 GPIO (5V) PH15 R14 GPIO (5V) PD2 R15 GPIO (5V) PD7 R16 GPIO PB8 T1 GPIO (5V) PC4 T2 GPIO PA7 T3 GPIO (5V) PA10 T4 GPIO PA12 T5 GPIO (5V) PA14 T6 GPIO PB11 T7 GPIO (5V) PA14 T6 GPIO (5V) PH44 T9 GPIO (5V) PH1 T8 GPIO (5V) PH4 T9 GPIO (5V) PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO (5V) PB13 T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH9	R11	GPIO (5V)	PH12	R12	GPIO (5V)
PD2R15GPIO (5V)PD7R16GPIOPB8T1GPIOPC4T2GPIOPA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIO (5V)PH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PH14	R13	GPIO (5V)	PH15	R14	GPIO (5V)
PB8T1GPIOPC4T2GPIOPA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PD2	R15	GPIO (5V)	PD7	R16	GPIO
PA7T3GPIOPA10T4GPIOPA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PB8	T1	GPIO	PC4	T2	GPIO
PA12T5GPIO (5V)PA14T6GPIOPB11T7GPIOPH1T8GPIO (5V)PH4T9GPIOPH7T10GPIO (5V)PH10T11GPIO (5V)PB13T12GPIOPB14T13GPIOAVDDT14Analog power supply.PD1T15GPIOPD6T16GPIO	PA7	Т3	GPIO	PA10	T4	GPIO
PB11 T7 GPIO PH1 T8 GPIO (5V) PH4 T9 GPIO PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PA12	T5	GPIO (5V)	PA14	Т6	GPIO
PH4 T9 GPIO PH7 T10 GPIO (5V) PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PB11	T7	GPIO	PH1	Т8	GPIO (5V)
PH10 T11 GPIO (5V) PB13 T12 GPIO PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH4	Т9	GPIO	PH7	T10	GPIO (5V)
PB14 T13 GPIO AVDD T14 Analog power supply. PD1 T15 GPIO PD6 T16 GPIO	PH10	T11	GPIO (5V)	PB13	T12	GPIO
PD1 T15 GPIO PD6 T16 GPIO	PB14	T13	GPIO	AVDD	T14	Analog power supply.
	PD1	T15	GPIO	PD6	T16	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.



Figure 5.5. EFM32GG11B4xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.5. EFM32GG11B4xx in BGA120 Device Pino	ut
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Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF4	A9	GPIO	PF2	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regu- lator output. Power for USB PHY in USB-enabled OPNs



Figure 5.8. EFM32GG11B8xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A10	0: PE3 1: PD6 2: PC10 3: PB10		External Bus Interface (EBI) address output pin 10.
EBI_A11	0: PE4 1: PD7 2: PI6 3: PB11		External Bus Interface (EBI) address output pin 11.
EBI_A12	0: PE5 1: PD8 2: PI7 3: PB12		External Bus Interface (EBI) address output pin 12.
EBI_A13	0: PE6 1: PC7 2: PI8 3: PD0		External Bus Interface (EBI) address output pin 13.
EBI_A14	0: PE7 1: PE2 2: PI9 3: PD1		External Bus Interface (EBI) address output pin 14.
EBI_A15	0: PC8 1: PE3 2: PI10 3: PD2		External Bus Interface (EBI) address output pin 15.
EBI_A16	0: PB0 1: PE4 2: PH4 3: PD3		External Bus Interface (EBI) address output pin 16.
EBI_A17	0: PB1 1: PE5 2: PH5 3: PD4		External Bus Interface (EBI) address output pin 17.
EBI_A18	0: PB2 1: PE6 2: PH6 3: PD5		External Bus Interface (EBI) address output pin 18.
EBI_A19	0: PB3 1: PE7 2: PH7 3: PD6		External Bus Interface (EBI) address output pin 19.
EBI_A20	0: PB4 1: PC8 2: PH8 3: PD7		External Bus Interface (EBI) address output pin 20.
EBI_A21	0: PB5 1: PC9 2: PH9 3: PC7		External Bus Interface (EBI) address output pin 21.
EBI_A22	0: PB6 1: PC10 2: PH10 3: PE4		External Bus Interface (EBI) address output pin 22.

Alternate	LOCA	ATION								
Functionality	0 - 3	4 - 7	Description							
LES_CH11	0: PC11		LESENSE channel 11.							
LES_CH12	0: PC12		LESENSE channel 12.							
LES_CH13	0: PC13		LESENSE channel 13.							
LES_CH14	0: PC14		LESENSE channel 14.							
LES_CH15	0: PC15		LESENSE channel 15.							
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8 7: PB9	Low Energy Timer LETIM0, output channel 0.							
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9 7: PB10	Low Energy Timer LETIM0, output channel 1.							
LETIM1_OUT0	0: PA7 1: PA11 2: PA12 3: PC2	4: PB5 5: PB2 6: PG0 7: PG2	Low Energy Timer LETIM1, output channel 0.							
LETIM1_OUT1	0: PA6 1: PA13 2: PA14 3: PC3	4: PB6 5: PB1 6: PG1 7: PG3	Low Energy Timer LETIM1, output channel 1.							
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.							
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.							
LEU1_RX	0: PC7 1: PA6 2: PD3 3: PB1	4: PB5 5: PH1	LEUART1 Receive input.							
LEU1_TX	0: PC6 1: PA5 2: PD2 3: PB0	4: PB4 5: PH0	LEUART1 Transmit output. Also used as receive input in half duplex communication.							

Alternate	LOCA	TION								
Functionality	0 - 3	4 - 7	Description							
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional ex- ternal clock input pin.							
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.							
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.							
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.							
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.							
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.							
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.							
OPA2_OUT	0: PD5		Operational Amplifier 2 output.							
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.							
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.							
OPA3_N	0: PC7		Operational Amplifier 3 external negative input.							
OPA3_OUT	0: PD1		Operational Amplifier 3 output.							
OPA3_P	0: PC6		Operational Amplifier 3 external positive input.							

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM2_CC1	0: PA9 1: PA13 2: PC9 3: PE12	4: PC0 5: PC3 6: PG9 7: PG6	Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	0: PA10 1: PA14 2: PC10 3: PE13	4: PC1 5: PC4 6: PG10 7: PG7	Timer 2 Capture Compare input / output channel 2.
TIM2_CDTI0	0: PB0 1: PD13 2: PE8 3: PG0		Timer 2 Complimentary Dead Time Insertion channel 0.
TIM2_CDTI1	0: PB1 1: PD14 2: PE14 3: PG1		Timer 2 Complimentary Dead Time Insertion channel 1.
TIM2_CDTI2	0: PB2 1: PD15 2: PE15 3: PG2		Timer 2 Complimentary Dead Time Insertion channel 2.
TIM3_CC0	0: PE14 1: PE0 2: PE3 3: PE5	4: PA0 5: PA3 6: PA6 7: PD15	Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	0: PE15 1: PE1 2: PE4 3: PE6	4: PA1 5: PA4 6: PD13 7: PB15	Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	0: PA15 1: PE2 2: PE5 3: PE7	4: PA2 5: PA5 6: PD14 7: PB0	Timer 3 Capture Compare input / output channel 2.
TIM4_CC0	0: PF3 1: PF13 2: PF5 3: PI8	4: PF6 5: PF9 6: PD11 7: PE9	Timer 4 Capture Compare input / output channel 0.
TIM4_CC1	0: PF4 1: PF14 2: PI6 3: PI9	4: PF7 5: PD9 6: PD12 7: PE10	Timer 4 Capture Compare input / output channel 1.
TIM4_CC2	0: PF12 1: PF15 2: PI7 3: PI10	4: PF8 5: PD10 6: PE8 7: PE11	Timer 4 Capture Compare input / output channel 2.
TIM4_CDTI0	0: PD0		Timer 4 Complimentary Dead Time Insertion channel 0.
TIM4_CDTI1	0: PD1		Timer 4 Complimentary Dead Time Insertion channel 1.

Alternate	LOCATION									
Functionality	0 - 3	4 - 7	Description							
US3_RTS	0: PA5 1: PC1 2: PA14 3: PC15	4: PG5 5: PG11	USART3 Request To Send hardware flow control output.							
US3_RX	0: PA1 1: PE7 2: PB7 3: PG7	4: PG1 5: PI13	USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).							
US3_TX	0: PA0 1: PE6 2: PB3 3: PG6	4: PG0 5: PI12	USART3 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART3 Synchronous mode Master Output / Slave Input (MOSI).							
US4_CLK	0: PC4 1: PD11 2: PI2 3: PI8	4: PH6	USART4 clock input / output.							
US4_CS	0: PC5 1: PD12 2: PI3 3: PI9	4: PH7	USART4 chip select input / output.							
US4_CTS	0: PA7 1: PD13 2: PI4 3: PI10	4: PH8	USART4 Clear To Send hardware flow control input.							
US4_RTS	0: PA8 1: PD14 2: PI5 3: PI11	4: PH9	USART4 Request To Send hardware flow control output.							
US4_RX	0: PB8 1: PD10 2: PI1 3: PI7	4: PH5	USART4 Asynchronous Receive. USART4 Synchronous mode Master Input / Slave Output (MISO).							
US4_TX	0: PB7 1: PD9 2: PI0 3: PI6	4: PH4	USART4 Asynchronous Transmit. Also used as receive input in half duplex communica- tion. USART4 Synchronous mode Master Output / Slave Input (MOSI).							
US5_CLK	0: PB11 1: PD13 2: PF13 3: PH12		USART5 clock input / output.							
US5_CS	0: PB13 1: PD14 2: PF12 3: PH13		USART5 chip select input / output.							
US5_CTS	0: PB14 1: PD15 2: PF11 3: PH14		USART5 Clear To Send hardware flow control input.							
US5_RTS	0: PB12 1: PB15 2: PF10 3: PH15		USART5 Request To Send hardware flow control output.							

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	СНЗ	CH2	CH1	CH0
APORT0X	BUSADC1X																									2Hd	9Hd	PH5	PH4	EH4	PH2	PH1	ЬНО
APORT0Y	BUSADC1Y																									2Hd	9Hd	5HG	PH4	EH4	PH2	PH1	ЬНО
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		6A9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		6Yd		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		63d		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PFO		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.28. ADC1 Bus and Pin Mapping



Figure 9.3. BGA112 Package Marking

The package marking consists of:

- PPPPPPPPP The part number designation.
- TTTTTT A trace or manufacturing code. The first letter is the device revision.
- YY The last 2 digits of the assembly year.
- WW The 2-digit workweek when the device was assembled.

11. TQFP64 Package Specifications

11.1 TQFP64 Package Dimensions



Figure 11.1. TQFP64 Package Drawing