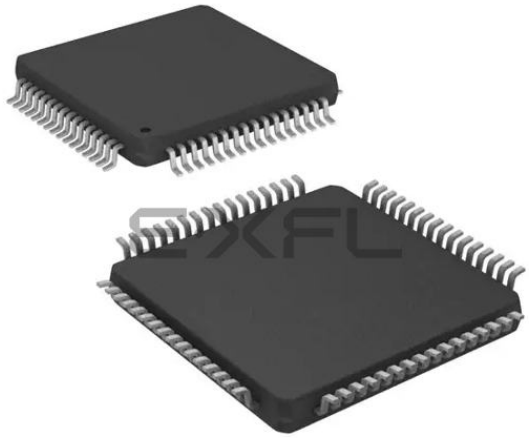

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Number of I/O	47
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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
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Data Converters	A/D 16x12b SAR; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
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Supplier Device Package	64-TQFP (10x10)
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4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range[6]	T_A	-G temperature grade	-40	25	85	°C
		-I temperature grade	-40	25	125	°C
AVDD supply voltage[2]	V_{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage[2] [1]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass, 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass, T ≤ 85 °C	—	—	200	mA
		DCDC in bypass, T > 85 °C	—	—	100	mA
DVDD operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage	V_{IOVDD}	All IOVDD pins[5]	1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor[3] [4]	$C_{DECOUPLE}$		0.75	1.0	2.75	µF
HFCORECLK frequency	f_{CORE}	VSCALE2, MODE = WS3	—	—	72	MHz
		VSCALE2, MODE = WS2	—	—	54	MHz
		VSCALE2, MODE = WS1	—	—	36	MHz
		VSCALE2, MODE = WS0	—	—	18	MHz
		VSCALE0, MODE = WS2	—	—	20	MHz
		VSCALE0, MODE = WS1	—	—	14	MHz
		VSCALE0, MODE = WS0	—	—	7	MHz
HFCLK frequency	f_{HFCLK}	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFSRCCLK frequency	$f_{HFSRCCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFBUSCLK frequency	$f_{HFBUSCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERCLK frequency	$f_{HFPERCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERBCLK frequency	$f_{HFPERBCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFPERCCLK frequency	$f_{HFPERCCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz

4.1.4 DC-DC Converter

Test conditions: L_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 µF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.8	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC accuracy	ACC_{DC}	Low Noise (LN) mode, 1.8 V target output	TBD	—	TBD	V
Regulation window[4]	WIN_{REG}	Low Power (LP) mode, LPCMPBIASEMxx[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 µA	TBD	—	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	TBD	—	TBD	V
Steady-state output ripple	V_R		—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	25	TBD	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

4.1.5 5V Regulator

V_{VREGI} = 5 V, V_{VREGO} = 3.3 V, C_{VREGI} = 10 µF, C_{VREGO} = 4.7 µF, unless otherwise specified.

Table 4.5. 5V Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VREGI or VBUS input voltage range	V_{VREGI}	Regulating output	2.7	—	5.5	V
		Bypass mode enabled	2.7	—	3.8	V
VREGO output voltage	V_{VREGO}	Regulating output, 3.3 V setting	3.1	3.3	3.5	V
		EM4S open-loop output, I_{OUT} < 100 µA	1.8	—	3.8	V
Voltage output step size	V_{VREGO_SS}		—	0.1	—	V
Resistance in Bypass Mode	R_{BYP}	Bypass mode enabled	—	1.2	TBD	Ω
Output current	I_{OUT}	EM0 or EM1, V_{VREGI} > V_{VREGO} + 0.6 V	—	—	200	mA
		EM0 or EM1, V_{VREGI} > V_{VREGO} + 0.3 V	—	—	100	mA
		EM2, EM3, or EM4H, V_{VREGI} > V_{VREGO} + 0.6 V	—	—	2	mA
		EM2, EM3, or EM4H, V_{VREGI} > V_{VREGO} + 0.3 V	—	—	0.5	mA
		EM4S	—	—	20	µA
Load regulation	LR_{VREGO}	EM0 or EM1	—	0.10	—	mV/mA
		EM2, EM3, or EM4H	—	2.5	—	mV/mA
DC power supply rejection	PSR_{DC}		—	40	—	dB
VREGI or VBUS bypass capacitance	C_{VREGI}		—	10	—	µF
VREGO bypass capacitance	C_{VREGO}		1	4.7	10	µF
Supply current consumption	I_{VREGI}	EM0 or EM1, No load	—	29	—	µA
		EM2, EM3, or EM4H, No load	—	270	—	nA
		EM4S, No load	—	70	—	nA
VREGI and VBUS detection high threshold	V_{DET_H}		TBD	1.18	—	V
VREGI and VBUS detection low threshold	V_{DET_L}		—	1.12	TBD	V
Current monitor transfer ratio	$IMON_{XF}$	Translation of current through VREGO path to voltage at ADC input	—	0.35	—	mA/mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode[3]	I_{ACTIVE_LPM}	32 MHz HFRCO, CPU running while loop from flash	—	82	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	83	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	88	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	257	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1]	$I_{ACTIVE\_CCM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	117	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1231	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode[3]	$I_{ACTIVE\_LPM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	72	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	219	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{EM1_DCM}	72 MHz HFRCO	—	42	—	µA/MHz
		50 MHz crystal	—	46	—	µA/MHz
		48 MHz HFRCO	—	46	—	µA/MHz
		32 MHz HFRCO	—	53	—	µA/MHz
		26 MHz HFRCO	—	57	—	µA/MHz
		16 MHz HFRCO	—	72	—	µA/MHz
		1 MHz HFRCO	—	663	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode[3]	I_{EM1_LPM}	32 MHz HFRCO	—	42	—	µA/MHz
		26 MHz HFRCO	—	43	—	µA/MHz
		16 MHz HFRCO	—	48	—	µA/MHz
		1 MHz HFRCO	—	219	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2]	$I_{EM1\_DCM\_VS}$	19 MHz HFRCO	—	60	—	µA/MHz
		1 MHz HFRCO	—	637	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode[3]	$I_{EM1\_LPM\_VS}$	19 MHz HFRCO	—	39	—	µA/MHz
		1 MHz HFRCO	—	190	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode[3]	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	2.8	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	3.1	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[5]	—	2.1	—	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.4	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency limits	f_{HFRCO_BAND}	FREQRANGE = 0, FINETUNINGEN = 0	1	—	10	MHz
		FREQRANGE = 3, FINETUNINGEN = 0	2	—	17	MHz
		FREQRANGE = 6, FINETUNINGEN = 0	4	—	30	MHz
		FREQRANGE = 7, FINETUNINGEN = 0	5	—	34	MHz
		FREQRANGE = 8, FINETUNINGEN = 0	7	—	42	MHz
		FREQRANGE = 10, FINETUNINGEN = 0	12	—	58	MHz
		FREQRANGE = 11, FINETUNINGEN = 0	15	—	68	MHz
		FREQRANGE = 12, FINETUNINGEN = 0	18	—	83	MHz
		FREQRANGE = 13, FINETUNINGEN = 0	24	—	100	MHz
		FREQRANGE = 14, FINETUNINGEN = 0	28	—	119	MHz
		FREQRANGE = 15, FINETUNINGEN = 0	33	—	138	MHz
		FREQRANGE = 16, FINETUNINGEN = 0	43	—	163	MHz

Note:

1. Maximum DPLL lock time ~= 6 x (M+1) x t_{REF}, where t_{REF} is the reference clock period.

4.1.23.3 I2C Fast-mode Plus (Fm+)[1]

Table 4.33. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:
1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

4.1.24 USART SPI

SPI Master Timing

Table 4.34. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}	All USARTs except USART2	2 * $t_{HFPERCLK}$	—	—	ns
		USART2	2 * $t_{HFPERBCLK}$	—	—	ns
CS to MOSI [1] [3]	t_{CS_MO}	USART2, location 4, IOVDD = 1.8 V	-3.2	—	6.8	ns
		USART2, location 4, IOVDD = 3.0 V	-2.3	—	6.0	ns
		USART2, location 5, IOVDD = 1.8 V	-8.1	—	6.3	ns
		USART2, location 5, IOVDD = 3.0 V	-7.3	—	4.4	ns
		All other USARTs and locations, IOVDD = 1.8 V	-15	—	13	ns
		All other USARTs and locations, IOVDD = 3.0 V	-13	—	11	ns
SCLK to MOSI [1] [3]	t_{SCLK_MO}	USART2, location 4, IOVDD = 1.8 V	-0.3	—	9.2	ns
		USART2, location 4, IOVDD = 3.0 V	-0.3	—	8.6	ns
		USART2, location 5, IOVDD = 1.8 V	-3.6	—	5.0	ns
		USART2, location 5, IOVDD = 3.0 V	-3.4	—	3.2	ns
		All other USARTs and locations, IOVDD = 1.8 V	-10	—	11	ns
		All other USARTs and locations, IOVDD = 3.0 V	-9	—	11	ns
MISO setup time [1] [3]	t_{SU_MI}	USART2, location 4, IOVDD = 1.8 V	39.7	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	22.4	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	49.2	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	30.0	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	55	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	36	—	—	ns

SDIO DDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled. Slew rate for SD_CLK set to 6, all other GPIO set to 6, DRIVESTRENGTH = STRONG for all pins. SDIO_CTRL_TXDLYMUXSEL = 1. Loading between 5 and 10 pF on all pins or between 10 and 30 pF on all pins.

Table 4.49. SDIO DS Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Using HFRCO, AUXHFRCO, or USHFRCO	—	—	20	MHz
		Using HFXO	—	—	TBD	MHz
Clock low time	t_{WL}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock high time	t_{WH}	Using HFRCO, AUXHFRCO, or USHFRCO	22.6	—	—	ns
		Using HFXO	TBD	—	—	ns
Clock rise time	t_R		1.69	6.52	—	ns
Clock fall time	t_F		1.42	4.96	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}		6	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}		1.8	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}		0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}		0.8	—	—	ns
Input setup time, DAT[0:3] valid to SD_CLK	t_{ISU2X}		6	—	—	ns
Input hold time, SD_CLK to DAT[0:3] change	t_{IH2X}		1.5	—	—	ns
Output delay time, SD_CLK to DAT[0:3] valid	t_{ODLY2X}		0	—	16	ns
Output hold time, SD_CLK to DAT[0:3] change	t_{OH2X}		0.8	—	—	ns

4.1.28.2 QSPI DDR Mode

QSPI DDR Mode Timing (Location 0)

Timing is specified with voltage scaling disabled, PHY-mode, route location 0 only, TX DLL = 35, RX DLL = 70, 20-25 pF loading per GPIO, and slew rate for all GPIO set to 6, DRIVESTRENGTH = STRONG.

Table 4.56. QSPI DDR Mode Timing (Location 0)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Half SCLK period	T/2	HFXO	$(1/F_{SCLK})$ * 0.4 - 0.4	—	—	ns
		HFRCO, AUXHFRCO, USHFRCO	$(1/F_{SCLK})$ * 0.44	—	—	ns
Output valid	t_{OV}		—	—	T/2 - 5.0	ns
Output hold	t_{OH}		T/2 - 39.4	—	—	ns
Input setup	t_{SU}		33.1	—	—	ns
Input hold	t_H		-0.9	—	—	ns

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VREGVDD	J13	Voltage regulator VDD input	PC0	K1	GPIO (5V)
PC1	K2	GPIO (5V)	PE0	K12	GPIO (5V)
VREGSW	K13	DCDC regulator switching node	PC2	L1	GPIO (5V)
PC3	L2	GPIO (5V)	PA7	L3	GPIO
PB9	L13	GPIO (5V)	PB10	L14	GPIO (5V)
PD1	L17	GPIO	PC6	L18	GPIO
PC7	L19	GPIO	VREGVSS	L20	Voltage regulator VSS
PB7	M1	GPIO	PC4	M2	GPIO
PA8	M3	GPIO	PA10	M4	GPIO
PA13	M5	GPIO (5V)	PA14	M6	GPIO
RESETn	M7	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB12	M8	GPIO
PD0	M9	GPIO (5V)	PD2	M10	GPIO (5V)
PD3	M11	GPIO	PD4	M12	GPIO
PD8	M13	GPIO	PB8	N1	GPIO
PC5	N2	GPIO	PA9	N3	GPIO
PA11	N4	GPIO	PA12	N5	GPIO (5V)
PB11	N6	GPIO	BODEN	N7	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.
PB13	N8	GPIO	PB14	N9	GPIO
AVDD	N10	Analog power supply.	PD5	N11	GPIO
PD6	N12	GPIO	PD7	N13	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.4 EFM32GG11B5xx in BGA120 Device Pinout

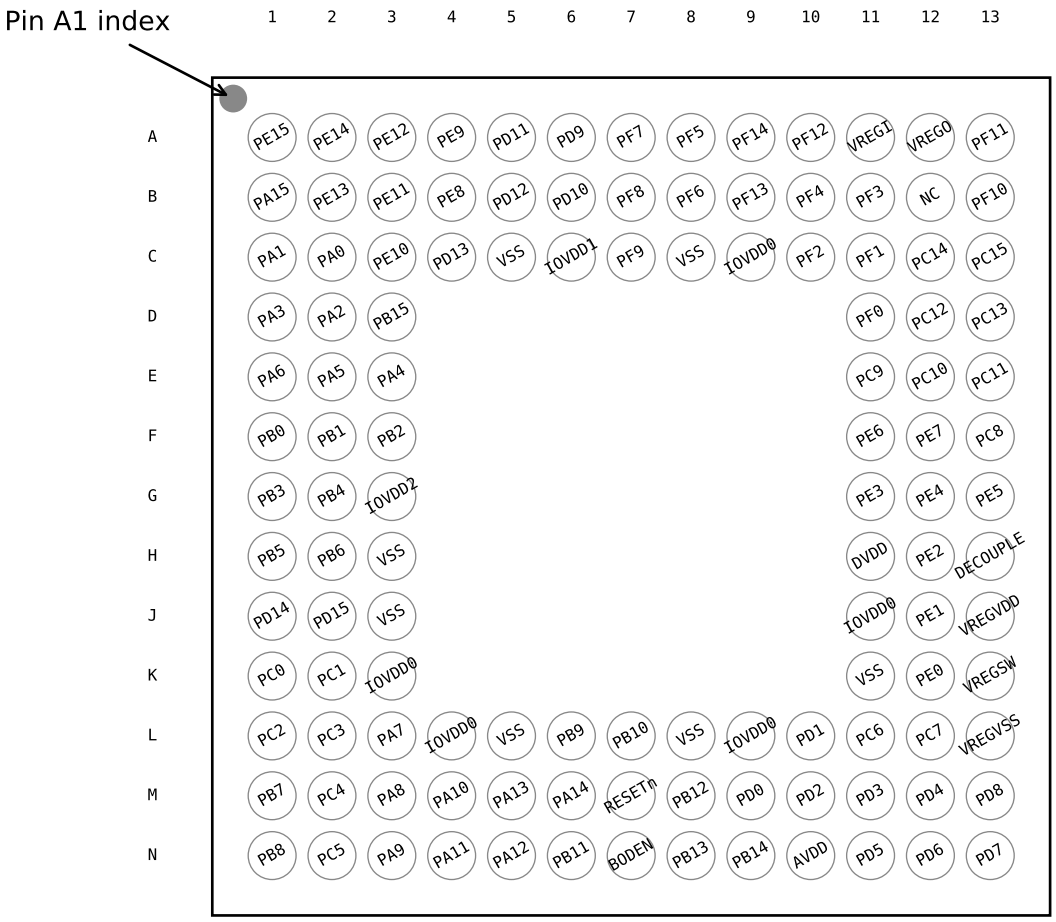


Figure 5.4. EFM32GG11B5xx in BGA120 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.20 GPIO Functionality Table or 5.21 Alternate Functionality Overview.

Table 5.4. EFM32GG11B5xx in BGA120 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PE15	A1	GPIO	PE14	A2	GPIO
PE12	A3	GPIO	PE9	A4	GPIO
PD11	A5	GPIO	PD9	A6	GPIO
PF7	A7	GPIO	PF5	A8	GPIO
PF14	A9	GPIO (5V)	PF12	A10	GPIO
VREGI	A11	Input to 5 V regulator.	VREGO	A12	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC1	J1	GPIO (5V)	PC3	J2	GPIO (5V)
PD15	J3	GPIO (5V)	PA12	J4	GPIO (5V)
PA9	J5	GPIO	PA10	J6	GPIO
PB9	J7	GPIO (5V)	PB10	J8	GPIO (5V)
PD2	J9	GPIO (5V)	PD3	J10	GPIO
PD4	J11	GPIO	PB7	K1	GPIO
PC4	K2	GPIO	PA13	K3	GPIO (5V)
PA11	K5	GPIO	RESETn	K6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
AVDD	K8 K9 L10	Analog power supply.	PD1	K11	GPIO
PB8	L1	GPIO	PC5	L2	GPIO
PA14	L3	GPIO	PB11	L5	GPIO
PB12	L6	GPIO	PB13	L8	GPIO
PB14	L9	GPIO	PD0	L11	GPIO (5V)

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 58 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB9	37	GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41 45	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	46	GPIO (5V)	PD1	47	GPIO
PD2	48	GPIO (5V)	PD3	49	GPIO
PD4	50	GPIO	PD5	51	GPIO
PD6	52	GPIO	PD7	53	GPIO
PD8	54	GPIO	PC6	55	GPIO
PC7	56	GPIO	DVDD	57	Digital power supply.
DECOUPLE	59	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE0	60	GPIO (5V)
PE1	61	GPIO (5V)	PE2	62	GPIO
PE3	63	GPIO	PE4	64	GPIO
PE5	65	GPIO	PE6	66	GPIO
PE7	67	GPIO	PC8	68	GPIO (5V)
PC9	69	GPIO (5V)	PC10	70	GPIO (5V)
PC11	71	GPIO (5V)	VREGI	72	Input to 5 V regulator.
VREGO	73	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs	PF10	74	GPIO (5V)
PF11	75	GPIO (5V)	PF0	76	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF3	79	GPIO	PF4	80	GPIO
PF5	81	GPIO	PF6	84	GPIO
PF7	85	GPIO	PF8	86	GPIO
PF9	87	GPIO	PD9	88	GPIO
PD10	89	GPIO	PD11	90	GPIO
PD12	91	GPIO	PE8	92	GPIO
PE9	93	GPIO	PE10	94	GPIO
PE11	95	GPIO	PE12	96	GPIO
PE13	97	GPIO	PE14	98	GPIO
PE15	99	GPIO	PA15	100	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM4_CDTI2	0: PD3		Timer 4 Complimentary Dead Time Insertion channel 2.
TIM5_CC0	0: PE4 1: PE7 2: PH13 3: PI0	4: PC8 5: PC11 6: PC14 7: PF12	Timer 5 Capture Compare input / output channel 0.
TIM5_CC1	0: PE5 1: PH11 2: PH14 3: PI1	4: PC9 5: PC12 6: PF10 7: PF13	Timer 5 Capture Compare input / output channel 1.
TIM5_CC2	0: PE6 1: PH12 2: PH15 3: PI2	4: PC10 5: PC13 6: PF11 7: PF14	Timer 5 Capture Compare input / output channel 2.
TIM6_CC0	0: PG0 1: PG6 2: PG12 3: PH2	4: PH8 5: PB13 6: PD1 7: PD4	Timer 6 Capture Compare input / output channel 0.
TIM6_CC1	0: PG1 1: PG7 2: PG13 3: PH3	4: PH9 5: PB14 6: PD2 7: PD5	Timer 6 Capture Compare input / output channel 1.
TIM6_CC2	0: PG2 1: PG8 2: PG14 3: PH4	4: PH10 5: PD0 6: PD3 7: PD6	Timer 6 Capture Compare input / output channel 2.
TIM6_CDTI0	0: PG3 1: PG9 2: PE4 3: PH5		Timer 6 Complimentary Dead Time Insertion channel 0.
TIM6_CDTI1	0: PG4 1: PG10 2: PE5 3: PH6		Timer 6 Complimentary Dead Time Insertion channel 1.
TIM6_CDTI2	0: PG5 1: PG11 2: PE6 3: PH7		Timer 6 Complimentary Dead Time Insertion channel 2.
U0_CTS	0: PF8 1: PE2 2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.
U0_RTS	0: PF9 1: PE3 2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	0: PF7 1: PE1 2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.

Table 5.27. ADC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSADC0X																									PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
APORT0Y	BUSADC0Y																									PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

9.3 BGA112 Package Marking

Figure 9.3. BGA112 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

13. Revision History

Revision 0.6

March, 2018

- Removed "Confindential" watermark.
- Updated 4.1 Electrical Characteristics and 4.2 Typical Performance Curves with latest characterization data.

Revision 0.2

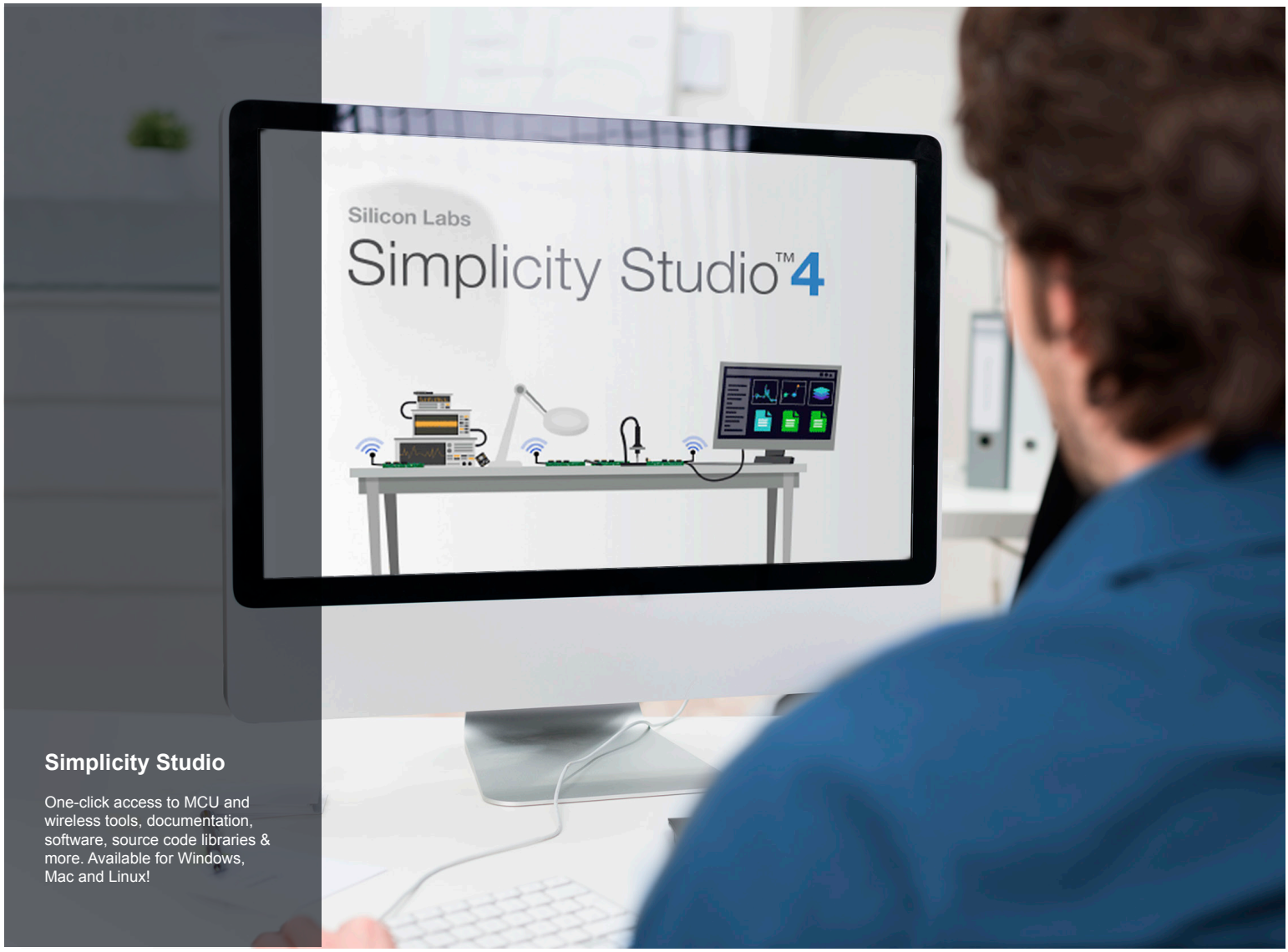
October, 2017

- Updated memory maps to latest formatting and to include all peripherals.
- Updated all electrical specifications tables with latest characterization results.
- **Absolute Maximum Ratings** Table:
  - Removed redundant I_{VSSMAX} line.
  - Added footnote to clarify V_{DIGPIN} specification for 5V tolerant GPIO.
- **General Operating Conditions** Table:
  - Removed dV_{DD} specification and redundant footnote about shorting VREGVDD and AVDD together.
  - Added footnote about IOVDD voltage restriction when CSEN peripheral is used with chopping enabled.
- **Flash Memory Characteristics** Table: Added timing measurement clarification for Device Erase and Mass Erase.
- **Analog to Digital Converter (ADC)** Table:
  - Added header text for general specification conditions.
  - Added footnote for clarification of input voltage limits.
- Minor typographical corrections, including capitalization, mis-spellings and punctuation marks, throughout document.
- Minor formatting and styling updates, including table formats, TOC location, and boilerplate information throughout document.

Revision 0.1

April 27th, 2017

Initial release.



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