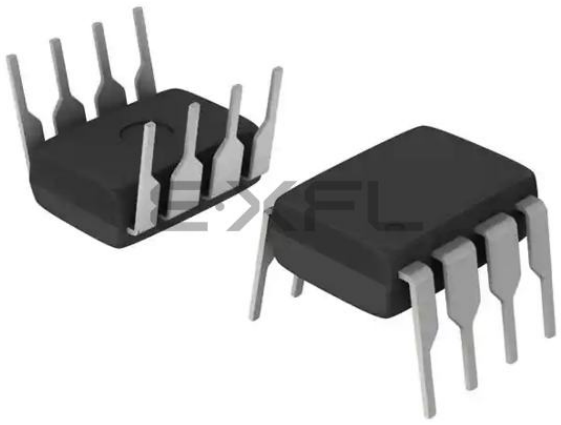

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Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 2x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24123-24pi

1.2 Pinouts

The PSoC devices are available in a variety of packages. Refer to the following information for details on individual devices. Note that every port pin (labeled with a “P”), except for Vss, Vdd, SMP, and XRES in the following tables and illustrations, is capable of Digital IO.

Table 1-2. 8-Pin Part Pinout (PDIP, SOIC)

Pin No.	Description
1	P0[5], A in, out
2	P0[3], A in, out
3	P1[1], XTALin, I^2C SCL

Pin No.	Description
4	Vss
5	P1[0], XTALout, I^2C SDA
6	P0[2], A in

Pin No.	Description
7	P0[4], A in
8	Vdd

LEGEND A: analog, D: digital, IO: input or output.

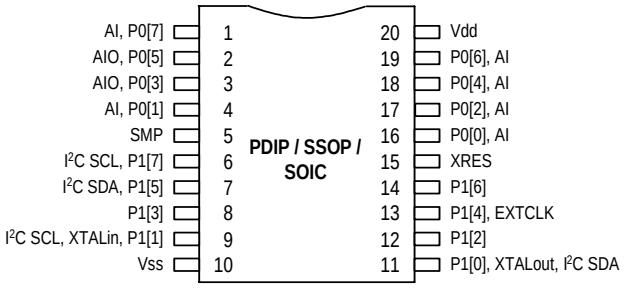
Table 1-3. 20-Pin Part Pinout (PDIP, SSOP, SOIC)

Pin No.	Description
1	P0[7], A in
2	P0[5], A in, out
3	P0[3], A in, out
4	P0[1], A in
5	SMP
6	P1[7], I^2C SCL
7	P1[5], I^2C SDA

Pin No.	Description
8	P1[3]
9	P1[1], XTALin, I^2C SCL
10	Vss
11	P1[0], XTALout, I^2C SDA
12	P1[2]
13	P1[4], EXTCLK
14	P1[6]

Pin No.	Description
15	XRES
16	P0[0], A in
17	P0[2], A in
18	P0[4], A in
19	P0[6], A in
20	Vdd

LEGEND A: analog, D: digital, IO: input or output.



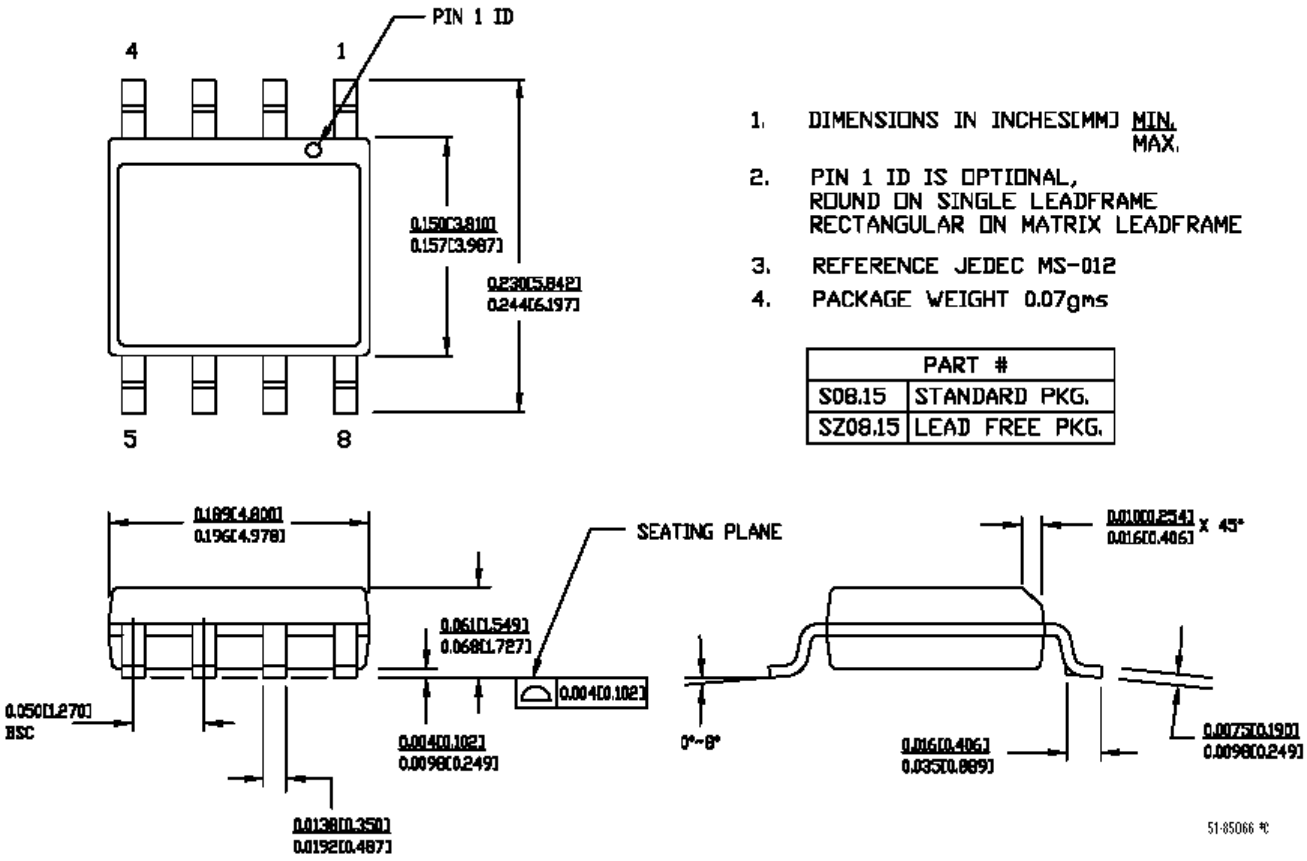


Figure 2-2. 8-Lead (150-Mil) SOIC

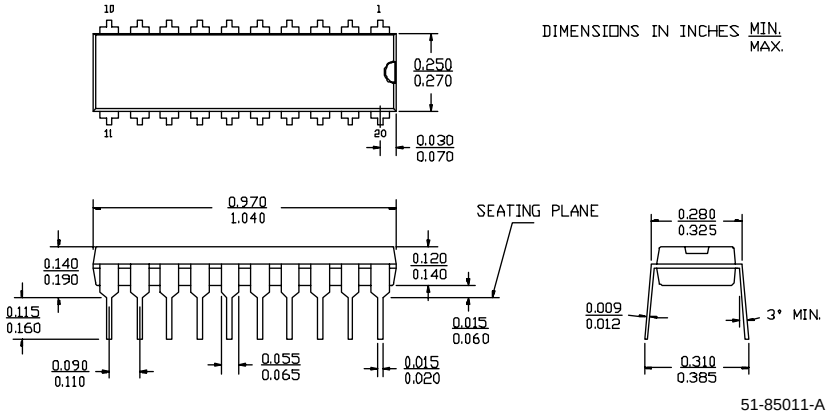


Figure 2-3. 20-Lead (300-Mil) Molded DIP

13.1.45 INT_CLR1

Interrupt Clear Register 1

Individual Register Names and Addresses

INT_CLR1: 0,DBh

	7	6	5	4	3	2	1	0
Access : POR					RW : 0	RW : 0	RW : 00	RW : 0
Bit Name					DCB03	DCB02	DBB01	DBB00

When bits in this register are read, a ‘1’ will be returned for every bit position that has a corresponding posted interrupt. When bits in this register are written with a zero (0) and ENSWINT is not set, posted interrupts will be cleared at the corresponding bit positions. If there was not a posted interrupt, there is no effect. When bits in this register are written with a one (1) and ENSWINT is set, an interrupt is posted in the interrupt controller. Note that the ENSWINT bit is in the INT_MSK3 register on page 135. For additional information, reference the “Register Definitions” on page 55 in the Interrupt Controller chapter.

Bit	Name	Description
[7:4]	**Reserved**	
[3]	**DCB03**	Digital Communications Block type B, row 0, position 3. Read 0 No posted interrupt. Read 1 Posted interrupt present. Write 0 AND ENSWINT = 0 Clear posted interrupt if it exists. Write 1 AND ENSWINT = 0 No effect. Write 0 AND ENSWINT = 1 No effect. Write 1 AND ENSWINT = 1 Post an interrupt.
[2]	**DCB02**	Digital Communications Block type B, row 0, position 2. Read 0 No posted interrupt. Read 1 Posted interrupt present. Write 0 AND ENSWINT = 0 Clear posted interrupt if it exists. Write 1 AND ENSWINT = 0 No effect. Write 0 AND ENSWINT = 1 No effect. Write 1 AND ENSWINT = 1 Post an interrupt.
[1]	**DBB01**	Digital Basic Block type B, row 0, position 1. Read 0 No posted interrupt. Read 1 Posted interrupt present. Write 0 AND ENSWINT = 0 Clear posted interrupt if it exists. Write 1 AND ENSWINT = 0 No effect. Write 0 AND ENSWINT = 1 No effect. Write 1 AND ENSWINT = 1 Post an interrupt.
[0]	**DBB00**	Digital Basic Block type B, row 0, position 0. Read 0 No posted interrupt. Read 1 Posted interrupt present. Write 0 AND ENSWINT = 0 Clear posted interrupt if it exists. Write 1 AND ENSWINT = 0 No effect. Write 0 AND ENSWINT = 1 No effect. Write 1 AND ENSWINT = 1 Post an interrupt.

13.1.46 INT_CLR3

Interrupt Clear Register 3

Individual Register Names and Addresses

INT_CLR3: 0,DDh

	7	6	5	4	3	2	1	0
Access : POR								RW : 0
Bit Name								I2C

When bits in this register are read, a ‘1’ will be returned for every bit position that has a corresponding posted interrupt. When bits in this register are written with a zero (0) and ENSWINT is cleared, any posted interrupt will be cleared. If there was not a posted interrupt, there is no effect. When bits in this register are written with a one (1) and ENSWINT is set, an interrupt is posted in the interrupt controller. For additional information, reference the “Register Definitions” on page 55 in the Interrupt Controller chapter.

Bit	Name	Description
[7:1]	**Reserved**	
[0]	**I2C**	Read 0 No posted interrupt for I2C. Read 1 Posted interrupt present for I2C. Write 0 AND ENSWINT = 0 Clear posted interrupt if it exists. Write 1 AND ENSWINT = 0 No effect. Write 0 AND ENSWINT = 1 No effect. Write 1 AND ENSWINT = 1 Post an interrupt for I2C.

13.1.48 INT_MSK0

Interrupt Mask Register 0

Individual Register Names and Addresses

INT_MSK0: 0,E0h

	7	6	5	4	3	2	1	0
Access : POR	RW : 0	RW : 0	RW : 0			RW : 0	RW : 0	RW : 0
Bit Name	VC3	Sleep	GPIO			Analog 1	Analog 0	V Monitor

Note that when an interrupt is masked off, the mask bit is ‘0’. The interrupt will still post in the interrupt controller. Therefore, clearing the mask bit only prevents a posted interrupt from becoming a pending interrupt. For additional information, reference the “Register Definitions” on page 55 in the Interrupt Controller chapter.

Bit	Name	Description	
[7]	**VC3**	0 1	Mask VC3 interrupt. Unmask VC3 interrupt.
[6]	**Sleep**	0 1	Mask sleep interrupt. Unmask sleep interrupt.
[5]	**GPIO**	0 1	Mask GPIO interrupt. Unmask GPIO interrupt.
[4:3]	**Reserved**		
[2]	**Analog 1**	0 1	Mask analog interrupt, column 1. Unmask analog interrupt.
[1]	**Analog 0**	0 1	Mask analog interrupt, column 0. Unmask analog interrupt.
[0]	**V Monitor**	0 1	Mask voltage monitor interrupt. Unmask voltage monitor interrupt.

13.1.59 MUL_DL

Multiply Result Low Byte Register

Individual Register Names and Addresses

MUL_DL: 0,EBh

	7	6	5	4	3	2	1	0
Access : POR	R : 00							
Bit Name	Data[7:0]							

For additional information, reference the “Register Definitions” on page 270 in the Multiply Accumulate chapter.

Bit	Name	Description
[7:0]	**Data[7:0]**	Low byte of MAC multiplier 16-bit product.

13.2.8 CLK_CR0

Analog Column Clock Control Register 0

Individual Register Names and Addresses

CLK_CR0: 1,60h

	7	6	5	4	3	2	1	0
Access : POR					RW : 0		RW : 0	
Bit Name					Acolumn1[1:0]		Acolumn0[1:0]	

Each column has two bits that select the column clock input source. The resulting column clock frequency is the selected input clock frequency divided by four. For additional information, reference the “Register Definitions” on page 238 in the Analog Interface chapter.

Bit	Name	Description
[7:4]	**Reserved**	
[3:2]	**Acolumn1[1:0]**	Clock selection for column 1. 00b Variable Clock 1 (VC1) 01b Variable Clock 2 (VC2) 10b Analog Clock 0 (ACLK0) 11b Analog Clock 1 (ACLK1)
[1:0]	**Acolumn0[1:0]**	Clock selection for column 0. 00b Variable Clock 1 (VC1) 01b Variable Clock 2 (VC2) 10b Analog Clock 0 (ACLK0) 11b Analog Clock 1 (ACLK1)

13.2.28 ECO_TR

External Crystal Oscillator Trim Register

Individual Register Names and Addresses

ECO_TR: 1,EBh

	7	6	5	4	3	2	1	0
Access : POR	W : 0							
Bit Name	PSSDC[1:0]							

The value of this register is used to trim the External Crystal Oscillator. Its value is set to the device specific, best value during boot. The value in this register should not be changed. For additional information, reference the “Register Definitions” on page 70 in the 32 kHz Crystal Oscillator chapter.

Bit	Name	Description
[7:6]	**PSSDC[1:0]**	Sleep duty cycle. Controls the ratios (in numbers of 32 kHz clock periods) of “on” time versus “off” time for PORLVD, Bandgap reference, and pspump. 00b 1 / 128 01b 1 / 512 10b 1 / 32 11b 1 / 8
[5:0]	**Reserved**	

17.2 Register Definitions

The Digital Block registers in this chapter are organized by function, as presented in Table 17-5. To reference timing diagrams associated with the digital block registers, see "Timing Diagrams" on page 214. For a complete list of the Digital Block registers showing their addresses and bit names, reference the "Digital Register Summary" on page 186.

Table 17-5. Digital Block Register Definitions

	DR0		DR1		DR2		CR0	
	Function	**Access**	**Function**	**Access**	**Function**	**Access**	**Function**	**Access**
Timer	Down Counter	R*	Period	W	Capture/Compare	RW	Control	RW
Counter	Down Counter	R*	Period	W	Compare	RW	Control	RW
Dead Band	Down Counter	R*	Period	W	N/A	N/A	Control	RW
CRCPRS	LFSR	R*	Polynomial	W	Seed	RW	Control	RW
SPIM	Shifter	N/A	TX Buffer	W	RX Buffer	R	Control/Status	RW**
SPIS	Shifter	N/A	TX Buffer	W	RX Buffer	R	Control/Status	RW**
TXUART	Shifter	N/A	TX Buffer	W	N/A	N/A	Control/Status	RW**
RXUART	Shifter	N/A	N/A	N/A	RX Buffer	R	Control/Status	RW**

LEGEND
* In Timer, Counter, Dead Band, and CRCPRS functions, a read of the DR0 register returns 00h and transfers DR0 to DR2.

** In the Communications functions, control bits are Read-Write access and status bits are Read-Only access.

Data and Control Registers

17.2.1 DxBxxDRx Registers

The Data and Control registers presented in this section encompass the DxBxxDR0, DxBxxDR1, and DxBxxDR2 registers. They are discussed according to which bank they are located in and then detailed in tables by function type.

There are two banks of registers associated with the PSoC device. Bank 0 encompasses the user registers for the device and Bank 1 encompasses the configuration registers for the device. Both are defined below. Reference the "Bank 0 Registers" on page 88 and the "Bank 1 Registers" on page 155 for more information.

For additional information, reference the Register Details chapter for the following registers:

- DxBxxDR0 register on page 92.
- DxBxxDR1 register on page 93.
- DxBxxDR2 register on page 94.

17.2.1.1 Timer Register Definitions

Bank 0: There are three 8-bit data registers and a 3-bit control register. Table 17-6 explains the meaning of these registers in the context of timer operation.

Bank 1: The mode bits in the Function register are block type specific. Other bit fields in this register, as well as the definitions of the Input and Output registers, are common to all functions and are described in the "DxBxxIN Registers" on page 214 and the "DxBxxOU Registers" on page 214.

These mode bits are independent in the Timer block and control the Interrupt Type and the Compare Type. Timers have a special divide by one mode, when the period of the DR0 register is set to 00h. In this configuration, the primary output Terminal Count (TC) is the inverted input clock. The interrupt output is also the input clock inverted.

Table 17-6. Timer Data Register Descriptions

Name	Function	Description
DR0	Count Value	Not Directly Readable or Writeable. During normal operation, DR0 stores the current count of a synchronous down counter. When disabled, a write to the DR1 Period register is also simultaneously loaded into DR0 from the data bus. When disabled, a read of DR0 returns 00h to the data bus and transfers the contents of DR0 to DR2. This transfer only occurs in the addressed block. When enabled, a read of DR0 returns 00h to the data bus and synchronously transfers the contents of DR0 to DR2. Operates simultaneously on the byte addressed and all higher bytes in a multi-block timer. Note that when the hardware capture input is high, the read of DR0 (software capture) will be masked and will not occur. The hardware capture input must be low for a software capture to occur.

Analog Register Summary

The table below lists all the PSoC registers in the analog system.

Summary Table of the Analog Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
ANALOG INTERFACE REGISTERS										
0,64h	CMP_CR0			COMP[1]	COMP[0]			AINT[1]	AINT[0]	RW : 00
0,66h	CMP_CR1			CLDIS[1]	CLDIS[0]					RW : 00
0,65h	ASY_CR		SARCNT[2:0]			SARSIGN	SARCOL[1:0]		SYNCEN	RW : 00
0,E6h	DEC_CR0	IGEN[3:0]				ICLKS0	DCOL[1:0]		DCLKS0	RW : 00
0,E7h	DEC_CR1	ECNT	IDEC			ICLKS1			DCLKS1	RW : 00
1,60h	CLK_CR0					Acolumn1[1:0]		Acolumn0[1:0]		RW : 00
1,61h	CLK_CR1		SHDIS	ACLK1[2:0]			ACLK0[2:0]			RW : 00
1,63h	AMD_CR0						AMOD0[2:0]			RW : 00
1,66h	AMD_CR1						AMOD1[2:0]			RW : 00
1,67h	ALT_CR0	LUT1[3:0]				LUT0[3:0]				RW : 00
ANALOG INPUT CONFIGURATION REGISTERS										
0,60h	AMX_IN					ACI1[1:0]		ACI0[1:0]		RW : 00
1,62h	ABF_CR0	ACol1Mux		ABUF1EN0		ABUF0EN0		Bypass	PWR	RW : 00
ANALOG REFERENCE REGISTER										
0,63h	ARF_CR		HBE	REF[2:0]			PWR[2:0]			RW : 00
SWITCHED CAPACITOR BLOCK REGISTERS										
Switched Capacitor Block Registers, Type C										
x,80h	ASC10CR0	FCap	ClockPhase	ASign	ACap[4:0]					RW : 00
x,81h	ASC10CR1	ACMux[2:0]			BCap[4:0]					RW : 00
x,82h	ASC10CR2	AnalogBus	CompBus	AutoZero	CCap[4:0]					RW : 00
x,83h	ASC10CR3	ARefMux[1:0]		FSW1	FSW0	BMuxSC[1:0]		PWR[1:0]		RW : 00
x,94h	ASC21CR0	FCap	ClockPhase	ASign	ACap[4:0]					RW : 00
x,95h	ASC21CR1	ACMux[2:0]			BCap[4:0]					RW : 00
x,96h	ASC21CR2	AnalogBus	CompBus	AutoZero	CCap[4:0]					RW : 00
x,97h	ASC21CR3	ARefMux[1:0]		FSW1	FSW0	BMuxSC[1:0]		PWR[1:0]		RW : 00
Switched Capacitor Block Registers, Type D										
x,84h	ASD11CR0	FCap	ClockPhase	ASign	ACap[4:0]					RW : 00
x,85h	ASD11CR1	AMux[2:0]			BCap[4:0]					RW : 00
x,86h	ASD11CR2	AnalogBus	CompBus	AutoZero	CCap[4:0]					RW : 00
x,87h	ASD11CR3	ARefMux[1:0]		FSW1	FSW0	BSW	BMuxSD	PWR[1:0]		RW : 00
x,90h	ASD20CR0	FCap	ClockPhase	ASign	ACap[4:0]					RW : 00
x,91h	ASD20CR1	AMux[2:0]			BCap[4:0]					RW : 00
x,92h	ASD20CR2	AnalogBus	CompBus	AutoZero	CCap[4:0]					RW : 00
x,93h	ASD20CR3	ARefMux[1:0]		FSW1	FSW0	BSW	BMuxSD	PWR[1:0]		RW : 00
CONTINUOUS TIME BLOCK REGISTERS										
x,70h	ACB00CR3					LPCMPEN	CMOUT	INSAMP	EXGAIN	RW : 00
x,71h	ACB00CR0	RTapMux[3:0]				Gain	RTopMux	RBotMux[1:0]		RW : 00
x,72h	ACB00CR1	AnalogBus	CompBus	NMux[2:0]			PMux[2:0]			RW : 00
x,73h	ACB00CR2	CPhase	CLatch	CompCap	TMUXEN	TestMux[1:0]		PWR[1:0]		RW : 00
x,74h	ACB01CR3					LPCMPEN	CMOUT	INSAMP	EXGAIN	RW : 00
x,75h	ACB01CR0	RTapMux[3:0]				Gain	RTopMux	RBotMux[1:0]		RW : 00
x,76h	ACB01CR1	AnalogBus	CompBus	NMux[2:0]			PMux[2:0]			RW : 00
x,77h	ACB01CR2	CPhase	CLatch	CompCap	TMUXEN	TestMux[1:0]		PWR[1:0]		RW : 00

LEGEND
x: An “x” before the comma in the address field indicates that this register can be accessed or written to no matter what bank is used.

20.2 Architectural Description

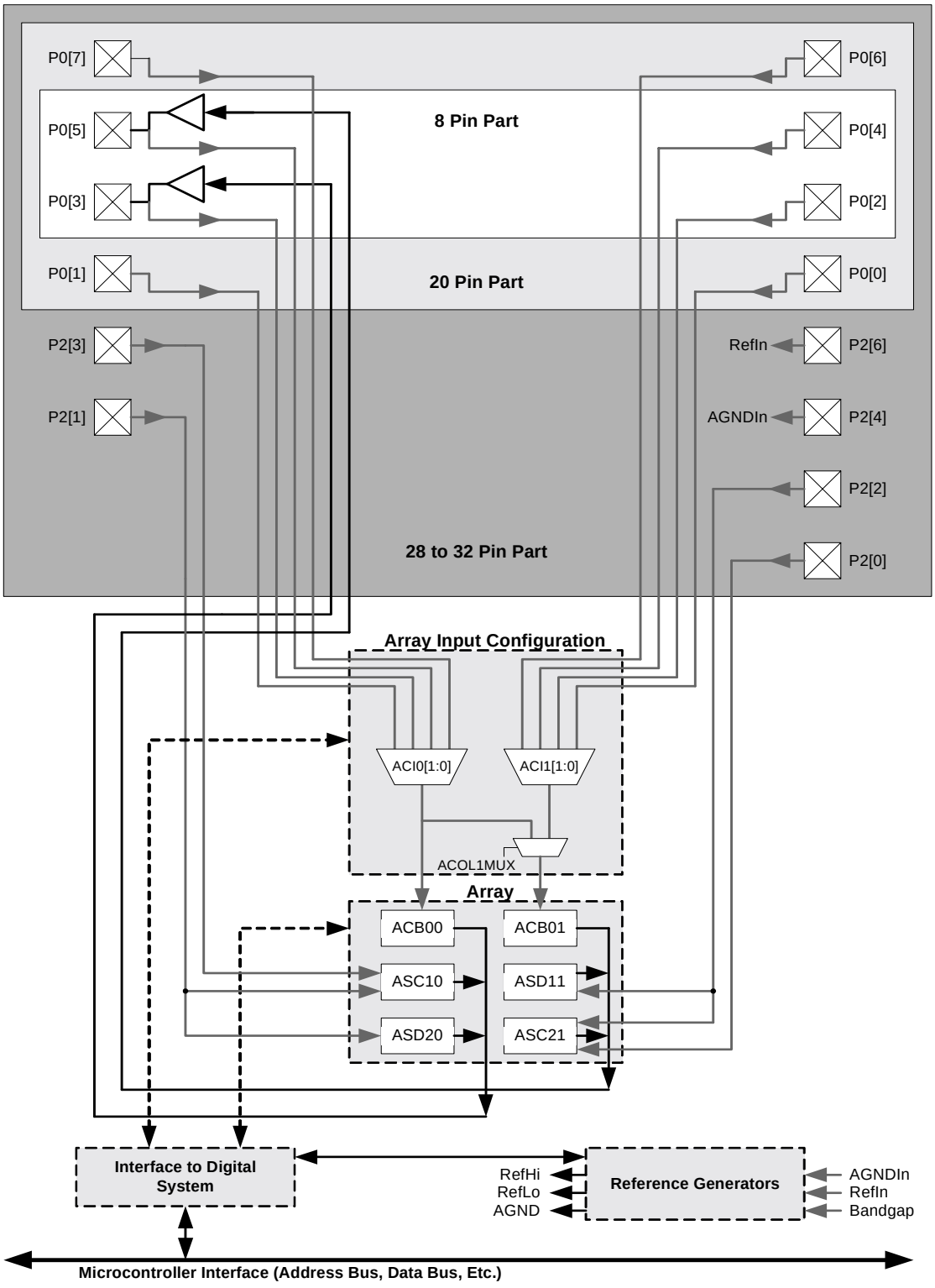


Figure 20-1. Analog Pin Block Diagram

21. Analog Reference

This chapter discusses the Analog Reference generator and its associated register. The reference generator establishes a set of three internally fixed reference voltages for AGND, RefHi, and RefLo.

Table 21-1. Analog Reference Register

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Access
0,63h	ARF_CR		HBE	REF[2:0]			PWR[2:0]			RW : 00

21.1 Architectural Description

The PSoC device is a single supply part, with no negative voltage available or applicable. Analog ground (AGND) is constructed near mid-supply. This ground is routed to all analog blocks and separately buffered within each block. Note that there may be a small offset voltage between buffered analog grounds. RefHi and RefLo signals are generated, buffered, and routed to the analog blocks. RefHi and RefLo are used to set the conversion range (i.e., span) of analog to digital (ADC) and digital to analog (DAC) converters. RefHi and RefLo can also be used to set thresholds in comparators.

The reference array supplies voltage to all blocks and current to the Switched Capacitor blocks. At higher block clock rates, there is increased reference current demand; the reference power should be set equal to the highest power level of the analog blocks used.

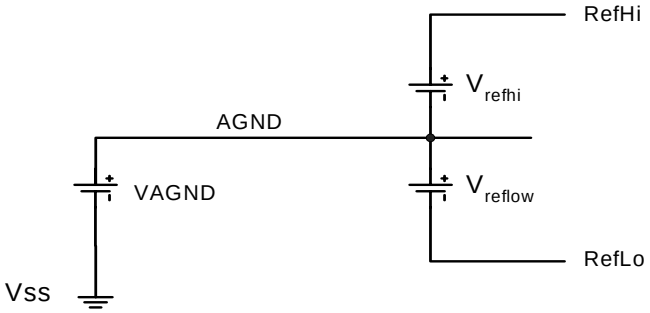


Figure 21-1. Reference Structure

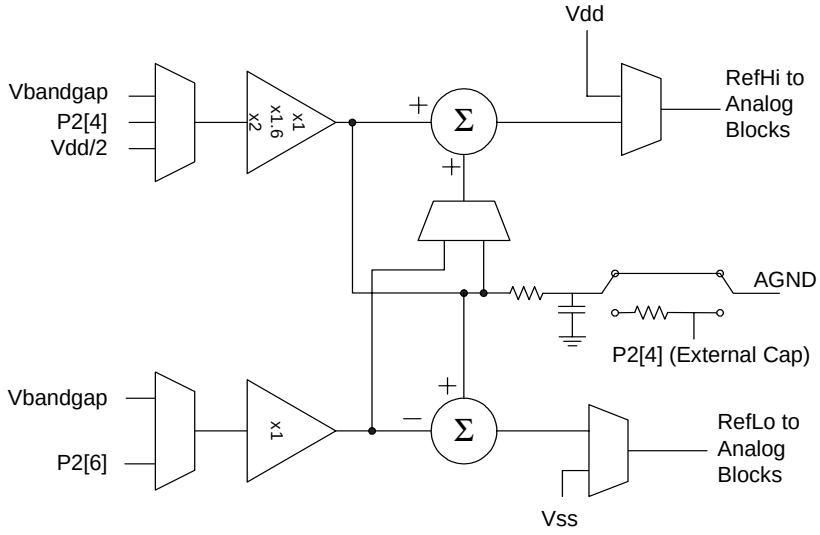


Figure 21-2. Analog Reference Control Schematic

Bit 2: CMOUT. The analog array may be used to build two different forms of instrumentation amplifiers. Two continuous time blocks combine to make a 2-opamp instrumentation amplifier (see Figure 23-2).

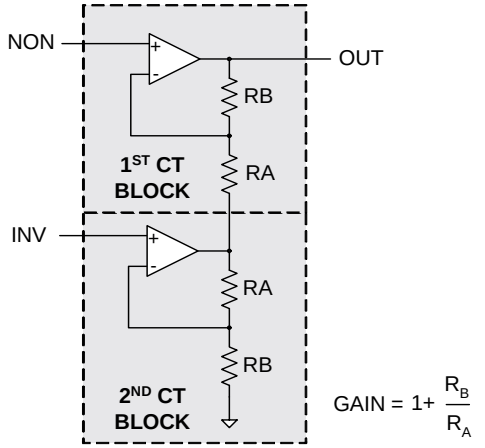


Figure 23-2. 2-Opamp Instrumentation Amplifier

Two continuous time blocks and one switched capacitor block combine to make a 3-opamp instrumentation amplifier (see Figure 23-3).

The 3-opamp instrumentation amplifier takes more resources, but handles a larger common mode input range. Bit2 (CMOUT) and bit1 (INSAMP) control switches are involved in the 3-opamp instrumentation amplifier. If bit2 (CMOUT) is high, then the node formed by the connection of the resistors between the continuous time blocks is connected to that continuous time block's ABus. This node is the common mode of the inputs to the instrumentation amplifier. The CMOUT bit is optional for the 3-opamp instrumentation amplifier.

Bit 1: INSAMP. This bit is used to connect the resistors of two continuous time blocks as part of a 3-opamp instrumentation amplifier. The INSAMP bit must be high for the 3-opamp instrumentation amplifier (see Figure 23-3).

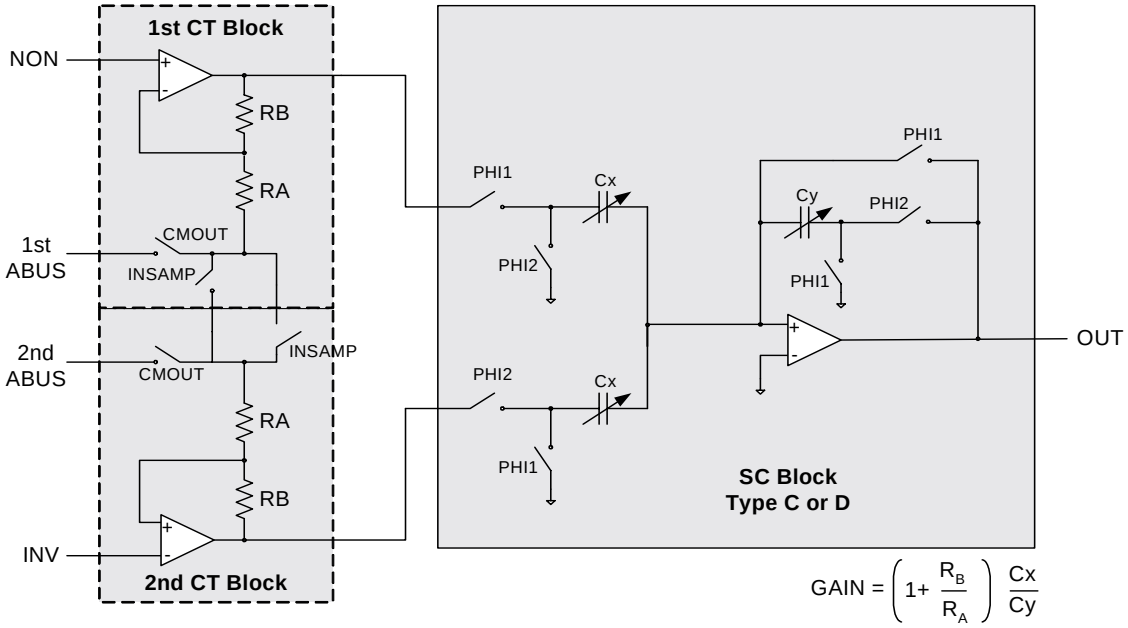


Figure 23-3. 3-Opamp Instrumentation Amplifier

24.2.4 OSC_CR1 Register

Bits 7 to 4: VC1 Divider[3:0]. The VC1 clock net is one of the variable clock nets available in the PSoC M8C. The source for the VC1 clock net is a simple 4-bit divider. The source for the divider is 24 MHz system clock; however, if the device is configured to use an external clock, the input to the divider will be the external clock. Therefore, the VC1 clock net is not always the result of dividing down a 24 MHz clock. The 4-bit divider that controls the VC1 clock net may be configured to divide, using any integer value between 1 and 16. Table 24-4 lists all values for the VC1 clock net.

Table 24-4. OSC_CR1[7:4] Bits: VC1 Divider Value

	Divider Source Clock	
Bits	Internal Main Oscillator	External Clock
0h	24 MHz	EXTCLK / 1
1h	12 MHz	EXTCLK / 2
2h	8 MHz	EXTCLK / 3
3h	6 MHz	EXTCLK / 4
4h	4.8 MHz	EXTCLK / 5
5h	4 MHz	EXTCLK / 6
6h	3.43 MHz	EXTCLK / 7
7h	3 MHz	EXTCLK / 8
8h	2.67 MHz	EXTCLK / 9
9h	2.40 MHz	EXTCLK / 10
Ah	2.18 MHz	EXTCLK / 11
Bh	2.00 MHz	EXTCLK / 12
Ch	1.85 MHz	EXTCLK / 13
Dh	1.71 MHz	EXTCLK / 14
Eh	1.6 MHz	EXTCLK / 15
Fh	1.5 MHz	EXTCLK / 16

Bits 3 to 0: VC2 Divider[3:0]. The VC2 clock net is one of the variable clock nets available in the PSoC M8C. The source for the VC2 clock net is a simple 4-bit divider. The source for the divider is the VC1 clock net. The 4-bit divider that controls the VC2 clock net may be configured to divide, using any integer value between 1 and 16. Table 24-5 lists all values for the VC2 clock net.

Table 24-5. OSC_CR1[3:0] Bits: VC2 Divider Value

	Divider Source Clock	
Bits	Internal Main Oscillator	External Clock
0h	(24 / (OSC_CR1[7:4]+1)) / 1	(EXTCLK / (OSC_CR1[7:4]+1)) / 1
1h	(24 / (OSC_CR1[7:4]+1)) / 2	(EXTCLK / (OSC_CR1[7:4]+1)) / 2
2h	(24 / (OSC_CR1[7:4]+1)) / 3	(EXTCLK / (OSC_CR1[7:4]+1)) / 3
3h	(24 / (OSC_CR1[7:4]+1)) / 4	(EXTCLK / (OSC_CR1[7:4]+1)) / 4
4h	(24 / (OSC_CR1[7:4]+1)) / 5	(EXTCLK / (OSC_CR1[7:4]+1)) / 5
5h	(24 / (OSC_CR1[7:4]+1)) / 6	(EXTCLK / (OSC_CR1[7:4]+1)) / 6
6h	(24 / (OSC_CR1[7:4]+1)) / 7	(EXTCLK / (OSC_CR1[7:4]+1)) / 7
7h	(24 / (OSC_CR1[7:4]+1)) / 8	(EXTCLK / (OSC_CR1[7:4]+1)) / 8
8h	(24 / (OSC_CR1[7:4]+1)) / 9	(EXTCLK / (OSC_CR1[7:4]+1)) / 9
9h	(24 / (OSC_CR1[7:4]+1)) / 10	(EXTCLK / (OSC_CR1[7:4]+1)) / 10
Ah	(24 / (OSC_CR1[7:4]+1)) / 11	(EXTCLK / (OSC_CR1[7:4]+1)) / 11
Bh	(24 / (OSC_CR1[7:4]+1)) / 12	(EXTCLK / (OSC_CR1[7:4]+1)) / 12
Ch	(24 / (OSC_CR1[7:4]+1)) / 13	(EXTCLK / (OSC_CR1[7:4]+1)) / 13
Dh	(24 / (OSC_CR1[7:4]+1)) / 14	(EXTCLK / (OSC_CR1[7:4]+1)) / 14
Eh	(24 / (OSC_CR1[7:4]+1)) / 15	(EXTCLK / (OSC_CR1[7:4]+1)) / 15
Fh	(24 / (OSC_CR1[7:4]+1)) / 16	(EXTCLK / (OSC_CR1[7:4]+1)) / 16

For additional information, reference the OSC_CR1 register on page 177.

24.2.5 OSC_CR2 Register

Bit 7: PLLGAIN. This is the only bit in the OSC_CR2 register that directly influences the PLL. When set, this bit keeps the PLL in a low gain mode.

Bits 6 to 3: Reserved.

Bit 2: EXTCLKEN. When the EXTCLKEN bit is set, the external clock becomes the source for the internal clock tree, SYSCLK, which drives most chip clocking functions. All external and internal signals, including the 32 kHz clock, whether derived from the internal low speed oscillator (ILO) or the crystal oscillator, are synchronized to this clock source. If an external clock is enabled, PLL mode should be off.

Bit 1: IMODIS. When set, the Internal Main Oscillator is disabled. If the doubler is enabled (SYSCLKX2DIS=0), the Internal Main oscillator will be forced on.

Bit 0: SYSCLKX2DIS. When set, the Internal Main Oscillator's doubler is disabled. This will result in a reduction of overall device power, on the order of 1 mA. It is advised that any application that does not require this doubled clock should have it turned off.

For additional information, reference the OSC_CR2 register on page 178.

The following table lists the units of measure used in this section.

Symbol	Units of Measure	Symbol	Units of Measure
°C	degree Celsius	µs	microsecond
AC	alternating current	µV	microvolts
dB	decibels	µVrms	microvolts root-mean-square
DC	direct current	mA	milliampere
fF	femto Farad	ms	millisecond
Hz	hertz	mV	millivolts
k	kilo, 1000	ns	nanosecond
K	2^{10}, 1024	nV	nanovolts
KB	1024 bytes	Ω	ohm
Kbit	1024 bits	pF	pico Farad
kHz	kilohertz	pp	peak-to-peak
kΩ	kilohm	ppm	parts per million
MHz	megahertz	sps	samples per second
MΩ	megaohm	σ	sigma: one standard deviation
µA	microampere	V	volts

Absolute Maximum Ratings

Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-65	–	+100	°C	Higher storage temperatures will reduce data retention time.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss-0.5	–	Vdd+0.5	V	
–	DC Voltage Applied to Tri-state	Vss-0.5	–	Vdd+0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
–	Static Discharge Voltage	2000	–	–	V	
–	Latch-up Current	–	–	200	mA	

Operating Temperature

Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See “Thermal Impedances” on page 32. The user must limit the power consumption to comply with this requirement.

3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	3.92	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	µs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	–	–	5.41	µs	
	Power = Low, Opamp Bias = High	–			µs	
	Power = Medium	–			µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	µs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.31	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	2.7	–		V/µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	V/µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.24	–		V/µs	
	Power = Low, Opamp Bias = High				V/µs	
	Power = Medium				V/µs	
	Power = Medium, Opamp Bias = High	1.8	–		V/µs	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	V/µs	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	V/µs	
BW_{OA}	Gain Bandwidth Product					Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels.
	Power = Low	0.67	–		MHz	
	Power = Low, Opamp Bias = High				MHz	
	Power = Medium				MHz	
	Power = Medium, Opamp Bias = High	2.8	–		MHz	
	Power = High (3.3 Volt High Bias Operation not supported)	–	–	–	MHz	
	Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported)	–	–	–	MHz	
E_{NOA}	Noise at 1 kHz (Turbo Medium)	–	200	–	nV/rt-Hz	